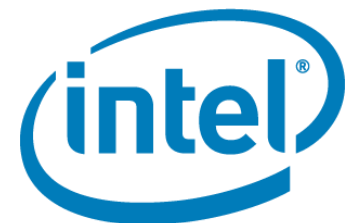


WideIO Memories

Ken Shoemaker, Intel

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December 2011

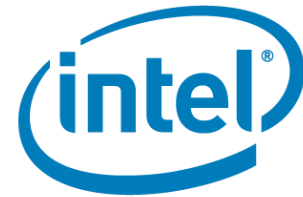




Disclaimer

- ▶ All information in this presentation is subject to change without notice.
- ▶ Refer to the JEDEC website for final specifications, when available

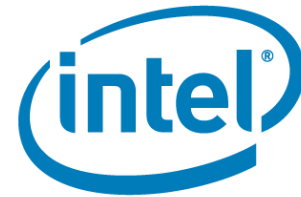
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Overview

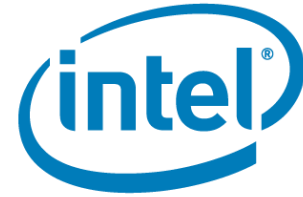
- ▶ Why 3D Logic + DRAM
- ▶ JEDEC Roadmap
- ▶ Details of WideIO Interface
- ▶ Challenges
- ▶ Future

Why 3D Logic + Memory

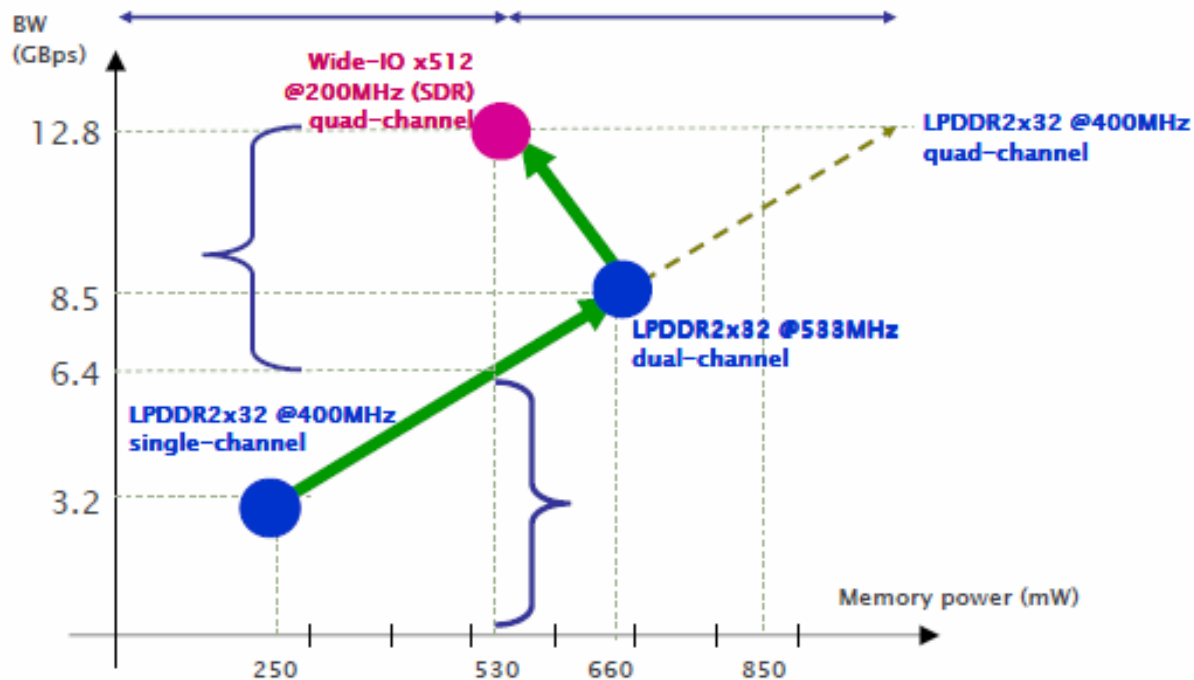


- ▶ Relentless need for increased memory bandwidth and improved memory power efficiency
 - Memory interface is the highest bandwidth interface in the system
 - System performance tied to memory bandwidth
 - Especially for graphics oriented devices
 - Memory power a growing portion of overall system power
- ▶ Process/cost differences between logic and DRAM chips
 - Logic chips focus on improving speed and power efficiency of logic functions
 - DRAM chips focus on reducing the area and reducing the refresh requirements for dynamic RAM cells
 - Very different device characteristics, wafer costs and throughput times

Why 3D Logic + Memory

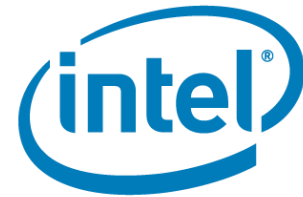


- WideIO offers twice the bandwidth of LPDDR2 at the same power

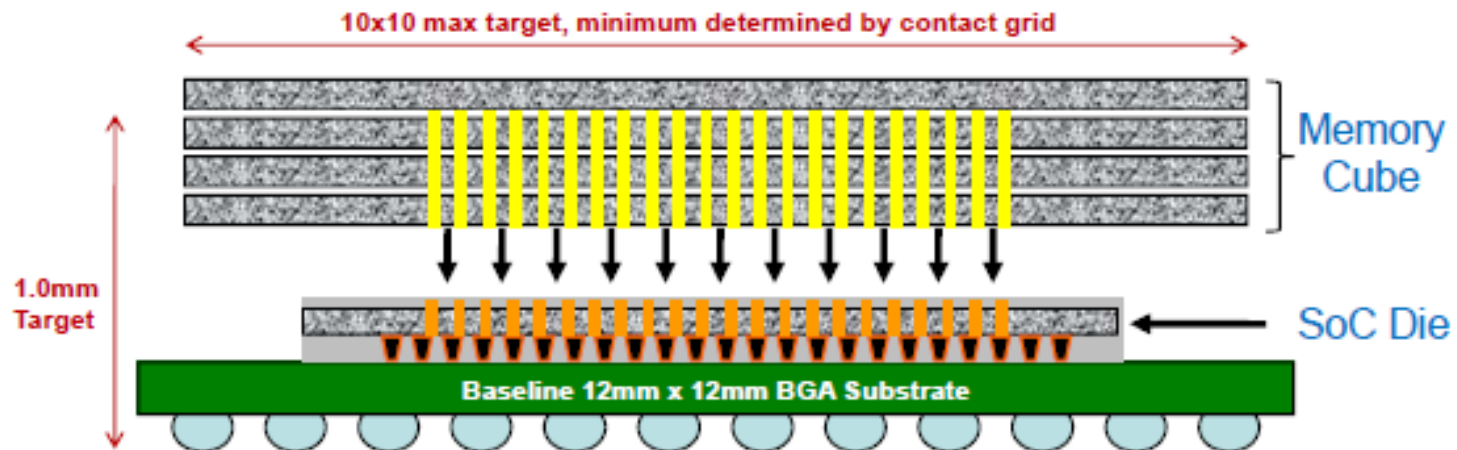


Source: Sophie Dumas, STE, Mobile Memory Forum, June' 11

Why 3D Logic + Memory

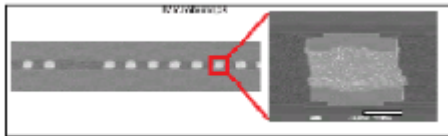


- ▶ WideIO enables thinner and smaller form factors

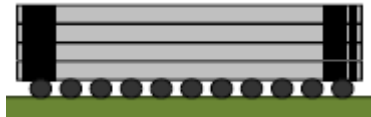


Source: Dan Skinner, Micron, Mobile Memory Forum, June' 11

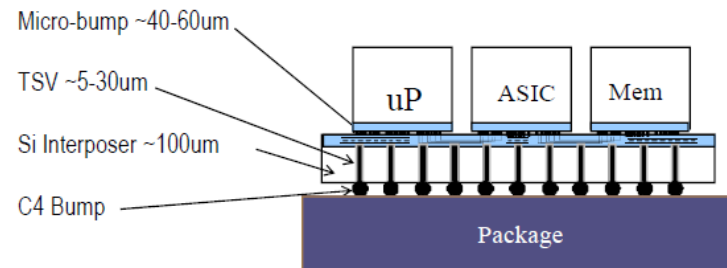
Example 3D Assemblies



- ▶ Face to Face
- ▶ No TSV in Logic or Memory



- 3D Stacking
- TSV in Logic and Memory



- Side by Side
- TSV in Si Interposer

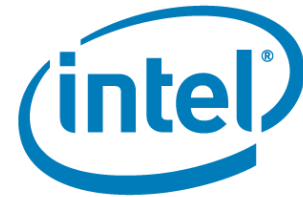
Source: K
Kumagai, 2006
ISSCC

JEDEC Roadmap



- ▶ Investigation began December '08
 - Task group under JC42.6 (low power DRAM) committee
 - Task group chartered to achieve 2x LPDDR2 bandwidth and 2x LPDDR2 power efficiency
- ▶ First WideIO specification available (internally) December '10
 - Published by JEDEC December'11
- ▶ Work begun on next Generation WideIO interface in December'11
- ▶ Industry participation:
 - Samsung (TG lead), Elpida, Hynix, Micron, Qualcomm, TI, Intel, ST, AMD, Apple, Advantest, others

What Is Specified?



- ▶ The Logic/Memory Interface (LMI) is defined
- ▶ Two JEDEC Committees: JC42.6 (Low Power DRAMs) and JC11 (Mechanical Standardization)
 - JC42.6 covers functional aspects of the device
 - Electrical, protocols, geometries, ballout, etc.
 - JC11 covers mechanical aspects of the chip
 - Pad dimensions, tolerances, locations, etc.
- ▶ Mechanical interface is called a micropillar gate array (MPGA)

What Is Specified?



- ▶ Novel items standardized
 - Boundary scan (to test interconnect continuity)
 - Post-assembly direct access memory array test
 - Exact mechanical layout of the chip-to-chip interface
 - Memory thermal sensor locations
 - Provides reliable operation with induced thermal gradients

What Is Not Specified



- ▶ Internal aspects of memory chip/memory stack design or manufacture
- ▶ Interconnect method between memory and logic chip
 - Spec can support any of the 3 example assemblies
- ▶ Exact mechanical placement of interface on either the memory or the logic chip
- ▶ Dimensions/placement of TSVs

What Is Not Specified



- ▶ Thickness of chips
- ▶ Post-assembly test methods for memory array or SoC
- ▶ Business model



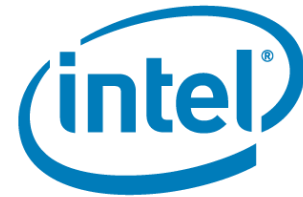
Details of the Interface

- ▶ WideIO defines 4 memory channels on the LMI
 - Each channel is 128 data bits wide; 512 data bits total
 - Each channel includes all control, power and ground for the channel
 - Power connections shared between channels
 - Each channel is independently controlled
 - Independent control, clock and data
 - Each channel is 300 connections, 6 rows x 50 columns
 - 1200 total connections in all 4 channels
 - Pin locations are symmetric between channels



Details of the Interface

- ▶ Up to 4 ranks per channel (presumes 4-high DRAM stacks)
 - Multiple drive strengths
- ▶ 1.2v CMOS signal levels, no termination
- ▶ Pad pitch is 40u x 50u
 - Total LMI dimension is 0.52mm x 5.25mm



Details of the Interface

- ▶ Data rate is 266mtps, SDR
 - Total bandwidth: 17Gbytes/sec (4.26Gbytes/sec per channel)
- ▶ LPDDR-like commands
 - Standard activate/read/write/precharge commands
 - Support for self refresh, TCSR, PASR
- ▶ LPDDR-like core timing parameters

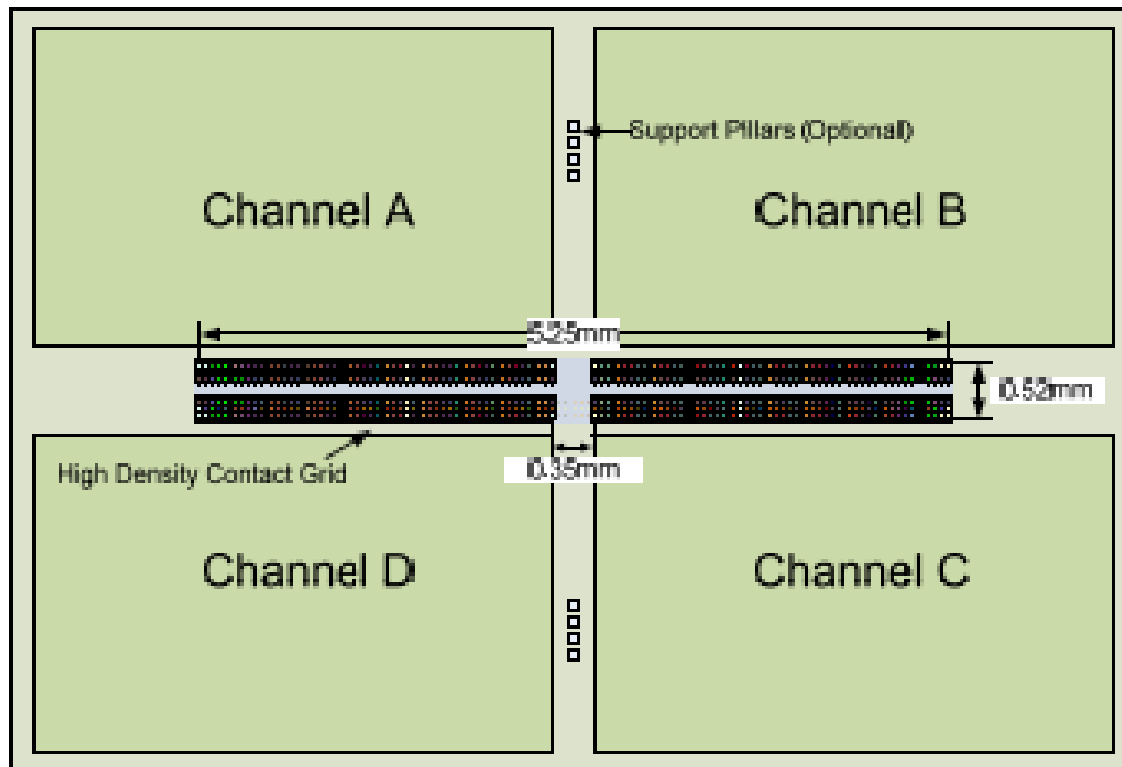


Details of the Interface

Channel A														Channel B					
44	45	46	47	48	49	50							51	52	53	54	55	56	
C44	C45	C46	C47	C48	C49	C50							C50	C49	C48	C47	C46	C45	
2150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950	3000	3050	
VDD2	VDD2	DM15a	DAa	DM14a	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DM14b	DAb	DM15b	VDD2	
VDD2	VDD2	DQ123a	NC	DQ118a	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DQ118b	NC	DQ123b	VDD2	
DQ108a	DQ124a	VDDQ	DQS7_c a	VSSQ	DQ112a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ112b	VSSQ	DQS7_c b	VDDQ	DQ124b	
DQ109a	DQ125a	VDDQ	DQS7_ta	VSSQ	DQ113a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ113b	VSSQ	DQS7_tb	VDDQ	DQ125b	
DQ110a	DQ126a	DQ122a	DQ119a	DQ117a	DQ114a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ114b	DQ117b	DQ119b	DQ122b	DQ126b	
DQ111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0_n	nb	nb	nb	nb	nb	nb	RST1_n	DQ115b	DQ116b	DQ120b	DQ121b	DQ127b	
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	
DQ111d	DQ127d	DQ121d	DQ120d	DQ116d	DQ115d	RST3_n	nb	nb	nb	nb	nb	nb	RST2_n	DQ115c	DQ116c	DQ120c	DQ121c	DQ127c	
DQ110d	DQ126d	DQ122d	DQ119d	DQ117d	DQ114d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ114c	DQ117c	DQ119c	DQ122c	DQ126c	
DQ109d	DQ125d	VDDQ	DQS7_td	VSSQ	DQ113d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ113c	VSSQ	DQS7_tc	VDDQ	DQ125c	
DQ108d	DQ124d	VDDQ	DQS7_cd	VSSQ	DQ112d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ112c	VSSQ	DQS7_cc	VDDQ	DQ124c	
VDD2	VDD2	DQ123d	NC	DQ118d	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DQ118c	NC	DQ123c	VDD2	
VDD2	VDD2	DM15d	DAd	DM14d	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DM14c	DAc	DM15c	VDD2	
2150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950	3000	3050	
C44	C45	C46	C47	C48	C49	C50							C50	C49	C48	C47	C46	C45	
44	45	46	47	48	49	50							51	52	53	54	55	56	
Channel D														Channel C					

Details of the Interface

Wide I/O Floorplan



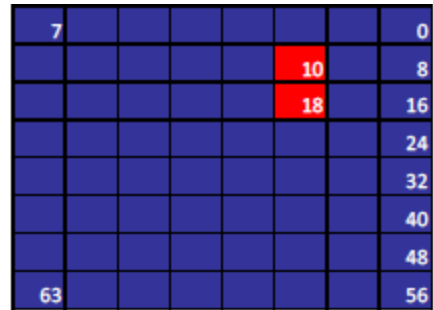
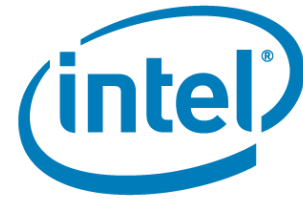
Source: Dan Skinner, Micron, Mobile Memory Forum, June '11

Thermal Considerations

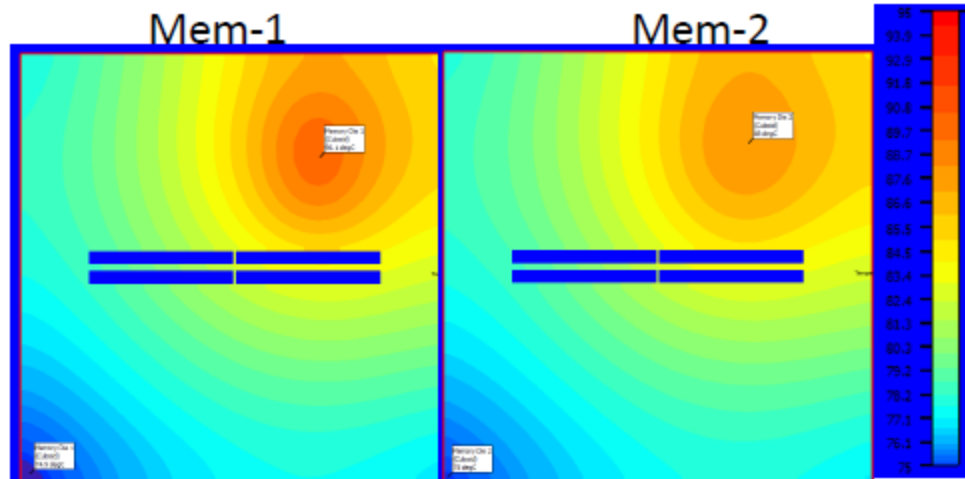


- ▶ DRAM expects uniform temperature of device
- ▶ Logic chip can generate hot spots caused by non-uniform duty cycle of modules

Thermal Considerations



8x8, 1mm² square (64mm² total a
2 mW/square
600 mW/square
1324 mW total



Thermal Solution

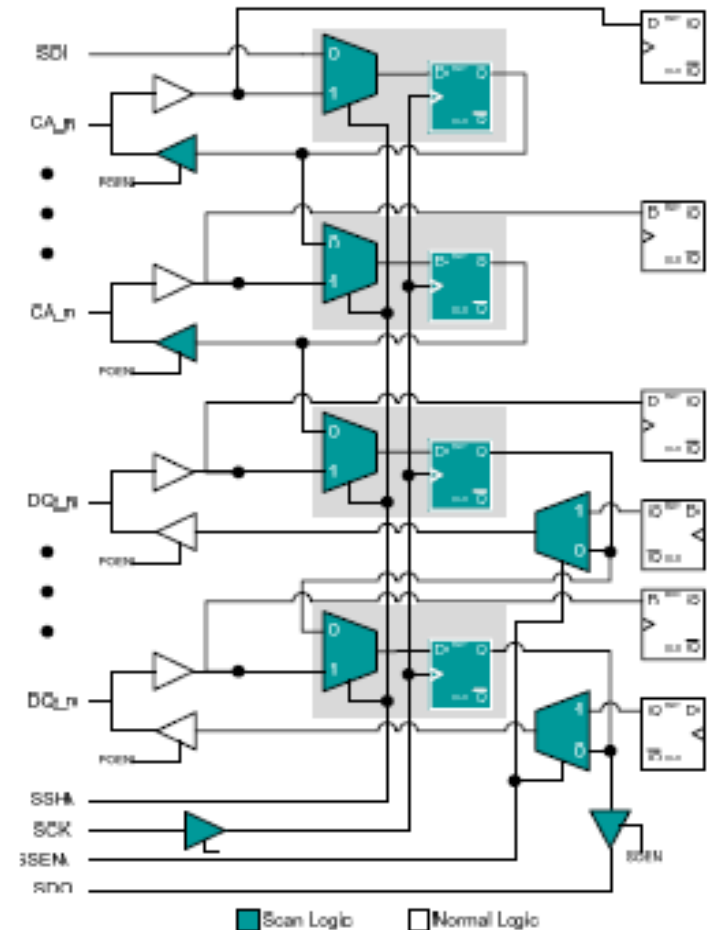


- ▶ DRAM self-refresh rate varies with temperature
 - DRAM has one or two thermal sensors
 - Thermal sensor accuracy and protocol are proprietary
- ▶ Logic chip “hot spots” vary between design and within time in a single design
- ▶ Solution: logic chip determines the temperature delta between its hot spot and the memory thermal sensor
 - Small thermal gradient within stack
 - Standardized locations for memory thermal sensors



Boundary Scan Test

- ▶ Boundary Scan Logic is integrated into the die for contact and I/O testing
 - Serial scan in/out
 - Parallel capture in/out
- ▶ Provides full test coverage for MPGA contacts, drivers and receivers



Source: Dan Skinner, Micron,
Mobile Memory Forum, June' 11



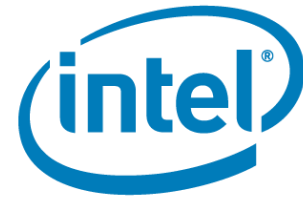
Direct Access Test

- ▶ WideIO provides two means of post-assembly DRAM testing
 - Direct Access:
 - Direct pass through to DRAM pins
 - Mechanical connection between package and DRAM pin
 - GPIO:
 - Electrical connection through GPIO drivers/receivers on SoC and memory drivers
- ▶ Both enable full array testing from limited number of package pins



Future

- ▶ Next Generation WideIO Discussions Begun
 - Proposals for significantly greater (up to 8x) bandwidth
 - Explicit support for 2.5D assembly
- ▶ JEDEC High Bandwidth Memory (HBM) group also active
 - WideIO-like DRAM using mainstream memory process
 - Higher performance at but at higher power
 - Wider interface (1024b proposed)
 - Targets: local graphics memory, networking and high performance computing



Conclusions

- ▶ 3D provides significant efficiency and functional advantages over conventional memory packaging
- ▶ 3D standards create new requirements
 - But many elements can be the same
- ▶ Standardized interface simplifies design
- ▶ Standardized interface enables interchangeability