

OpenPDK Coalition: Status Report

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Interoperability – Standards – Collaborative Technology

Innovation Through Collaboration



Expected OpenPDK Scope

- Stakeholder-specified requirements:

- Interoperable symbols
- Device Parameter Specifications
- Callback Specifications
- SPICE Socket
- OA Technology File enhancements
- OpenDFM verification rules (DRC/LVS/Litho/Targeting/...)
 - ◆ Exploits synergy with DFM Coalition to add specific enhancements on top of OpenDFM from DFMC

First Beneficiary:

All foundries / all nodes

All foundries / all nodes

All foundries / all nodes

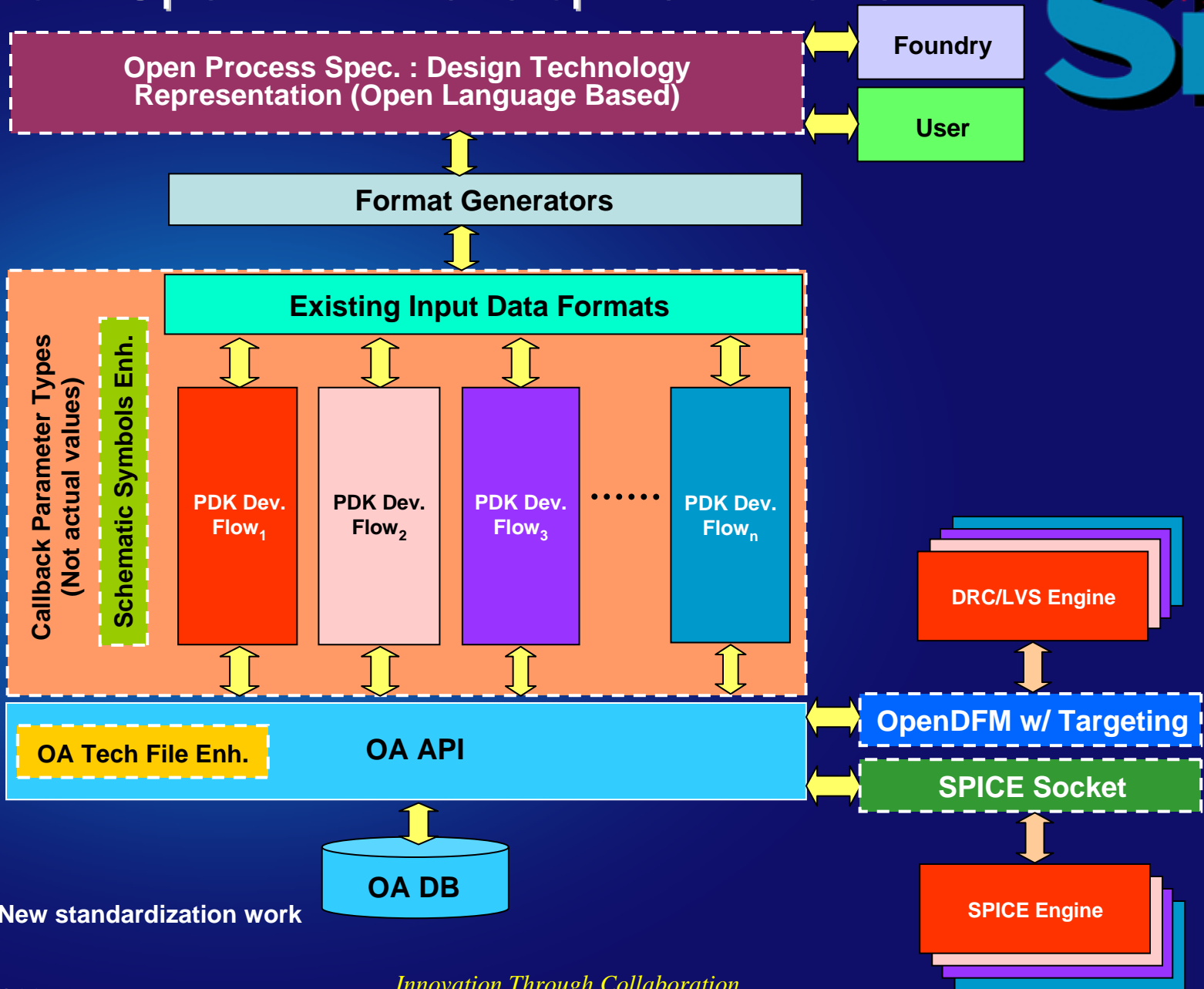
All foundries / all nodes

32nm & 22nm

All foundries / all nodes
(22nm initially for Targeting)

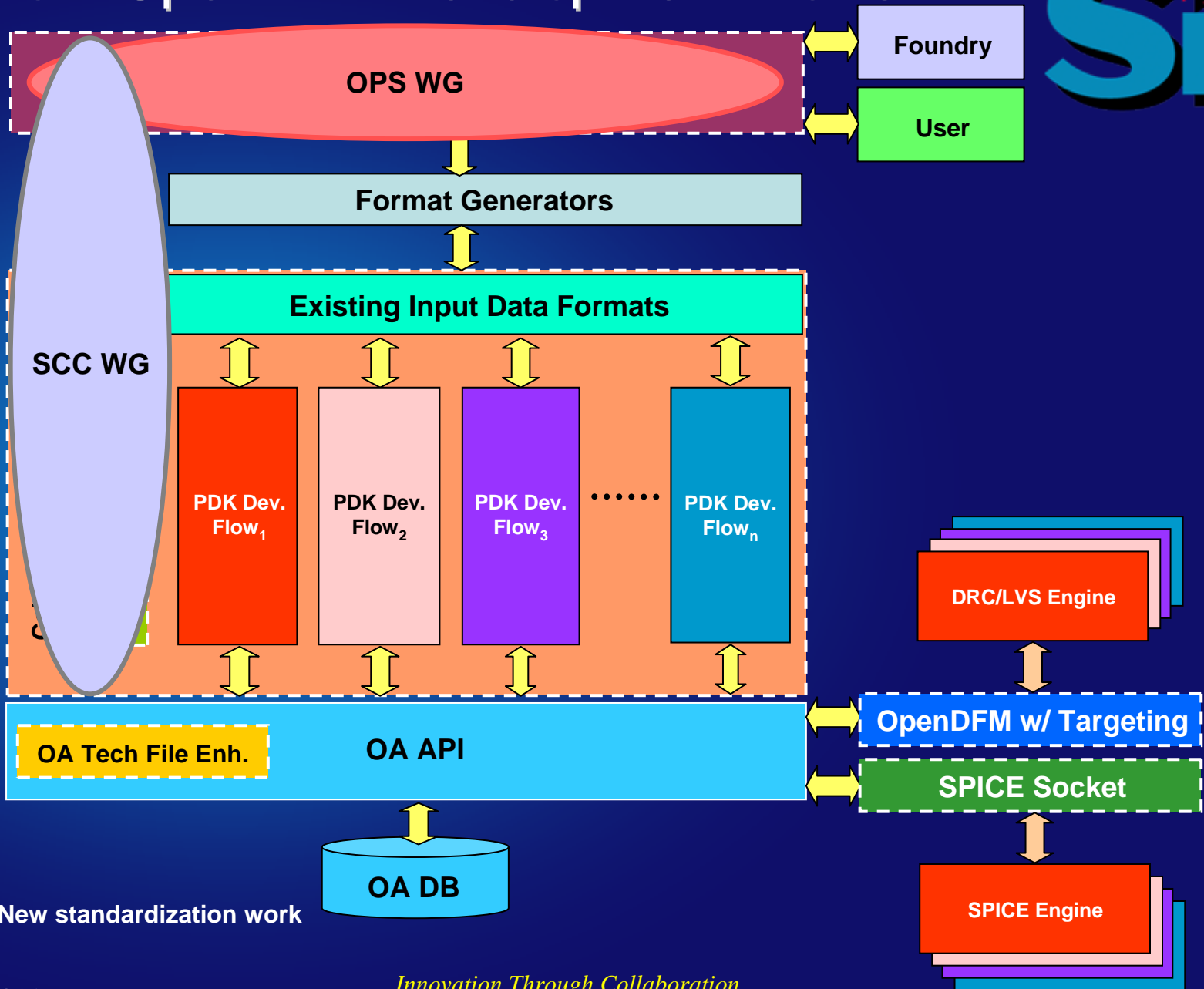


Vision: OpenPDK Development Flows





Vision: OpenPDK Development Flows



- - - New standardization work



Open Process Spec. WG (OPS WG)

- **Goals:**
 - Develop industry–standard specifications for representing process information for electrical definition of Process Design Kits
- **OPS scope includes:**
 - Technology layers
 - Tool-specific layers
 - Technology constraints
 - Design rules
 - DFM/DFY rules
 - Electrical parameters, e.g., dielectric coefficients
 - Process parameters
 - Device specifications
 - Design Kit test harness,...



Symbols, CDF Parameter & Callbacks WG (SCC WG)

- **Goals:**
 - Develop device parameter & callback standard specifications
 - Augment Si2 Symbol Library with additional symbols, parameters and properties
- **Scope of proposed standards includes:**
 - Develop specification for device parameters (a la “CDF”)
 - Define semantics for parameter and attribute keywords
 - Current parameters used commonly in PDKs should be easily captured by new specification
 - Develop specification for CDF callback mechanism
 - Define symbols to add to the current set of Si2 standard symbols
 - Define OpenAccess specifications for CDF as an interoperability goal

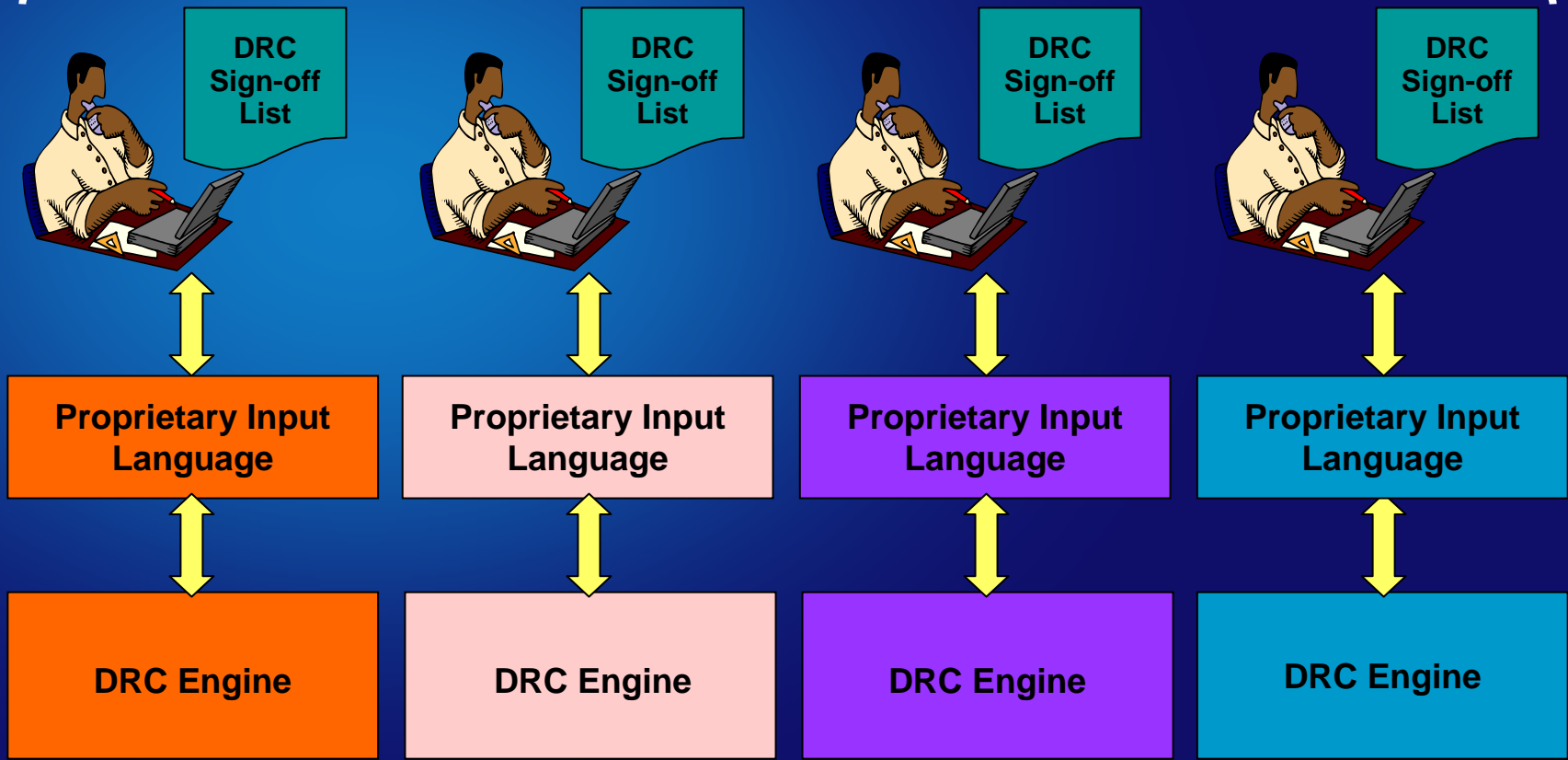
Design Rule Checking Today



DRC Sign-off List



How am I ever going to keep them synchronized?



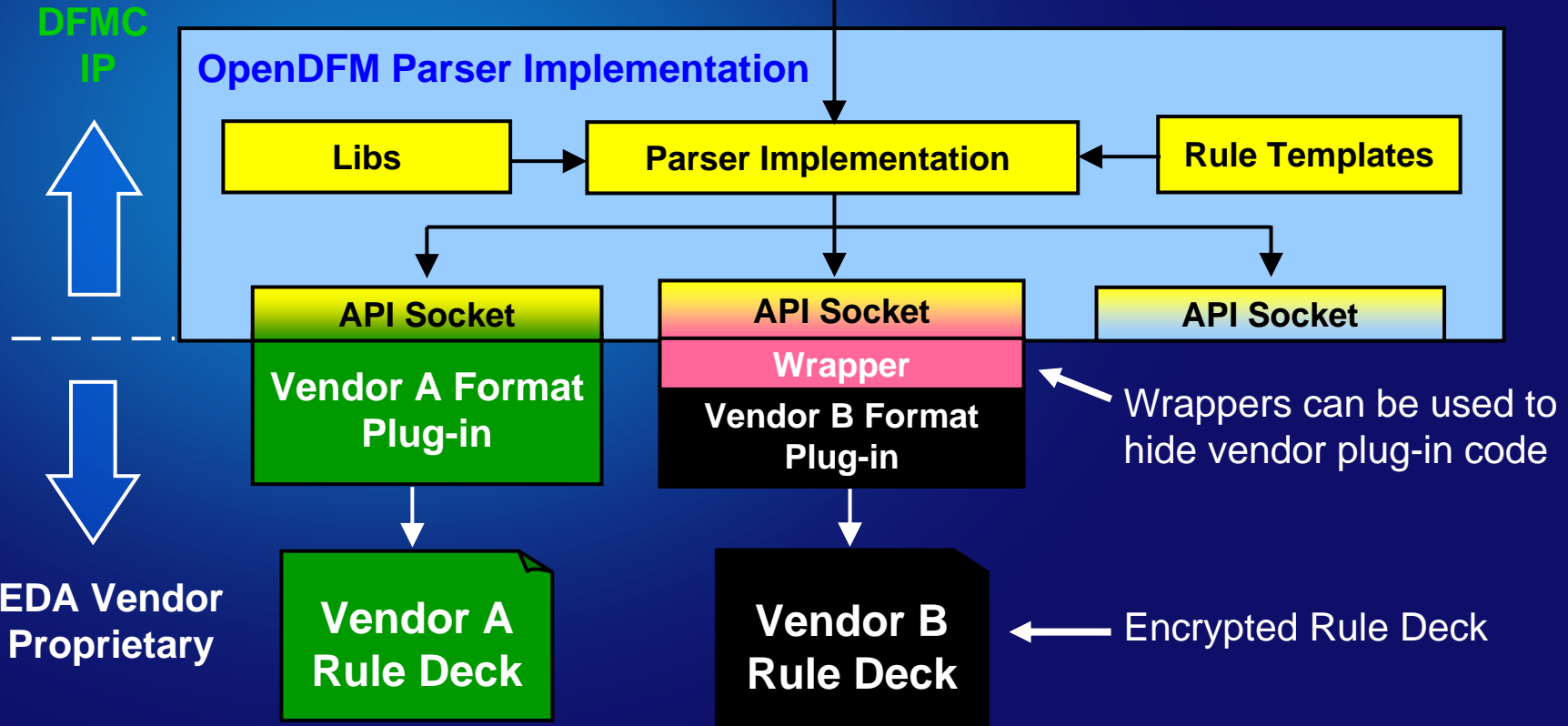


OpenDFM Architecture: Improved Security

OpenDFM:
Si2 Standard format for physical verification

Source File
OpenDFM Rules
3X - 5X Smaller

OpenDFM describes **verification intent**,... and **NOT** how to verify

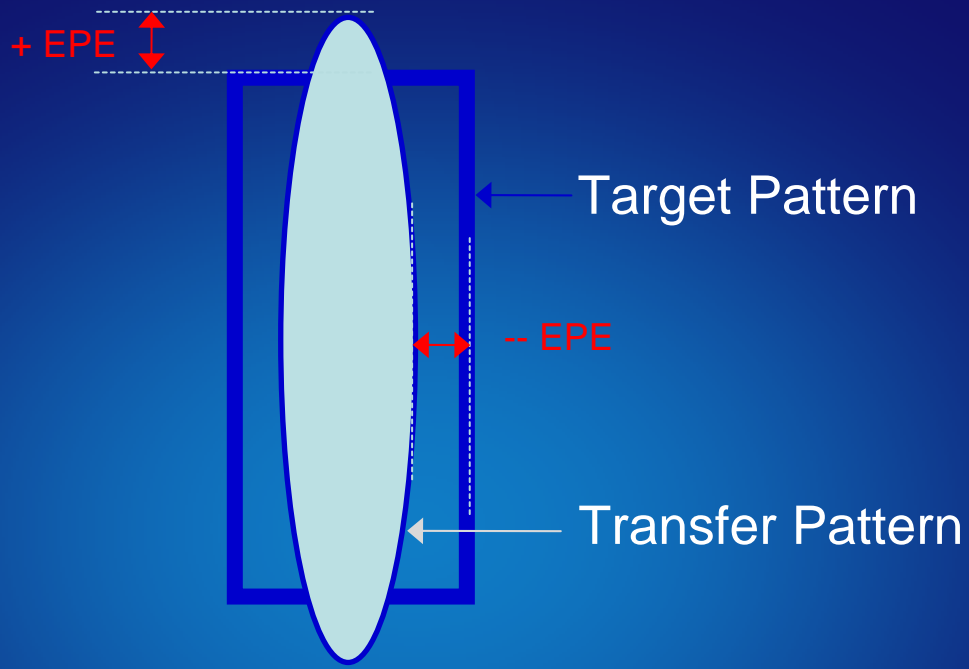


EDA Vendor Proprietary

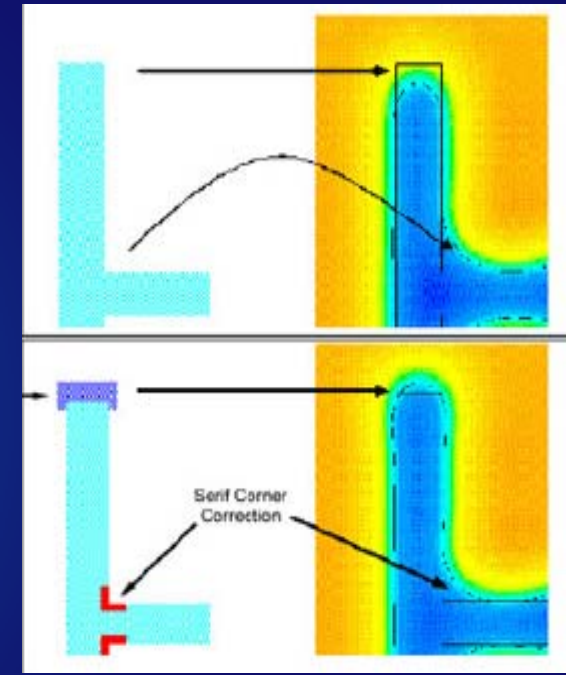
Wrappers can be used to hide vendor plug-in code

Encrypted Rule Deck

Targeting: What is It?



Lithography Process



The **Target Pattern** is the ideal on-silicon pattern.

The **Transfer Pattern** is the actual on-silicon image that results from:
 f (Illumination, Lens_Abberations, Diffraction, Polarization, Defocus, Exposure, Reflectic_Coatings, Resist_Stack, Mask_Misalignment , Etch, Pattern_Context)

Targeting is the process to bring the 2 closer together

EPE = Edge Placement Error



In Conclusion...

- **OPS WG status**
 - Elected Flavien Delauche (ST Microelectronics) as chair
 - Received contribution of UML description of device structure from ST Micro
 - Chosen Eclipse/TestCaseD as UML editor
- **SCC WG status**
 - Elected Barry Nelson (Cadence) as chair
 - Created 3 parallel sub-groups to drive faster progress
 - Received contribution of 30 new symbols from SpringSoft
 - Chosen YAML as repository for symbol / device data
- **DFMC Targeting spec. status**
 - Spec. within 1 week of starting 60-day exclusion period (EP)
 - Verified with 1 user and 1 EDA company, more verification underway
 - Beta version of parser within 1 week of completion
 - Target date for standard release: 03/31/2011
- **In conclusion...**
 - Momentum building, exciting things underway, members making critical decisions
 - If interested, please contact Bob Carver (bobc@si2.org) for membership details

Thank You!

