



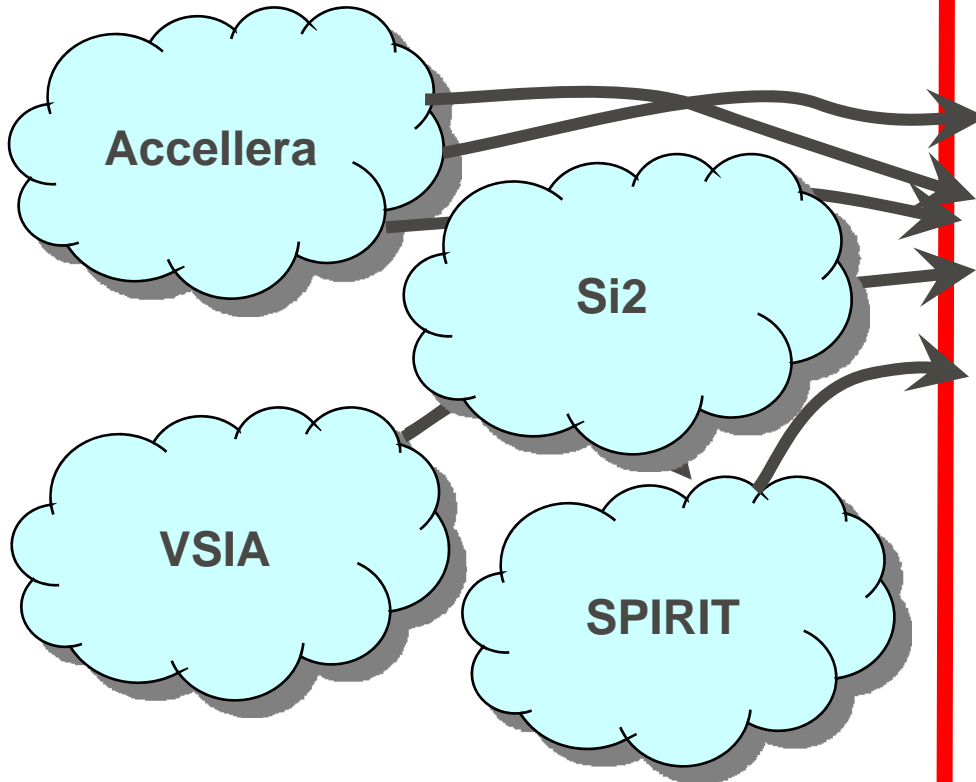
# **SPIRIT IP-XACT & IEEE Standards GSA EDA Standards Discussion**

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Vice Chair, IEEE P1801  
Past architect, Si2 Low Power Coalition**

# EDA Standards Development Today

## Early Discussion / Planning



## IEEE Standard Process

1	2	3	4	5	6	7	8	9	10	11
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1. Initiating a Project
2. Project Authorization Request (PAR)
3. Working Group Extension Requests
4. Has Your PAR Been Approved?
5. Working Group Development
6. Writing the Draft
7. Balloting the Draft
8. Final Approval
9. Publishing the Standard
10. Reaffirming the Standard
11. IEEE Standards Forms

## EDA Standards Listing

– not complete

– shown to provide a scope to the problem

- IEEE IEEE-SA – LSI Corporate membership
  - P1685: IP-XACT: XML Meta data and Tool Interfaces
  - P1734: QIP – IP Quality Metrics
  - P1735: IP Encryption
  - P1801: Low Power Design Intent
- Accellera P1801
- Open SystemC Initiative (OSCI)
  - SystemC
  - TLM (Transaction Level Modeling)
- Silicon Integration Initiative (Si2)
  - Design Technology Council (DTC)
  - Low Power Coalition (LPC)
  - Open Access Coalition (OAC)
- The SPIRIT Consortium
  - IP-XACT
  - SystemRDL – register description language
  - Debug, verification, Documentation working groups
  - Interworking with: OASIS, Eclipse, Si2, Low Power
- Virtual Socket Interconnect Alliance (VSIA) – finished!
  - Transferred to IEEE, The SPIRIT Consortium, OCP, and the Public Domain

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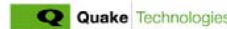
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# Now More Than 100 Members Strong

## Reviewing Members

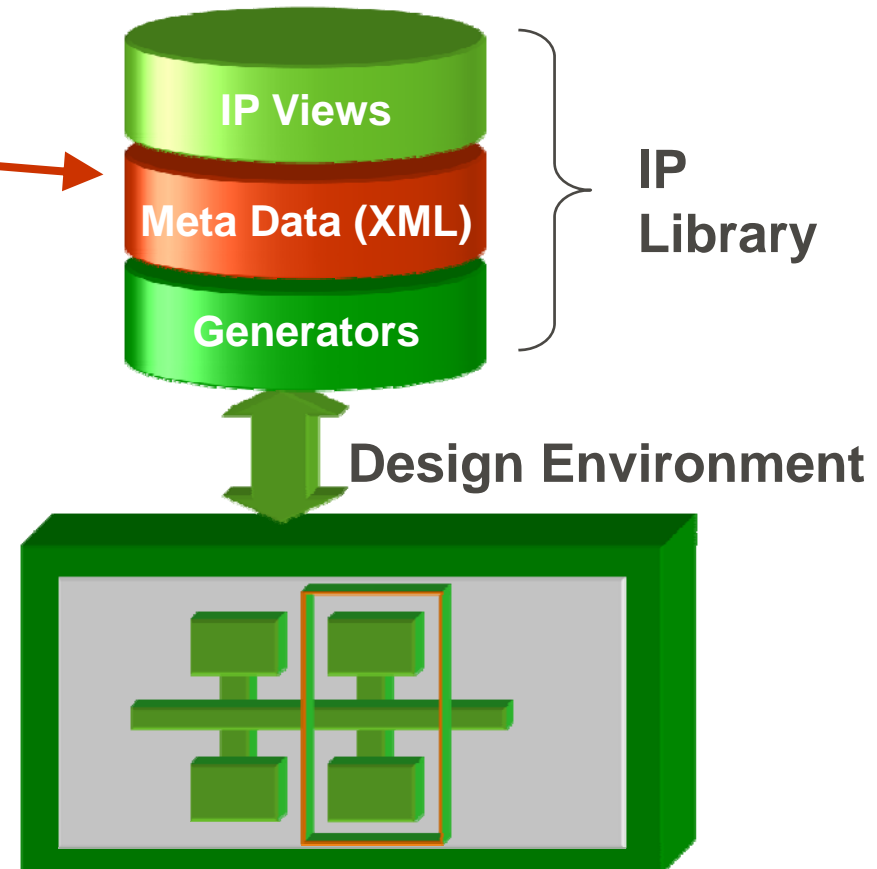




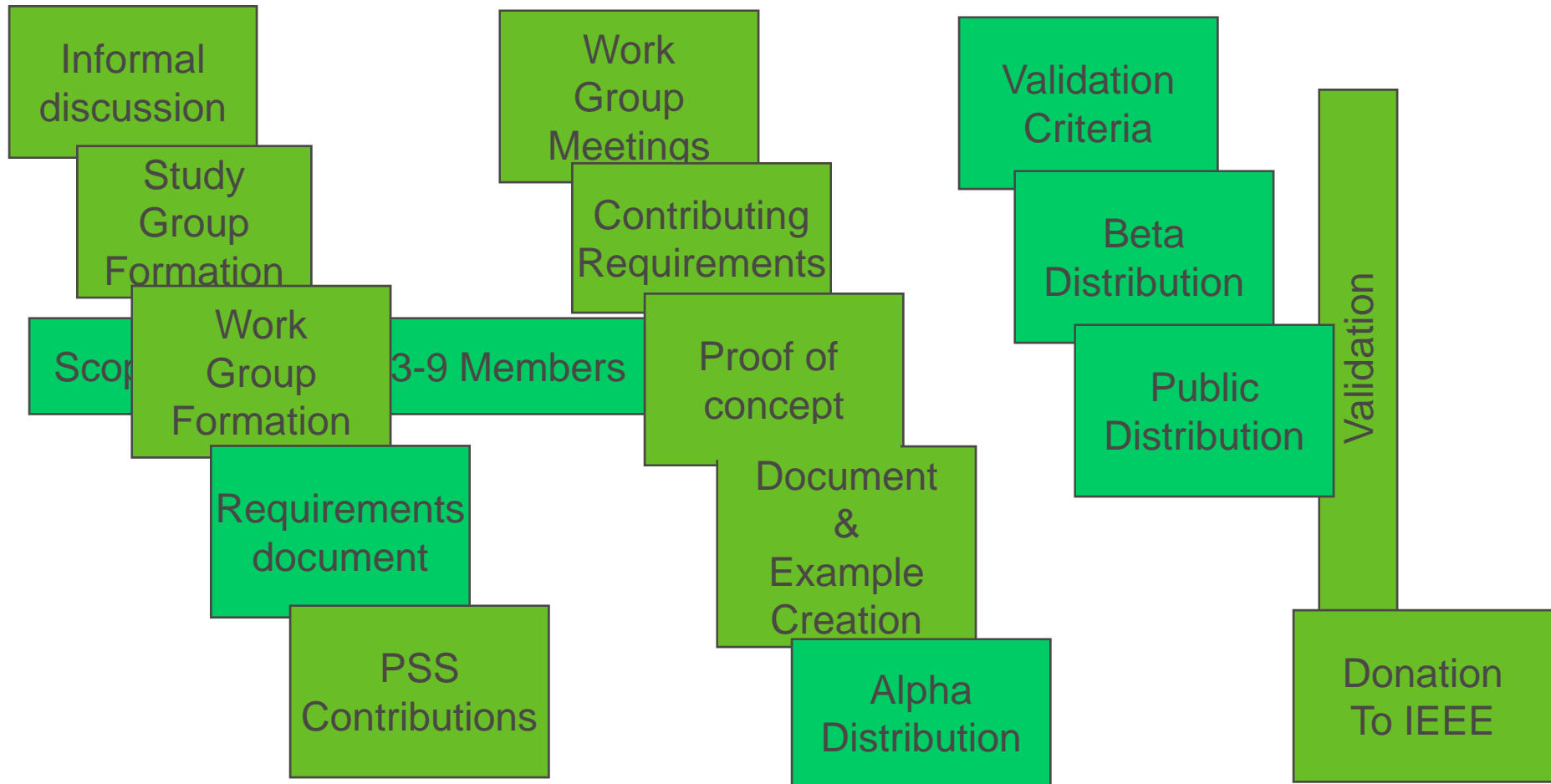
# for IP Descriptions

specifies ...

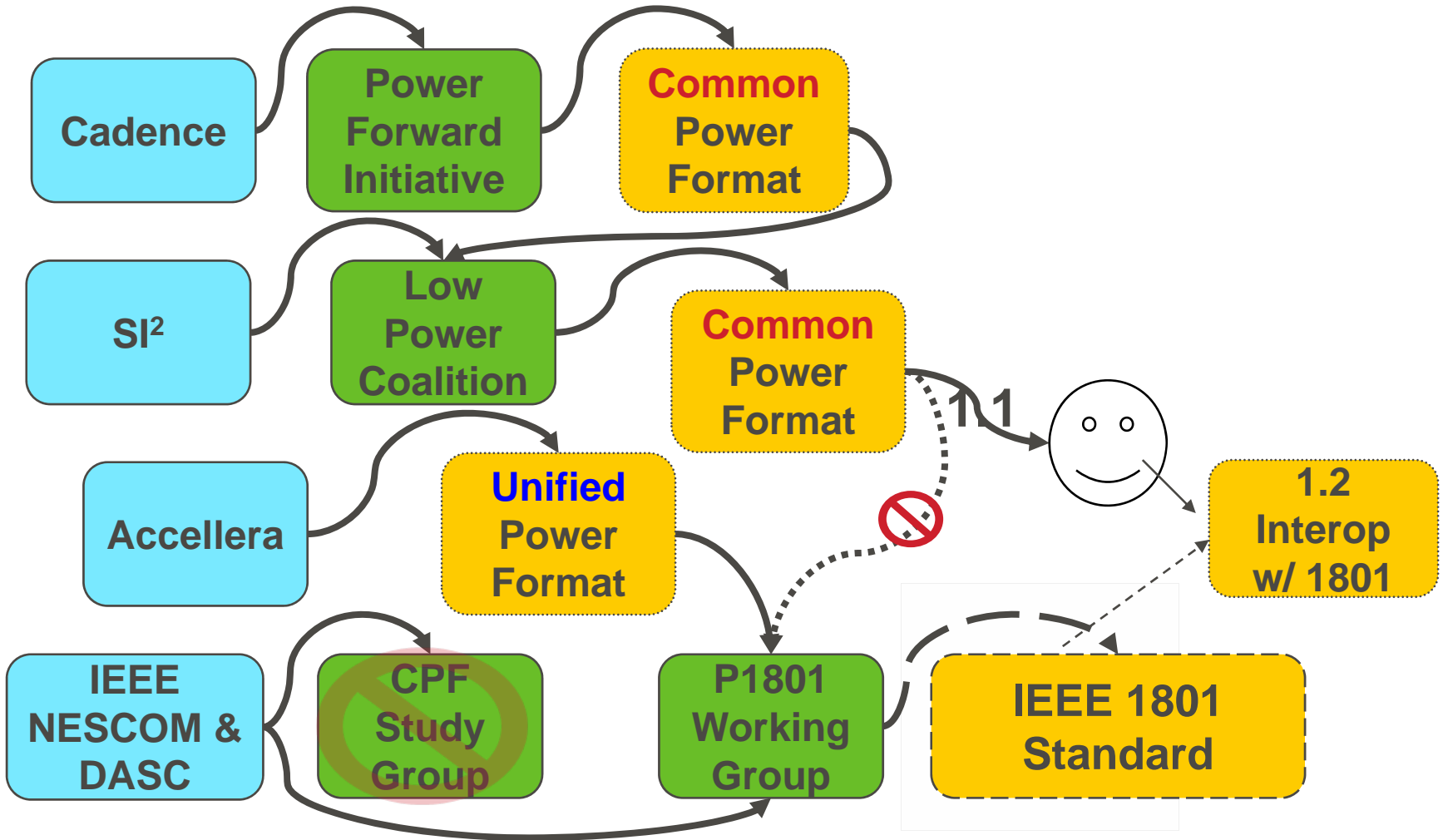
- IP-XACT is The SPIRIT Consortium specification for describing IP
  - Enables automated design creation and configuration
  - Enables designers to include specialist knowledge in their components
- Benefits
  - Build repeatable design flows
  - Access to machine readable description of all aspects of IP using the IP-XACT XML databook
  - Common interface descriptions
  - Tool independent



# Development Process of The SPIRIT Consortium



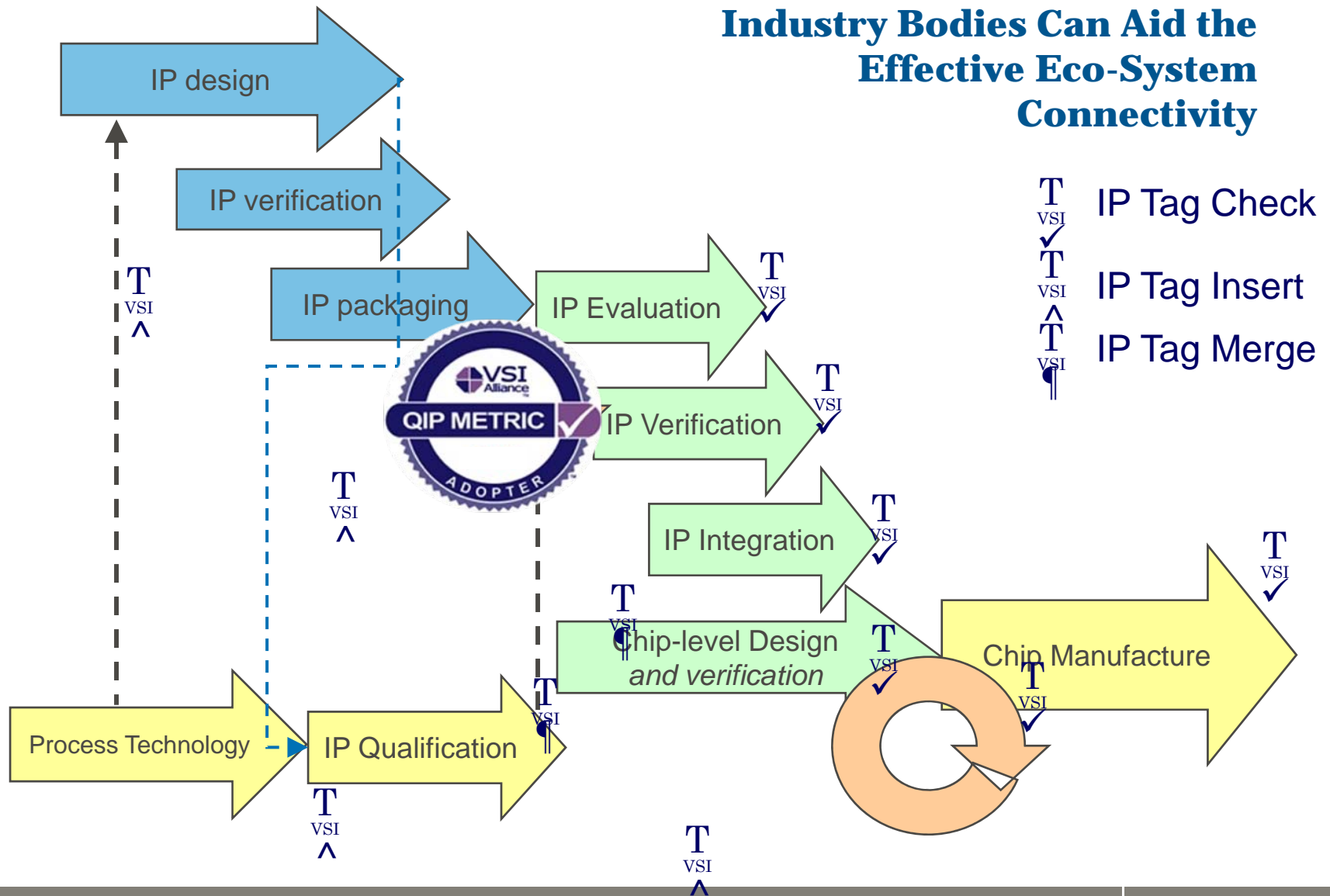
# The Low Power Standards “Program” (you can’t tell the players without “The Program”)



## Verification “Standards”

- In the past, System Verilog and SystemC had many separate implementations, not interoperable.
- OVM
  - Cadence & Mentor combined their contributions and just released
- VMM
  - Synopsys
- VMM “donated” to Accellera
- IP-XACT descriptions work for both
- Performance is an issue for running, but not for configuration
- Why we care
  - verification activities across the corporation are unifying and sharing

# The IP ECO System



## Thank you

- Sometimes competition is inevitable
- Convergence is better
- Fewer is better
  - Less is more