

Analog and Mixed-Signal Connectivity IP at 65nm and Below

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The demand for connectivity intellectual property (IP) for high-speed serial busses such as USB 2.0, PCI Express®, SATA, DDR2 and HDMI is increasing as these standard interfaces are included in SoCs designed for applications such as single chip recordable DVD CODEC's and MP3 players. In order to stretch battery life of these SoCs, the semiconductor technologies require ultra-low power derivatives of high-performance logic manufacturing processes that enable production of very low-power SoCs for these mobile platforms and small form-factor devices. Today, many of these SoCs are manufactured in 90nm process nodes, and the ramp for 65nm design starts has been more aggressive than expected. The 45nm process design is following close behind, with early versions of design rules and process parameters already available.

The challenge from the IP provider's viewpoint is to meet analog performance in a technology that has been targeted for densely packed digital logic. From the SoC integrator's perspective, the IP should be easy to integrate. The IP provider should have already dealt all of the details of creating the IP. The IP should also incorporate new circuit design techniques that accommodate lower supply voltages necessary for portable systems. At the smaller process nodes, design for manufacturing (DFM) must also be taken into account.

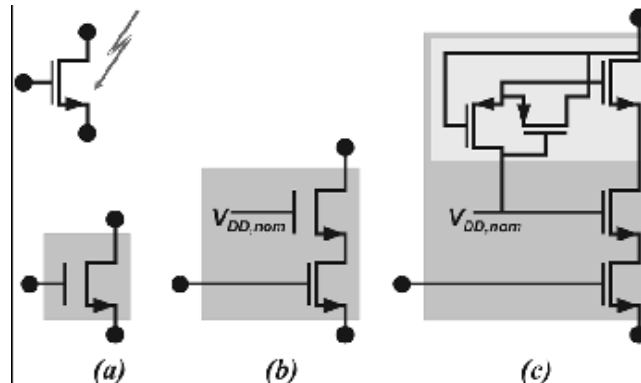
Creating IP at 65nm and Below

Reduced supply voltages mean that architectures that once worked at 3.3 V or 2.5 V now need to work at 1.8 V or lower, without any loss in performance. One way to address this is to use a mixture of high voltage I/O devices with the lower voltage core devices. This will be discussed in the next section. In addition, all the post processing to support DFM requirements increases the performance variation in these devices. This is due to effects like shallow-trench isolation (STI) induced stress, (NMOS becomes slower and the PMOS faster) nwell proximity effects, contact stress and phase shift mask correction algorithms. There is also a time-dependent variation due to negative bias temperature instability (NBTI) in PMOS devices and hot carrier injection (HCI) in NMOS devices.

Circuit Design

Performance can be maintained at 90nm, 65nm and even at 45nm by using a mixture of I/O and core devices. The trick is to know where and how to use them, which is where the expertise of the IP provider comes in.

For analog circuits operating at higher supply voltages, high voltage-tolerant transistors can be used to replace the standard transistors that can only reliably operate up to nominal supply voltages.



1. These I/O transistors are examples of devices that can operate at higher supply voltage levels.

Figure 1 illustrates three examples using I/O transistors that can typically operate at higher supply voltages. These transistors enable direct re-use of most circuit architectures, running at supply voltages corresponding to the original design, but are high supply voltages when compared to the nominal supply voltage of the CMOS process used. These structures are adequate for ESD protection, but more exotic protection schemes are needed for embedded analog functions.

The easiest way to design with high supply voltages is to use the commonly available thick-oxide transistor (*Fig. 1(a)*) that is comparable to a two-generations-old standard transistor. However, in order to benefit from technology scaling, you need to use compound structures that have thin-oxide transistors, as in *Fig. 1(b) or (c)*, which typically outperform the thick-oxide transistor in *Fig. 1(a)* in matching noise and output impedance. These compound structures have some disadvantages: they are asymmetric, do not solve gate-leakage issues and require suitable cascade voltages at power-up.

Careful selection of the analog sections to run at high supply voltages and careful selection of the best type of transistor (thin oxide, thick oxide, or compound) will, to a great extent circumvent one of the main roadblocks in 65-nm CMOS technologies-- the low nominal supply voltage. Note that thick-oxide transistors also solve gate-leakage issues as their gate leakage is usually negligible.

The Impact of Processing

To meet DFM demands, additional processing steps are required. These are also sources that add variation in devices and, therefore, adversely impact IP performance. Some of these sources are described below.

- Shallow trench isolation (STI) is a fabrication method used to isolate active areas and can cause currents to be different from simulation. It depends on transistor location.
- NBTI degrades PMOS devices progressively over time by an increase in the threshold voltage and reduction in mobility due to negative gate bias and/or higher temperatures, usually around 100°C. The net effect is that the PMOS current drive is degraded over time. This can induce timing failures in digital circuits modeled as a $V_{sub>th}$ shift.
- Matched devices, like current mirrors and differential pairs, which are asymmetrically stressed, will have an additional mismatch component, in addition to mismatch from processing variations, causing additional system performance degradation.
- HCI degrades the performance of NMOS devices in a similar way, but through a different physical mechanism to NBTI. Unlike NBTI, HCI is a function of the electric field across the channel (i.e. from drain to source) whereas NBTI degradation is a function of the field across the oxide modeled as an I_{dsat} shift.

These effects do have a serious impact on the design of the analog/mixed-signal portions of the connectivity IP and the vendor must have deep expertise in understanding these effects and including them as automated simulation tools.

With these higher voltages, electro-migration checks for potential short conditions must be made. This can occur on dense arrays of conducting thin-film metallic conductors, and over time, high current densities cause these conductors to fail resulting in metal separation. Also, there should be checks for adequate metal widths and checks for metal/MOS/POLY/VIA/ contacts. Therefore, it is important to have an EDA flow that includes automated checks for junction stress, as well as HCI/NBTI degradation simulations.

Circuit layout must also be able to accommodate well proximity effects. Advanced extraction decks include STI/nwell proximity effects, however, these are only back-annotated after layout is complete. Layout immune methodology helps bridge the gap between schematic simulations and extracted simulation results.

Time-Dependent Variations

A good example of time-dependent variations is the impact of NBTI on the input devices of a USB PHY. In USB designs, for example, the stress on the input devices varies drastically between standby mode and normal high-speed operation. Furthermore, many of these circuits are typically designed with

PMOS input stages in order to handle the low common mode voltage in high-speed operating mode. As a result, these circuits are very susceptible to NBTI induced degradation (V_{th} shifts) which can ultimately compromise their compliance/functionality by causing large input offset voltages on these circuits. An application of temporal NBTI effect can be seen in modern USB designs. The differential USB data lines (DP/DM) are held at opposite polarities during suspend mode, i.e., 3.3 V and ground.

The stress on the input devices varies drastically between suspend mode and normal operation. The duty-cycle between suspend and normal operation can vary, but one could assume 50 percent for sake of an example. Typically, there is sensitive input circuitry connected to the differential data lines (DP/DM), for example, squelch detector, high speed receiver, disconnect detector, etc. Furthermore, many of these circuits are typically designed with PMOS input stages in order to handle the low common mode voltage in high-speed operating mode. As a result, these circuits are very susceptible to NBTI induced degradation (V_t shifts) which can ultimately compromise USB compliance/functionality by causing large input offset voltages on these circuits.

Fortunately, scenarios like this are well understood, and so in this particular case, the designs are usually modified to block the large delta V_{gs} across the sensitive input circuitry when suspended. The true benefit of NBTI modeling/simulation tools are in uncovering non-obvious/subtle scenarios and circuits where designers may not have recognized the potential for large V_t shifts in their design. These tools will enable designers to uncover long-term shifts in the design due to NBTI stress early on in the design process, thereby enabling circuit modifications to mitigate the impact and improve system reliability and performance.

Chip Integration

From the SoC integrator's perspective, the IP vendor should not only address all the issues above, but should also provide all the views for chip floor planning and integration, integration of the analog/mixed signal in the SoC, and the SoC on the board, i.e., LEF and SPICE models of the I/O's. The IP should also have no special requirements for guarding combinations or distances between the IP and the intended SoC.

Other important considerations are that the analog/mixed signal IP is designed in a standard CMOS digital process. There are no process options required such as deep NWEELL or on-chip inductors or varactors.

Since IP providers often don't know where customers will place the IP, they must thoroughly test the noise rejection of the IP in their testchips. They should mimic a very noisy SoC environment, both substrate and supply, when they perform jitter measurements.

Testing becomes a real issue with high-speed analog/mixed-signal designs. It's important to ensure maximum fault coverage with minimum test time. It's impractical to spend 30 seconds on the tester, so the IP should contain hooks to allow the production test engineer to test the IP without adding to the test time budget. The SoC designers do not design the IP and therefore cannot add test features. If they cannot simulate it with a test bench, they cannot test it. Additional issues that the test engineer faces include:

- SoC test engineers usually have vectors they stream in/out from simulation. All analog tests have to be hand coded.
- Test engineers have to devise tests to get acceptable analog fault coverage. The designers do not know much about the analog portion of the IP.
- Most analog tests require external hardware to properly test. Setting up this hardware takes time.

Therefore, the IP vendor needs to provide the appropriate test vectors and IP test features that address these testing challenges.

To illustrate this, the first time that test vectors/code are tested on real silicon is when the SoC comes back from the fab. For example, how does the test engineer incorporate the PCI Express compliance eye-mask into the ATE without changing the signal? He certainly cannot hang a high-speed tester on each pin. The test engineer's concern is that with the simple pass/fail test of the external loop-back approach, he will not know how much margin he has--chips that pass the loop back test that are marginal may fail over time when subjected to real world conditions. Using techniques such as voltage and phase margining, the link can be reliably tested in a production test environment. These limits are set by simple input and compare vectors that are provided with the IP.

The future: 45nm, 32nm and SOI

In scaling to 45nm and below process nodes, the main issues concern the design of mixed-signal IP with 1.8 V thick oxide devices with a 0.9 V digital supply. In order to meet lower leakage and higher speeds, the technology could move to SOI which would require special analog design techniques. The devices can also be optimized by introducing compressive/tensile stress to improve performance.

Summary

The demand for sophisticated connectivity IP is increasing as high-speed serial busses such as USB 2.0, PCI Express, SATA, DDR2 and HDMI are widely adopted. These require high-performance analog/mixed-signal circuits that can be designed using standard deep sub-micron CMOS technologies. However, a thorough understanding of the deep-submicron process effects is necessary to produce working, robust production worthy analog/mixed-signal designs. This requires that IP vendors, in concert with fabrication process engineers, circuit designers and EDA vendors, develop IP that takes process variations and other DFM concerns into account. The IP vendor, therefore, must be carefully chosen to ensure that they understand, not only the intended behavior of the IP, but the silicon processes in which it will be implemented. The IP provider should also have a roadmap that considers the next generations of process nodes and an understanding of the challenges that will arise when customers migrate to these processes. Engineers who use care in choosing such an IP vendor will be able to concentrate on their designs, safe in the knowledge that they are using proven IP that will work properly all the way through device implementation.

References:

1. *Analog Circuits in Ultra-Deep-Submicron CMOS* by Anne-Johan Annema et al IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1, JAN 2005.
2. *A New Simulation Method for NBTI Analysis in SPICE Environment* by Rakesh Vattikonda, Yansheng Luo, Alex Gyure, Xiaoning Qi, Sam Lo, Mahmoud Shahram, Yu Cao, Kishore Singhal and Dino Toffolon.

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