



White paper **Sofics hebistors**

Latch-up Immune on-chip ESD protection for High Voltage processes and applications

While High Voltage interfaces are broadly used in many IC applications like motor control, power management and conversion, LCD panel drivers and automotive systems, many IC designers still lack a low leakage, cost-effective and latch-up immune ESD protection clamp.

This white paper introduces a newly developed protection device and compares it with the traditional approaches, based on measurements on TSMC 0.35um 15V and TSMC 0.25um 40V technology. Within an area of 35.000um², the novel *hebistor* device with holding voltage above 40V achieves more than 4kV HBM, 200V MM while the leakage and capacitance stay well below typical requirements (<10nA and <250fF). Hebistors form a family of high voltage ESD/EOS/IEC protection clamps which are branded under the Sofics *PowerQubic* portfolio.

Introduction

A growing set of IC applications require a high voltage interface. Examples include power management, power conversion and automotive chips with interfaces typically between 12V and 60V. Also mobile devices like cell phones and personal navigation devices today include interfaces above 10V to e.g. control and sense MEMS gyroscopic or compass sensors. And, most LCD/OLED display technologies require driving voltages between 10 and 40V. Besides the power, MEMS and display interfaces many devices include some sort of motor like the optical zoom lens and shutter control of digital cameras or the ‘silent mode’ vibrator in cell phones.

Though these applications represent fast growth markets, the underlying silicon process technologies lack standardized high performance ESD solutions. Today, different protection clamp types are used in the industry, each with significant performance and cost burdens that prevent generic use. The main problems with traditional solutions are high leakage current, large silicon area consumption and extensive custom (trial and error) development cycles for each process/fab change. Sofics introduces hebistors that address these stated needs and requirements.

This white paper first provides an overview of the currently used ESD protection solutions (Section I). In Section II the requirements for a generic high voltage process ESD device are summarized. Section III introduces the innovative solution from Sofics that meets all these requirements within a small silicon area and without the need for semiconductor process tuning. The main benefits are summarized in the Conclusion of this white paper.

I. Comparison of traditional ESD solutions

Today IC designers use a variety of ESD protection devices in HV-CMOS or BCD process nodes to protect integrated circuits against ESD stress. Below a non-exhaustive overview highlights the main types.

1. Zener diodes

Zener based protection devices have been around for a long time. The characteristic behavior is depicted in Figure 1 (type 'a'). The breakdown and holding voltage are above the supply voltage level ensuring latch-up immune ESD protection. Zeners can be applied in many technology nodes though there are many drawbacks for ESD protection:

- The ESD robustness level per micron device width is rather low which leads to a large device size.
- The large device size means that the capacitance and leakage values are higher than any other device type when scaled to the same protection level.
- For many circuits the Zener device cannot provide effective protection due to a too high holding voltage. A change in the holding voltage is possible by dedicated process modifications (doping levels/profiles) with the risk of degrading core functional performance or by adding expensive processing steps and masks. Furthermore IC designers can create applications with different supply voltage levels within one process technology which requires different Zener diodes.

2. RC-MOS (a.k.a. BIGFet)

The dynamically triggered MOS transistor is extensively used in low voltage technology nodes for many general purpose IO libraries. The characteristic behavior is depicted in Figure 1 (type 'b'). The MOS is biased such that all the ESD current is shunted in the active MOS conduction mode. The MOS device is turned off during normal operation. Many different configurations exist to tune the device behavior (timing, boosted bias, false trigger prevention). However, in high voltage technologies the application of RC-MOS devices is less straight forward, typically leading to very large area consumption, even for a low ESD HBM protection level.

3. PMOS, PNP

The HV-PMOS device has a characteristic similar to the Zener device (Figure 1, type 'a'), however, the ESD performance is very process dependent. In 'good' technology nodes the robustness level per micron device width is higher than the Zener device due to the bipolar PNP action. This results in a somewhat better performance for the leakage and silicon area consumption. Moreover, due to a lower breakdown and holding voltage the device is typically better suited to protect sensitive circuits.

4. NMOS, NPN

Designers use NMOS and NPN based approaches because the I_{t2} robustness level is typically higher compared to the 3 previous device types leading to smaller silicon area and reduced leakage. However, degradation issues due to non-uniform triggering are a major problem and road block, as reported and documented by various sources. In addition, the key issue is the latch-up weakness due to a low holding voltage, typically much below the supply voltage. This characteristic behavior is depicted in Figure 1 (type 'c').

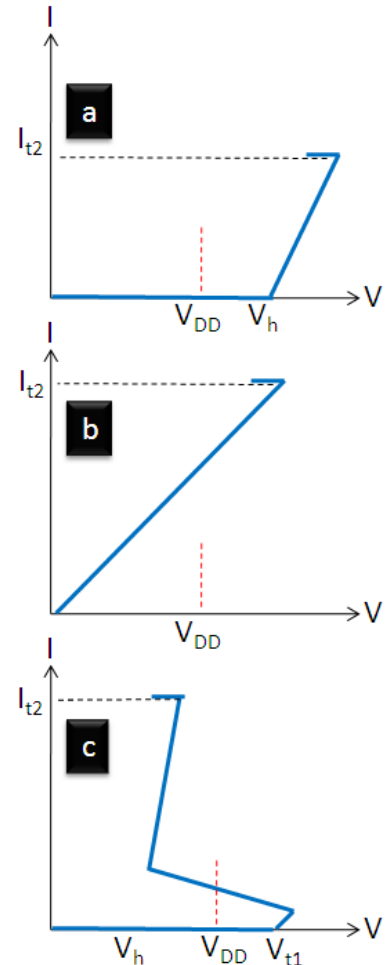
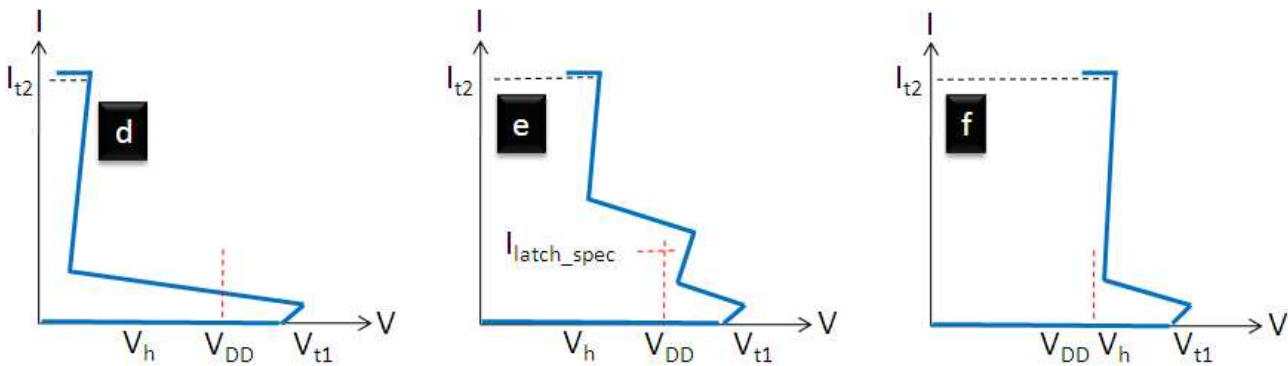


Figure 1: Simplified behavior of the main ESD solution types used for protection of high voltage interfaces: (a) Zener diode, (b) RC MOS, (c) NMOS or NPN device

5. SCR

Finally for some high voltage signal pins it is possible to rely on Silicon Controlled Rectifier (SCR) based protection devices. SCRs have superb ESD characteristics with low leakage and low capacitance but require careful high holding and trigger current control to avoid latch-up problems. The characteristic behavior of the basic SCR device is depicted in Figure 1 (type ‘d’) while the Sofics latch-up improved high holding current (HHI) SCR approach is shown as type ‘e’.

The table in Figure 1 summarizes the different devices with advantages and disadvantages. The star rating is based on extensive benchmarking of high voltage technologies from various foundries and IDMs but it is not an absolute overview. Exceptions exist where e.g. processes are modified to enhance the ESD properties of certain devices. Clearly within the existing device pool there is no generic and no optimal solution. It basically comes down to a selection between a cost-effective design (NPN, SCR) with major latch-up immunity weakness or a guaranteed latch-up immune design that occupies a huge chip area (Zener diode, PMOS). A single, generic device that solves all the different aspects would greatly simplify IC design in HVCMOS and BCD process technology.



Clamp	Curve	Flexibility	Effective protection	ESD/Area	JEDEC Latch-up immunity	Transient Latch-up immunity	ESD/Leakage
Zener diode	a	I_{max}	☆	☆	☆☆☆☆☆	☆☆☆☆☆	☆
RC-MOS	b	I_{max}, V_{t1}	☆☆☆☆☆	☆	☆☆☆☆☆	☆☆☆	☆
PNP, PMOS	a	I_{max}	☆☆	☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆☆
NPN, NMOS	c		☆☆☆	☆☆☆	☆	☆	☆☆☆
BASIC SCR	d	I_{max}	☆☆☆	☆☆☆☆☆	☆	☆	☆☆☆☆☆
Sofics HHI-SCR	e	I_{max}, V_{t1}, I_{t1}	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆	☆☆☆☆☆
Sofics Hebistor	f	I_{max}, V_{t1}, V_h	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆

Figure 1 – continued: Simplified behavior of the main ESD solution types used for protection of high voltage interfaces: (d) Basic SCR, (e) HHI-SCR, (f) Novel hebistor. The table summarizes the most relevant performance parameters for each device type: The higher the number of stars the better. The ‘flexibility’ parameter summarizes the behavior parameters that can be easily changed (‘tuned’) by changes in the device layout. The ‘Effective protection’ column depicts the ability to protect sensitive circuits. The ‘ESD/area’ and ‘ESD/leakage’ columns compare the ESD performance per area and per leakage. The latch-up immunity parameter is split up between tests according to JEDEC 78A and intrinsic transient system latch-up robustness which can be relevant for instance for IEC 61000-4-2 conformity when no board level components are applied..

II. Requirements for the high voltage ESD clamps

This section outlines the requirements for such a generic high performance ESD protection device for high voltage and power IC processes and applications. A generic solution must fulfill a number of requirements which are summarized below.

1. ESD, EOS, Latch-up

Foremost, the ESD clamp needs to protect the chip circuitry. This can be an entire power domain (supply pin protection) or a single input, output or IO circuit (IO pin protection).

Transmission Line Pulse ('TLP') testers are standard systems to characterize the ESD relevant performance parameters of the protection clamps. Example TLP curves are depicted on Figure 2 for a Zener diode, HV-PMOS and a hebistor clamp device, all produced in a 0.35um 15V technology.

Three important conclusions can be drawn:

- All clamps have a high enough holding voltage above VDD to ensure latch-up immune operation
- The operation regime of the Zener is above the maximum allowed voltage ('Vmax') leading to destruction of the sensitive to-be-protected circuits, hence rendering the clamp ineffective
- The PMOS device has an ineffective operation region above 0.8 Ampere which means that the clamp size has to be increased if more than 1kV HBM with a minimum safety margin is required.

ESD devices are routinely characterized with TLP to determine the optimal design. There are however 2 main problems with TLP measurements that are relevant for this discussion:

- The TLP characteristic is based on averaged values of voltage and current versus time waveforms, hence the TLP curve hides relevant information about the time dependent behavior
- The TLP pulse width is typically limited to 100ns; that is enough for ESD relevant analysis but it is not relevant for EOS (electrical overstress) which has a much longer timeframe.

Therefore, in addition to standard TLP analysis, it is important for high voltage applications to look carefully into the full waveform information and to include longer pulse durations in the evaluation. This is evident from Figure 3: the voltage versus time waveform of the Basic HV SCR shows that the device has an operating regime well above Vdd for the first 100ns (TLP time domain – highlighted by the rectangle). However the operating voltage drastically decreases below the Vdd voltage for longer pulses. This means that latch-up issues may occur when this device is used as ESD protection clamp under transient latch-up situations like some EOS and IEC 61000-4-2 stress situations. To compare, the novel hebistor device (Figure 3, right side) exhibits the desired behavior under long stress pulses. The clamping voltage stays above the supply level.

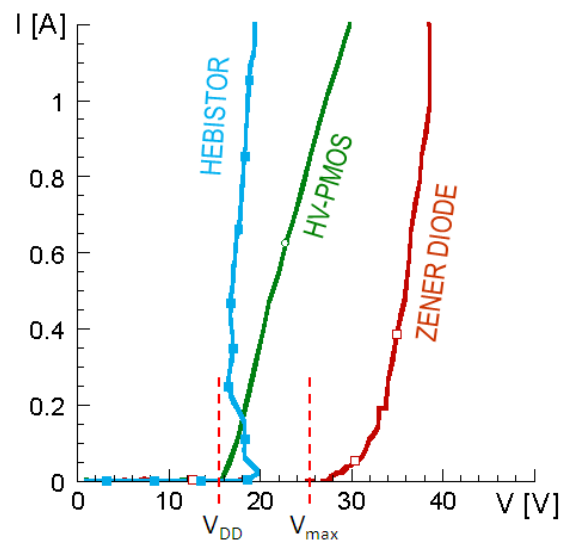


Figure 2: Transmission Line Pulse ('TLP') IV curves for 3 device types measured on 0.35um 15V CMOS technology: Zener diode, HV-PMOS and the novel Hebistor. The 3 devices are latch-up immune thanks to their high transient current operating regime above the supply voltage. The hebistor is the most effective clamp to absorb ESD stress.

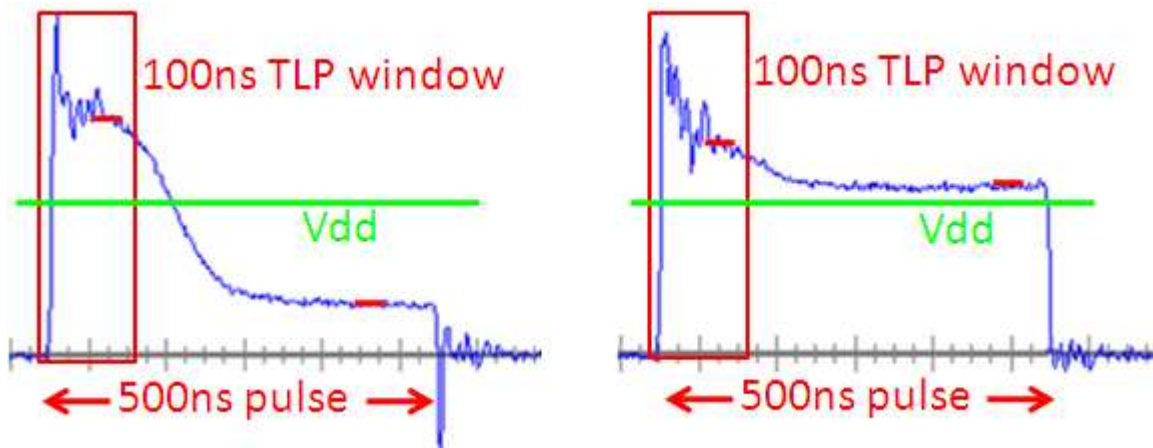


Figure 3: Voltage versus time waveform characterization of a basic high voltage SCR device (left side) and the novel hebistor (right side) in 0.35um 15V CMOS. The voltage waveforms are measured with a TLP like setup with solid state pulse generators with a much longer pulse width (500ns instead of the TLP standard 100ns duration). Within the 100ns TLP window the measured holding voltage is high enough for both devices. However for the Basic SCR device, the voltage drops drastically below the supply level after 250ns... which can lead to latch-up. The hebistor on the other hand shows a voltage level above the supply voltage for the entire pulse width ensures latch-up immunity.

2. Normal functional operation

Furthermore, the behavior of the ESD protection clamps under normal or functional operation conditions and at elevated temperature are also important. Traditional clamps like ggNMOS, Zener and PMOS devices exhibit a high leakage current which e.g. burdens the user experience for mobile applications.

This is where the novel hebistor presents a big difference compared to the traditional latch-up immune solutions: Thanks to a powerful clamp body device the required active junction area remains small. The small junction area directly translated in to excellent performance for the 'ESD performance per area' (ESD/area) and 'ESD performance per leakage' (ESD/leakage) as evident from the overview table on Figure 1. The leakage for a 4kV HBM device for instance is in the order of 10nA for the 40V clamp in TSMC 0.25um 40V at room temperature. At 125 degrees C it remains low at about 150ns. Without special process tweaking this is an order of magnitude lower compared to the other devices. Furthermore the capacitance is only about 250fF which means that the hebistor can be used for accurate capacitance sensing MEMS circuits or for the protection of sensitive HV output drivers. The small area overhead makes the hebistor the most cost-effective approach.

On-chip ESD protection for high voltage interfaces must fulfill many requirements. Current solutions cannot provide a low leakage, cost-effective and latch-up immune ESD protection clamp that is needed for the growing set of high voltage applications. Sofics hebistor devices which provide the solution will be discussed in the next Section.

III. Hebistors: novel ESD clamps for high voltage applications

Sofics has developed a family of novel ESD clamps that fulfill all requirements for protection of high voltage interfaces. This section provides measurement results from TSMC 0.35um 15V and TSMC 0.25um 40V hebistors that support these claims.

1. TSMC 0.35um 15V

The TLP curve for the hebistor device in 0.35um 15V CMOS is compared to the Zener diode and HVP MOS clamps on Figure 2. The measurement with long pulse duration depicted on Figure 3 (right side) shows that the holding voltage remains above the supply voltage. Further beyond-the-standard transient latch-up stress tests clearly show that the hebistor is guaranteed latch-up free.

2. TSMC 0.25um 40V

The TLP characteristics of two hebistor clamps in TSMC 0.25um 40V are depicted on Figure 4. In both cases, the holding voltage is above the Vdd potential while the Vt1 transient trigger voltage is below the maximum voltage ensuring an effective protection. Because the Vt1 trigger voltage and Vh holding voltage can be tuned independently the hebistor device can be used for many different applications and interfaces including IO and supply protection.

Because many high voltage applications require reliable operation at elevated temperature conditions TLP and latch-up tests were performed at 125 degrees C. The difference with results on 25 degrees C is minimal as is evident from the two measurements on the hebistor with 20V holding voltage on Figure 5.

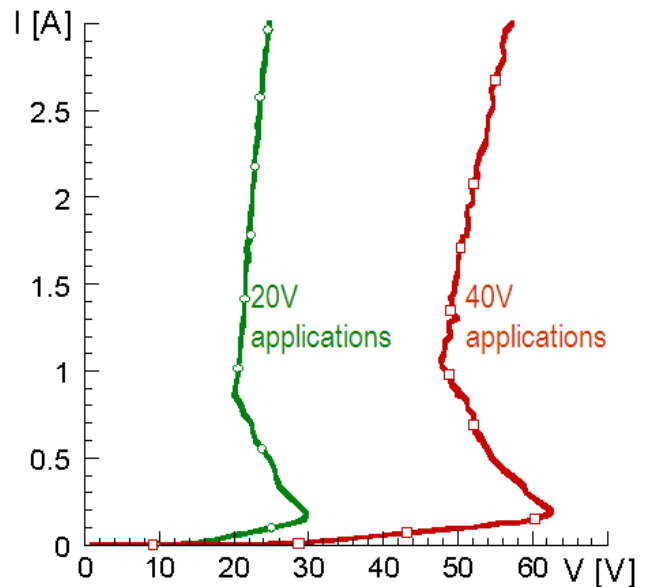


Figure 4: TLP IV curves for 2 variations of the hebistor device processed at TSMC 0.25um 40V technology. One device has a holding voltage tuned to 20V while the second is tuned to 40V holding voltage. The initial behavior before reaching the Vt1 trigger voltage is related to the transient trigger mechanism used to turn-on the hebistor clamp during ESD stress. The DC leakage current of the hebistors is below 10nA at room temperature and less than 150nA at 125 degrees C.

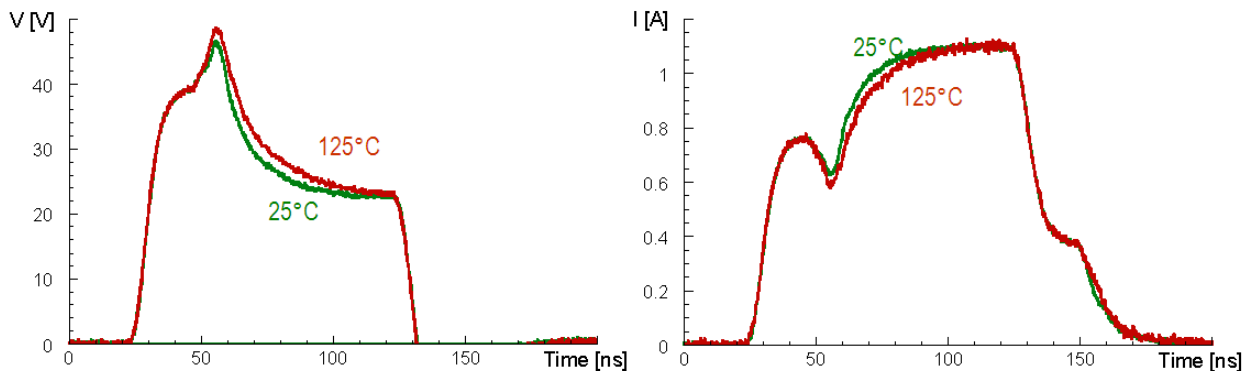


Figure 5: Voltage and current versus time measurements for the 20V hebistor variation measured at both room temperature and at 125 degrees C. The behavior at different temperatures is identical. The initial peak at the voltage waveform is not real (an artifact) related to the specific TLP system approach where incident and reflected waveforms are overlapping to simplify software and calibration procedures (the under shoot (data points below 0V) is not shown in the graph).

The robustness level scaling to any HBM level was verified by extensive silicon testing.

Besides TLP IV measurements extensive waveform analysis was performed (Figure 6) to investigate the holding voltage. Clearly the holding voltage does not drop below the supply voltage even under longer pulse durations. Finally, the hebistor behavior was also checked with transient latch-up approaches.

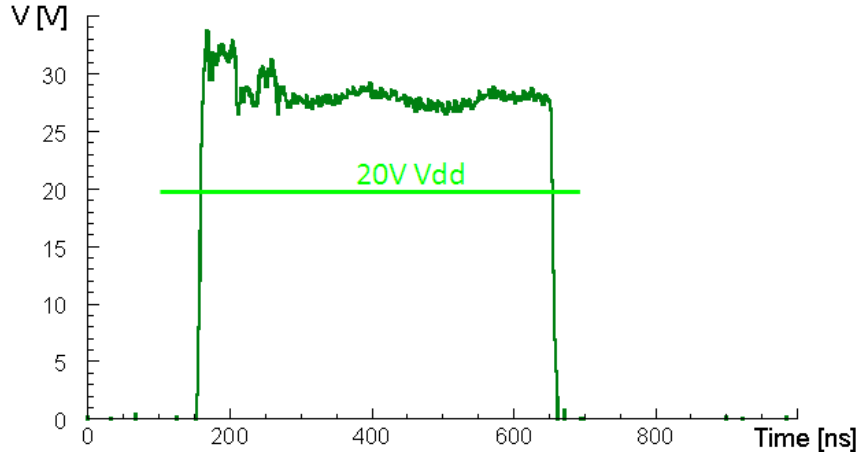


Figure 6: Voltage versus time waveform measurement on the hebistor device for 20V applications. Even during long duration pulse stress (500ns) the holding voltage never drops below the supply voltage which guarantees absolute latch-up immunity.

To check for hidden degradation effects, the final hebistor clamps have been stressed multiple times at a level of 80% of the I_{t2} failure current. No degradation effects were found even after 1,000 stress pulses.

The PowerQubic hebistor portfolio contains different variations such that the trigger voltage and holding voltage can be tuned. This ensures that various application types and IO circuits can be protected with the same generic approach. Figure 7 demonstrates that the holding voltage can be tuned to a broad set of values through the use of different clamp body types combined with tuning control circuits.

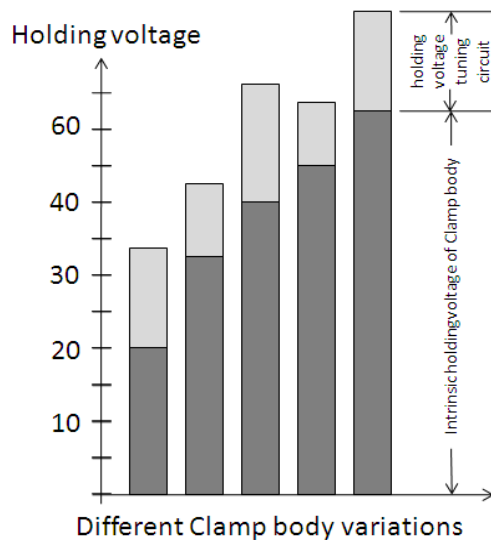


Figure 7: Overview of holding voltage tuning of the hebistor clamp in the TSMC 0.25um 40V technology. The holding voltage of the different clamp body types can be further adapted through the use of holding voltage control circuits. Clearly, in the TSMC 0.25um 40V technology, a broad set of applications between 20V and 60V can be covered with the same generic approach.

Conclusion

While IC designers worldwide continue to produce very creative systems and applications based on HVCMOS or BCD technology nodes the ESD protection clamps have almost not evolved: the industry is still using large area, highly leaky clamps that typically require extensive process tuning and time consuming trial and error experiments and analysis.

Time has come to change that: Sofics' PowerQubic portfolio with the novel hebistor protection clamps provides effective protection for various HV circuits like motor control, power management and conversion, LCD panel drivers and automotive systems without the disadvantages of the traditional solution types. This paper introduced the newly developed hebistor protection device and compared it to the traditional approaches, based on extensive development and silicon verification on TSMC 0.35um 15V and TSMC 0.25um 40V high voltage process technology.

The PowerQubic hebistor devices are latch-up immune for the various industry standard requirements including transient latch-up, long pulse durations and high temperature conditions.

Within an area of 35.000um², the hebistors with holding voltage above 40V achieve more than 4kV HBM while the leakage (<10nA) and capacitance (<250fF) stay well below typical requirements. The ESD protection levels can be scaled to any level while the ESD behavior can easily be tuned (Vt1, Vh, Vmax).

Sofics' hebistor clamps are already available today on TSMC 0.35um 15V, TSMC 0.25um 40V and are being ported to other proprietary technology nodes of IDM companies for the protection of power management ICs.

Sofics team is highly experienced in technology transfer through which PowerQubic hebistor solutions can be customized and transferred to any proprietary (foundry or IDM) silicon process technology.

Contact information

Sofics (www.sofics.com; formerly known as Sarnoff Europe and now independent from Sarnoff Corporation) develops, supports and licenses on-chip ESD design solutions for nano, standard and HV processes. Sofics is a TSMC Design Center Alliance (DCA) and UMC IP Alliance partner, and also collaborates with Tower Semiconductor for advanced ESD foundry solutions. Sofics also proudly partners with the IC design house ICsense (www.icsense.com).



TakeCharge and PowerQubic solutions complement the public, foundry or customer owned protection solutions and are created to provide technical and economic advantages.

Sofics ESD solutions are product proven in 0.5um to 40nm low voltage processes, and are used today in more than 600 ICs in high volume production across many proprietary fabs and foundries like TSMC, UMC and Chartered.

TakeCharge ESD solutions are applied for a broad set of applications (including HDMI, USB 3.0, SATA, SerDes, RFID, LNA ...) and enable requirements including 8kV HBM and IEC 61000-4-2. A complete list of GDSII cells is available on ChipEstimate at www.ChipEstimate.com.

Hebistor, PowerQubic, TakeCharge, and Sofics are trademarks of Sofics BVBA

Groendreef 31 (tel) +32-9-21-68-341
B-9880 Aalter, Belgium (fax) +32-9-37-46-846
RPR 0472.687.037 bd@sofics.com

Note

As is the case with many published ESD design solutions, the techniques and protection solutions described in this white paper, including hebistors, are protected by patents and patents pending and cannot be copied freely.