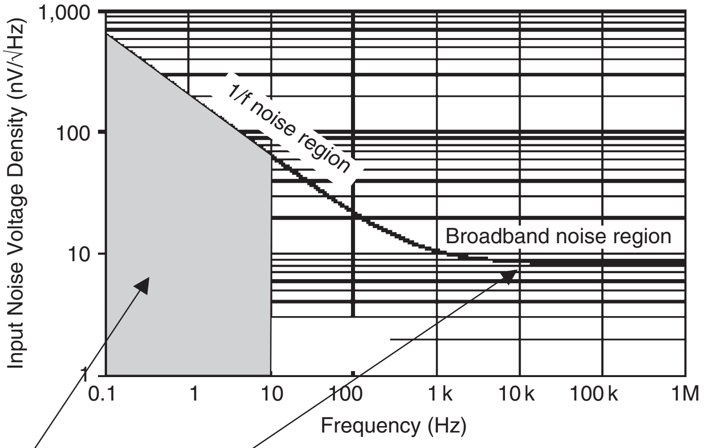
Operational Amplifiers

It is important to understand the noise that operational amplifiers create, because almost every analog circuit will have an op-amp somewhere in the circuit. The op-amp noise behavior, over frequency, has a signature that is unmistakable.

If you look for the amplifier noise specification in the typical amplifier datasheet, you will notice that it is a “referred-to-input” specification. The location of this noise source is at the noninverting input of the amplifier. In the specification table, you will typically find input noise and input noise density specifications. The input noise specification will describe the low-frequency noise of the amplifier in terms of bandwidth. You will find this bandwidth in the “conditions” column. 1/f noise is this lower-frequency noise. This is mainly because this part of the curve actually follows the ratio of 1:frequency times a multiple. The transistors in the input stage of the amplifier generate the noise through this frequency band. This is primarily the differential input stage, but it also includes the input stage load transistors.

Input noise density calls out a noise figure that refers to one frequency. For instance, the noise specifications in **Figure 8-9** identify the input voltage noise density at 10 kHz to equal 8.7 nV/√Hz. You measure the input voltage noise density at the specified frequency across a 1 Hz bandwidth. Usually this specification appears in the broadband noise portion of the frequency plot (Figure 8-9). Theoretically, this broadband noise is flat. Assuming that it is



Noise:						
Input Voltage Noise	E_n	—	2.9	—	μVp-p	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_n	—	8.7	—	nV/√Hz	f = 10 kHz

Figure 8-9: This is a representation of the noise of an example amplifier. The specifications for the noise performance of the amplifier are in tabular form at the bottom of the figure. These specifications numerically refer to the input noise voltage density versus frequency plot.

flat is a good estimate of the amplifier's behavior. It is also the foundation or baseline of the 1/f noise portion of the curve. The diffused resistors inside the operational amplifier primarily generate the broadband noise. These resistors can be diffused resistors or the source or drain of the transistors in the amplifier.

Further, on in the amplifier datasheet you will find a typical specification graph that will show you the input noise voltage density vs. frequency. Figure 8-9 shows an example of this type of graph. In this example, the input voltage noise specification is equal to the area beneath the input-voltage, noise-density curve between the specified frequencies of 0.1 Hz to 10 Hz. Note that in the table the units for this specification are peak-to-peak. To convert this to an rms value, simply divide the value by 6.6 (industry standard crest factor = 3.3).

You can easily calculate the noise underneath the curve for different input voltage noise bandwidths in the 1/f region. The first order of business in this calculation is to determine the input noise density at 1 Hz. Once you find that value, this simple formula will provide the rms noise under the curve:

$$V_{(1/f)\,:\,f_2-f_1} = B\sqrt{\ln(f_2/f_1)} \qquad [8\text{-}5]$$

where *B* is equal to the input noise density at 1 Hz. As an example, the amount of rms noise produced by the amplifier shown in Figure 8-9 from 0.1 Hz to 1000 Hz is equal to:

$$\begin{aligned} V_{(1/f)\,:\,f_2-f_1} &= B\sqrt{\ln(f_2/f_1)} \\ V_{(1/f)\,:\,f_2-f_1} &= 200\,\text{nV} \times \sqrt{\ln(1000/0.1)} \qquad [8\text{-}6] \\ V_{(1/f)\,:\,f_2-f_1} &= 607\,\text{nVrms or } 4\,\mu\text{Vp-p} \end{aligned}$$

When you think about noise at these low frequencies you may jump to the conclusion that you should take this formula down to a very low frequency, such as 0.0001 Hz (0.0001 Hz = 1 cycle per 2.8 hours). Be careful when you look at frequencies lower than 0.1 Hz, which is one cycle every 10 seconds. At lower frequencies, it is very possible that other things are changing in your circuit, such as temperature, aging, or component life. If you think of this realistically, low-frequency noise from your amplifier will probably not appear at this sample speed. But changes in your circuit, such as temperature or power supply voltage, could.

The amplifier table of specifications also gives the input noise density value. This specification is always at a higher frequency in the area where the input voltage noise is relatively constant. For this region of the curve, multiplying the square root of the bandwidth and the noise content is defined by multiplying the square root of the bandwidth by the noise density. For example, if the noise of the amplifier is 8.7 nV/ √Hz @ 10 kHz, the noise from the amplifier across the bandwidth of 1 kHz to 100 kHz is equal to:

$$\begin{aligned} V_{100k-1k} &= (\text{Noise Density } @10\,\text{kHz}) \times \sqrt{\text{BW}} \\ V_{100k-1k} &= (8.7\,\text{nV}/\sqrt{\text{Hz}}) \times \sqrt{(100{,}000 - 1{,}000)} \\ V_{100k-1k} &= 2.74\,\mu\text{V rms or } 18.1\,\mu\text{Vp-p} \end{aligned} \qquad [8\text{-}7]$$

Where BW is equal to the bandwidth of interest.

The challenge from the manufacture is to give you good data so you can work through the impact of their device in your application. So how do you get from the manufacture's graph to a meaningful result in your application circuit? You calculate the area beneath the noise curve and multiply that times the noise gain of the amplifier. Let's go through this process with a real circuit and real component values.

The amplifier in **Figure 8-10** is in a typical inverting gain stage. The input to the circuit is V_{IN} and the output is V_{OUT}. The voltage at V_{SS} is equal to 0 volts or ground, and the voltage at V_{DD} is equal to 5 volts. There is a 2.5 V reference connected to the noninverting input of the amplifier at the V_{REF}.

Figure 8-10 shows the internal capacitors of the amplifier. They will come into play when we start to calculate the gain of the circuit over frequency and look at the noise. C_{CM} is equivalent to the common-mode capacitance of the input stage of the amplifier. For our example, C_{CM} is equal to 6 pF. This capacitance is referenced to ground. C_{DIFF} is equivalent to the differential input capacitance of the amplifier, and you will notice that it appears between the two input terminals. For our calculations we will use $C_{DIFF} = 3\,\text{pF}$.

The parasitic capacitance of the external resistors, R_1 and R_2, are C_{P-R1} and C_{P-R2}, as shown in this diagram. Although you might think that these are insignificant capacitances (at ~0.5 pF), they are worth paying attention to. They could affect the noise gain of the amplifier circuit at higher frequencies. Figure 8-7 shows the frequency effects of this parasitic capacitance.

The noise gain calculation of this amplifier circuit uses the noise source, e_n, as an input signal. This source is graphically inside the amplifier symbol. You will notice that this formula is not the same as the formula for the signal gain.

$$\begin{aligned} \text{Signal Gain} &= V_{OUT}/V_{IN} = -Z_2/Z_1 \\ \text{Noise Gain} &= V_{OUT}/V_{IN} = 1 + Z_2/Z_1 \end{aligned} \qquad [8\text{-}8]$$

Where Z_1 is the equivalent input resistor, capacitor network, and Z_2 is the equivalent feedback resistor, capacitor network

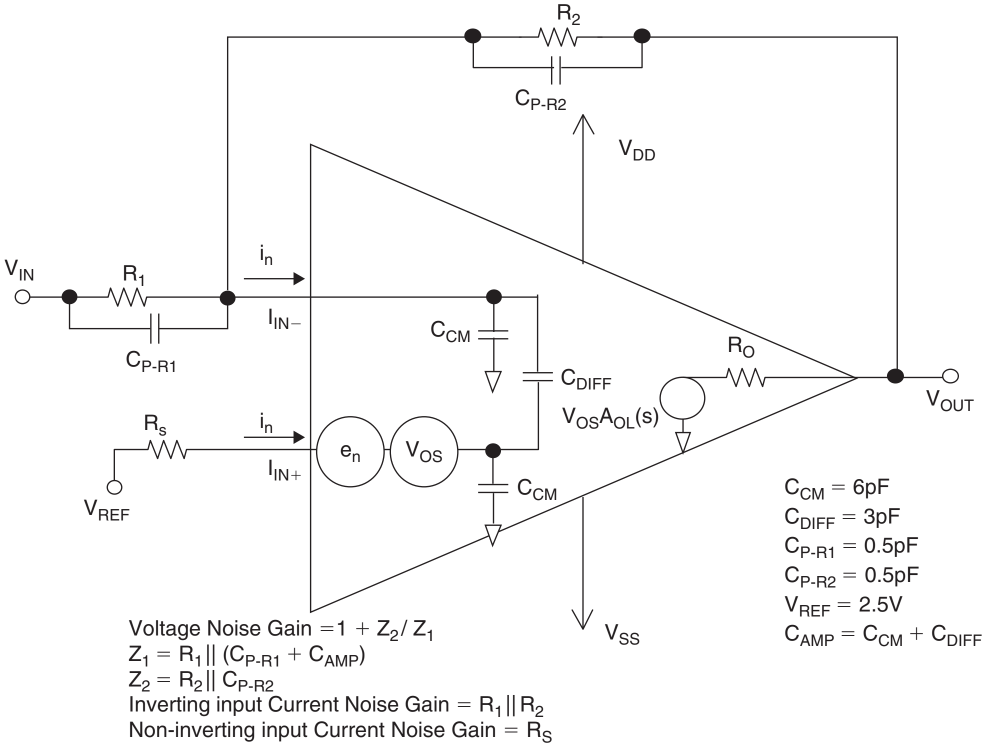
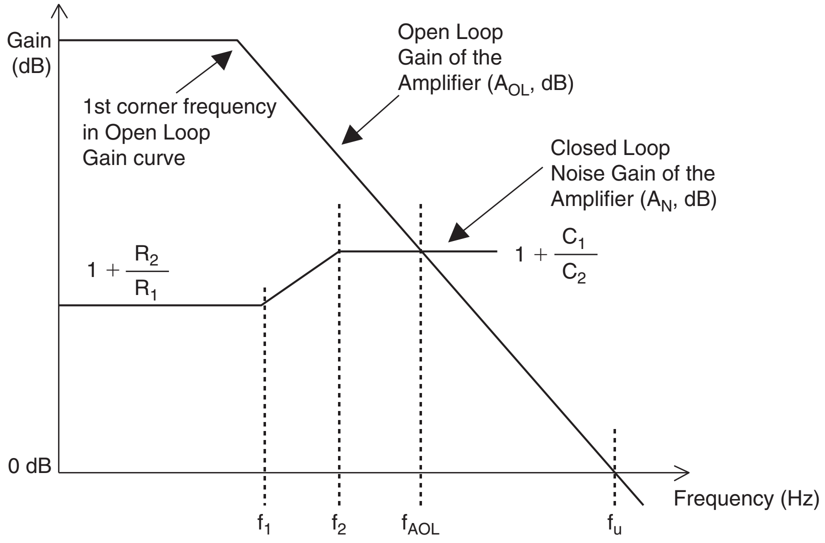


Figure 8-10: This amplifier circuit model is in an inverting gain configuration. This diagram illustrates the pertinent parasitics of the amplifier and resistors along with the calculation for noise gain.

When you are calculating the amount of noise that an amplifier produces, the noise gain equation will provide the correct results. This equation will also provide the correct closed-loop bandwidth of the amplifier circuit.

Figure 8-11 shows the frequency response of this amplifier circuit. The capacitors and resistors surrounding the amplifier, as well as the frequency response of the amplifier, affect the bandwidth of the circuit.

The DC noise gain of this circuit is dependent on the resistors in the circuit. At higher frequencies, the noise gain is dependent on the capacitors. It is possible in many circuits to design the second-corner frequency, f_2, higher than the f_{AOL} crossing. If this is the case, you can ignore the effects of f_2. If the value of R_2 is high ($>100\,k\Omega$), f_2 may come down in frequency, lower than the open-loop gain crossing. To optimize the noise and bandwidth performance of this type of amplifier circuit, the pole, f_2, should occur at or slightly before the point where the noise gain plot intersects the open-loop gain curve of the amplifier. This could require an additional capacitor in parallel with R_2.



$$f_1 = \frac{1}{2\pi(R_1 \parallel R_2)\,(C_{P\text{-}R1} + C_{AMP} + C_2 + C_{P\text{-}R2})}$$

$$f_{AOL} = \sqrt{\frac{f_u}{2\pi R_2\,(C_1 + C_{AMP})}}$$

$$f_2 = \frac{1}{2\pi(R_1 \parallel R_2)\,(C_2 + CR_2)}$$

Figure 8-11: The open-loop gain curve of the amplifier is on top of the closed-loop gain curve of an amplifier circuit. With the open-loop amplifier gain curve (A_{OL}), the first corner frequency follows the DC gain. Past this first pole, the gain of the amplifier attenuates at a rate of −20 dB/decade. With the closed-loop noise gain curve (A_N), the poles and zeros of the transfer function are shown along with their corner frequencies. The bandwidth of the noise gain is equal to f_{AOL}.

Once you calculate the gain across the frequency spectrum of the amplifier's bandwidth in this circuit, you can start to determine the circuit's referred-to-output noise. **Figure 8-12** separates the noise into six parts. Five of these noise parts are in the graph, and the sixth is part of the formula in the figure.

In region e_1, the 1/*f* noise of the amplifier is gained by the DC gain of the amplifier circuit. The specifications for amplifier noise are in nanovolts per root hertz. So the analysis is complete when you multiply the average noise over the region by the square root of the bandwidth of that region. For CMOS amplifiers, the 1/*f* region is usually from 0.1 Hz to 100 Hz up to 1000 Hz. Since this noise value is multiplied by the square root of the bandwidth, its contribution is low.

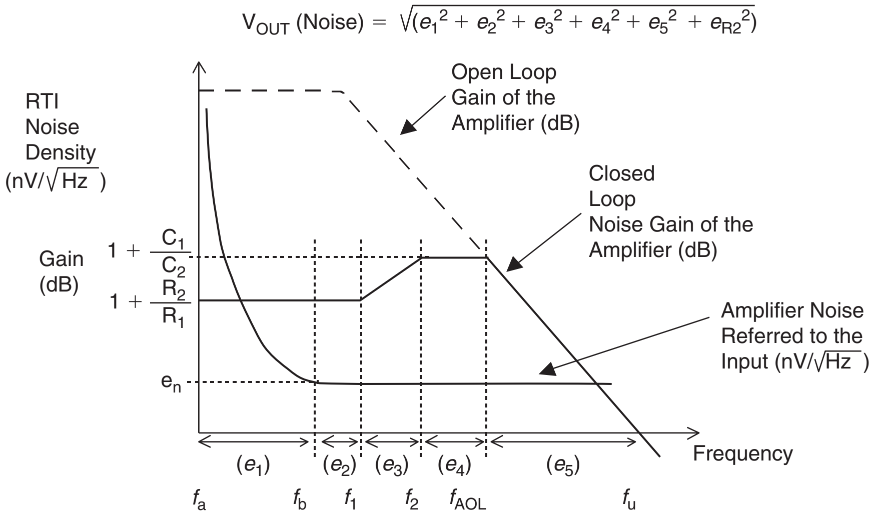


Figure 8-12: The noise of the amplifier is referred to the input of the device because the manufacturer doesn't know which configuration you are going to put your op-amp into. With the referred-to-input values you can calculate your own referred-to-output values, which you can use moving forward in the rest of your circuit.

In the second region, the broadband noise of the amplifier is multiplied by the DC noise gain. Again, the average noise is multiplied by the square root of the bandwidth of that region. The contribution of noise in this region is also relatively low.

The third, fourth, and fifth regions are calculated in the same manner, with each region contributing more to the overall noise of the circuit. The sixth part of the noise equation in Figure 8-12 represents the noise contribution of the feedback resistor, R_2. The noise contribution of this resistor might or might not be significant, depending on the magnitude of the resistor. This calculation will quickly demonstrate where the highest noise contribution is coming from and make it easier to refine the design.

Region e_1:

$$e_1 = (1 + R_2/R_1) \times B\sqrt{(\ln(f_b/f_a))} \tag{8-9}$$

Region e_2:

$$e_2 = (1 + R_2/R_1) \times e_n \times \sqrt{(f_2 - f_1)} \tag{8-10}$$

Region e_3:

$$e_3 = (1 + R_2/R_1) \times e_n \times (1\,\text{Hz}/f_1)\sqrt{(f_2/3 - f_1/3)} \tag{8-11}$$

Region e_4:

$$e_4 = (1 + C_1/C_2) \times e_n \times \sqrt{(f_{AOL} - f_2)} \tag{8-12}$$

Region e_5:

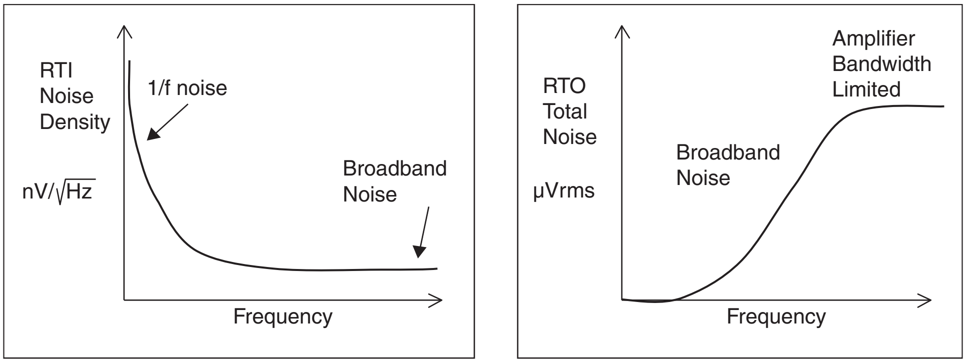
$$e_5 = (1 + C_1 / C_2) \times e_n \times \sqrt{(\pi / 2(f_u - f_{AOL}))} \qquad [8\text{-}13]$$

Region e_{R2}:

$$e_{R2} = \sqrt{(4 \times K \times T \times R_2 \times (BW))} \qquad [8\text{-}14]$$

Note: In this calculation, C_1 *is the parallel combination of the input capacitors, or* $C_{P\text{-}R1} \| 2C_{CM} \| C_{DIFF}$. C_2 *is the feedback capacitor or* C_{P-R2}.

All this being said, SPICE is a useful tool as you verify your noise calculations. The two graphs in Figure 8-13 demonstrate how SPICE can help you understand the noise in your circuit. The graph on the left (**Figure 8-13a**) shows the simulated noise as frequency increases. You will notice that the noise is very low at the lower frequencies. This is because the lower bandwidths are multiplied by the square root of a small number, the bandwidth. As frequency increases, the cumulative noise also increases. You would think that at higher frequencies the increases in noise would be less due to the characteristics of the left-hand graph (Figure 8-13a). As you can see, though, this is not true. The reason is that the bandwidth multiplier (square root of the bandwidth) is larger at higher frequencies.



(a) (b)

The area under the RTI plot of a frequency region is multiplied by the square root of that bandwidth and closed loop gain to calculate the RTO plot

Figure 8-13: Amplifier noise can be graphically represented as though the noise source is at the input of the amplifier (a), otherwise known as *referred-to-input (RTI)*, or as though it is at the output of the amplifier (b), otherwise known as *referred-to-output (RTO)*.

Going back to Figures 8-3 and 8-8, we concluded that reducing the resistor values was beneficial to a point. The next step is to reduce the amplifier noise. If the resistors are reduced ten times and the amplifiers are changed, the noise code width response in Figure 8-4 is reduced from 44 to 21 codes, p-p. This is not bad, considering we haven't changed the layout, just the devices.

A/D Converter Noise

The most talked-about noise from the A/D converter is *quantization noise*, which is the noise that an A/D converter generates as a consequence of dividing the input signal into discrete "buckets." **Figure 8-14** illustrates this concept. The width of these "buckets" is equal to the LSB size of the converter. The quantization noise of a converter determines the maximum Signal-to-Noise Ratio ($\text{SNR}_{\text{IDEAL}} = 6.02\,n + 1.76\,\text{dB}$). This noise is immediately apparent in the converted signal. If you want more accuracy, you need to change to a converter with a higher number of bits. Just as a caveat: Making this change does not guarantee a better SNR, because the converter might have other noise sources inside, but it is a good start.

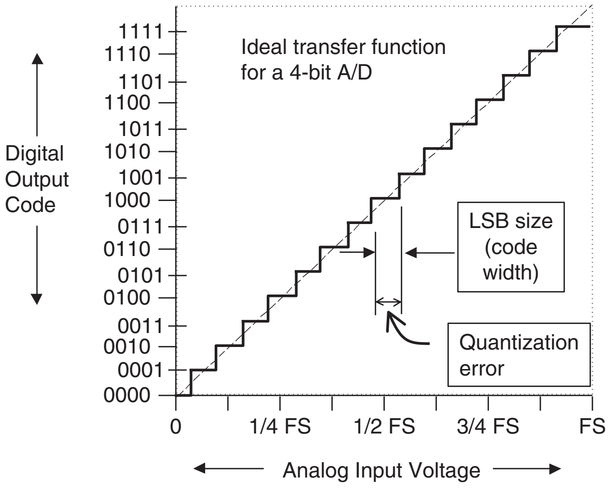


Figure 8-14: The A/D converter does not convert the analog signal to an ideal value. The A/D converter has a discrete number of output conditions and the analog signal has an infinite number of voltage states. This is called the *quantization error*, which accounts for quantization noise.

There is also noise inside the A/D converter that comes from the internal transistors. This type of noise is discussed in Chapter 13 in more detail, in the section "AC Specifications Imply Repeatability." Just to preview the discussion in Chapter 13, AC domain specifications, such as Signal-to-Noise Ratio (SNR), Effective Resolution (ER), Signal-to-(Noise + Distortion) (SINAD), or Effective Number of Bits (ENOB) help you