

Can MIPI and MDDI Co-Exist?

Since MIPI and MDDI standards both target interfaces to cameras and displays on mobile devices, are two separate standards really needed?

The accelerating use of smartphones and the emergence of an exciting class of mobile Internet devices (MIDs) and Netbooks are creating an explosion of data transfer across wireless networks. Such full-featured devices give the consumer a multimedia viewing and listening experience, higher-resolution photography, and a richer set of applications like Web browsing and Global Positioning System (GPS) navigation. Cell-phone manufacturers and the chip providers that supply them need to decide which interface bus to use to support the required low-power, high-speed data transfer between the components that make up these new devices. The Video Electronics Standards Association's (VESA's) Mobile Display Digital Interface (MDDI) and the Mobile Industry Processor Interface Alliance's (MIPI's) display and camera interfaces provide overlapping standards to meet these requirements. Each standard is a reflection of its origin and the industry participants driving it. This article will explore the different aspects of MDDI and MIPI to help designers determine whether they need to support both of them in their next chip or system design.

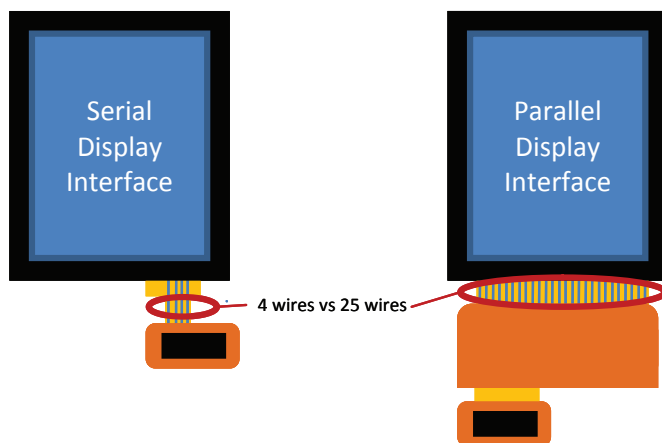


Figure 1: Here is an example of a serial versus parallel display interface. Fewer serial wires simplify routing.

Parallel interfaces are less attractive for mobile devices now because of pin count, electromagnetic-interference (EMI) radiation, signal-integrity concerns at higher bus speeds, and higher power-consumption profiles. Large parallel-bus harnesses aren't suited for connecting across hinged products like slider, swivel, or clamshell-type devices (see Figure 1). In

addition, parallel buses add complexity to routing on the small printed-circuit-board (PCB) footprints in mobile devices.

The need for serial interfaces began with the need to address the shortcomings of legacy parallel-bus connections. To solve these issues, companies jumped in to provide proprietary interfaces. For example, Texas Instruments introduced the FlatLink3G serializers and deserializers to provide a high-speed interface between liquid-crystal-displays (LCDs) and mobile application processors, such as its OMAP platform. These sub-low-voltage-differential-signaling (sub-LVDS) serializers work for red/green/blue (RGB) color data. They support screen resolutions from QVGA through XGA including VGA. QUALCOMM entered the fray as well with MDDI. A key aspect of these interfaces was that the transmitter side could be integrated into the baseband application processor and the receiver side in the display. A number of other companies also introduced proprietary solutions, bringing more choice and confusion.

With so many different choices, the systems integrator was faced with how to interconnect the components from different manufacturers. This was a perfect opportunity for the creation of an interface standard (or two). Under the leadership of QUALCOMM, VESA created a special interest group (SIG) to work on standardizing MDDI in April 2002. At that time, VESA had more than 150 members. MIPI was formed shortly after that, when an initial agreement to standardize on interfaces between TI and STMicroelectronics was expanded to include ARM and Nokia. MIPI developed a broad charter, moving beyond just rationalizing the interfaces of the platforms of OMAP (from TI) and Nomadik (from STMicroelectronics) processors. Intel and Motorola later joined as board members and the organization set about defining a number of different standards that could be shared among chip suppliers and systems OEMs. At present, MIPI's members have grown beyond 100 as well.

QUALCOMM's work on MDDI brought a silicon-proven interface to VESA. This early start allowed MDDI to get a solid headstart as a practical standard in use today. California Micro Devices, Epson, QuickLogic, Samsung, Toshiba, and others have developed chips using the MDDI standards—

some of which are shipping in volume. In VESA, work has continued on MDDI. In July of this past year, Version 1.2 of the MDDI standard was released. The new version of MDDI, which will be available in QuickLogic's ArcticLink II VX4C Customer Specific Standard Product (CSSP) platform later this year, provides support for audio transducers, keyboards, pointing devices, and other input devices integrated with a mobile display for up to 1-Gbps operation. Some other MDDI features include:

- Full-motion video in the form of full-screen or partial-screen bitmap fields or compressed video, depending on device capability
- Static bitmaps at low rates to conserve power and reduce implementation cost in some portable devices
- PCM or compressed audio data at any resolution or rate compatible with the serial-link speed
- Pointing-device position and selection
- Control and status information in both directions to detect the capability of the opposing device and set its operating parameters
- User-definable data types for capabilities yet to be defined
- Windowless video-stream packet with no X/Y windowing information
- Flexible video-stream packets to allow for the selective inclusion of a video-stream packet

The serial-link speed on each signal pair of the MDDI specification can vary over many orders of magnitude. As a result, the system designer can easily optimize cost, power, implementation complexity, and the update rate across many different cell-phone components. The added attributes of MDDI 1.2 now completely overlap some of MIPI's standards. So what is the state of these MIPI standards today?

After its founding, the MIPI Alliance went right to work converting legacy parallel display and camera interfaces to new serial standards. The standards, called Display Serial Interface (DSI) and Camera Serial Interface (CSI), both use the same common physical standard called the D-PHY. The D-PHY also is the physical-layer (PHY) standard for a universal protocol dubbed UniPro, which is currently being defined. In addition to the D-PHY, which uses source synchronous clocking with differential transceivers, the MIPI organization is defining an M-PHY. This low-power, higher-speed serialized transceiver has an embedded clock. The M-PHY has recently been targeted to act as the interface between the baseband and RF sections of the DigRF

standard—another standard that's now part of the MIPI Alliance. The high-speed roadmap for DSI and CSI includes use of the M-PHY. Figure 2 illustrates the MIPI Alliance vision of plug-and-play PHYs for different protocols.

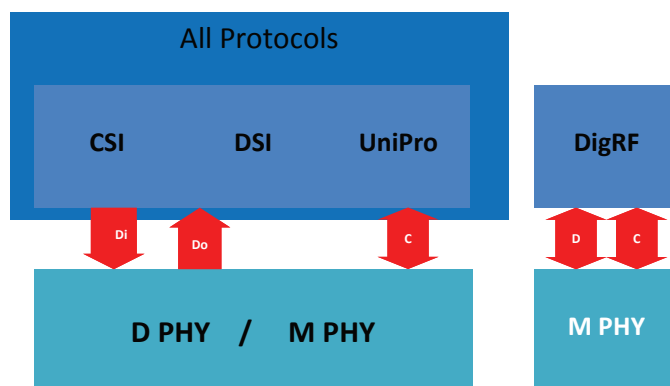


Figure 2: MIPI's D-PHY and M-PHY work as the physical layer of CSI, DSI, and UniPro. The M-PHY is the physical layer for the new DigRF standard.

The MIPI Alliance is organized into working groups focusing on display, camera, PHYs, and other standards. MIPI looks at software issues as well. It has working groups for test and debug. One of the major differences between MIPI and MDDI is the structure and workings of the groups that are defining and controlling the specifications. MDDI is a single specification. QUALCOMM is a major force in its definition and its use model. In fact, many still see MDDI as a QUALCOMM specification even though it has moved into VESA.

In contrast, MIPI has the look and feel of an IEEE standards group. In fact, IEEE-ISTO is the managing organization for MIPI. MIPI organized into multiple working groups with company voting rights based on attendance in addition to the contributor fee that must be paid to join. The specifications are comprehensive within the discipline of each working group. So the MIPI and MDDI standards both exist in the market and target interfaces to cameras and displays on mobile devices. Are these two standards necessary? Should they coexist? A closer look at market dynamics will provide the best answer.

Cellular has had two main competing network technologies: Global System for Mobile Communications (GSM) and Code Division Multiple Access (CDMA). Both of them are referred to as second-generation (2G) standards. The GSM Association is an international organization founded in 1987 that's dedicated to providing, developing, and overseeing the worldwide wireless standard of GSM, which is used more outside the United States. CDMA, a proprietary standard designed by QUALCOMM, has been the dominant network standard for North America, Korea, and South America.

In the U.S. today, AT&T-Wireless and T-Mobile use GSM while Sprint and Verizon use CDMA. Subscriber usage favors GSM because it is in use in 74% of the cellular markets worldwide. However, the lucrative American markets and the acceleration of CDMA usage in China and India put the market share of CDMA at 14% by 2013 (ABI Research). Both of these standards have evolved over time from 2G to 3G to 3.5G, thereby providing higher data rates. Specifically, GSM has evolved to Wideband CDMA (WCDMA) and then HSxPA technology while CDMA has evolved to CDMA2000 1X EV-DO Rev A to Rev B. Eventually, both camps seem to be converging to a shared Long Term Evolution (LTE) standard.

At the same time, both networks continue to make inroads into each other's respective territories. There are camps on both sides that firmly believe one cellular standard is superior to the other. What does this mean for MDDI and MIPI? MDDI evolved in the CDMA ecosystem driven by QUALCOMM while MIPI germinated from suppliers who focused on GSM platforms. The industry has two standards with usage divided along the industry lines: MDDI for CDMA and MIPI for GSM. Outside of the historical market evolution, however, are there differences that make one of these standards better than the other? The table compares the aspects of the MIPI standards (D-PHY) with those of VESA MDDI.

MIPI D-PHY	VESA MDDI
Defined inside MIPI, a multi-member organization	Defined by QUALCOMM, then moved public in VESA
Physical layer for a number of separately defined protocols, camera, display, universal	Physical layer defined in one comprehensive specification
Multiple PHY configurations, high speed in the forward direction with low speed in reverse	One PHY architecture, high speed in the forward direction with reverse direction at half that of the high-speed direction
Up to 8 data lanes (1, 2, 4, 8 data lanes)	Link Types 1-4 (1, 2, 4, 8 data lanes)
Differential-voltage model driver - implementation preference	Differential-current model driver - implementation preference
New to the market	Longer silicon history
Typical high-speed transfer 500 to 1000 Mbps	Typical high-speed transfer variable to 1000 Mbps
Roadmap to 5 Gbps per link (M-PHY)	No defined roadmap above 1000 Mbps
Separate protocol layers by specification - Camera, Display, UniPro	One protocol document with multiple packet definitions for camera, display, etc.
GSM market focus	CDMA market focus

Table: Comparison of the physical layer of the MIPI and MDDI standards

On inspection, the table shows some differences. But do these differences provide a technical advantage that might be the catalyst for a clear winner to emerge? Although MDDI is architecturally uniform (simple), it provides a powerful frame-based protocol platform that defines multiple packet types. The basic architecture has a host and client side. The host controls the flow of traffic—nominally forward, but the high-speed reverse can reverse communication flow through the use of a reverse link encapsulation packet.

The physical connection between the host and client comes in four different types. Type 1 is a six-wire interface with data and strobe each as a two-wire differential connection and an optional power and ground. The clock—driven from the host side—is distributed between the data and strobe. Types 2-4 use additional differential data connections sending 2, 4, and 8 bits, respectively, in parallel. The MDDI architecture is shown in Figure 3.

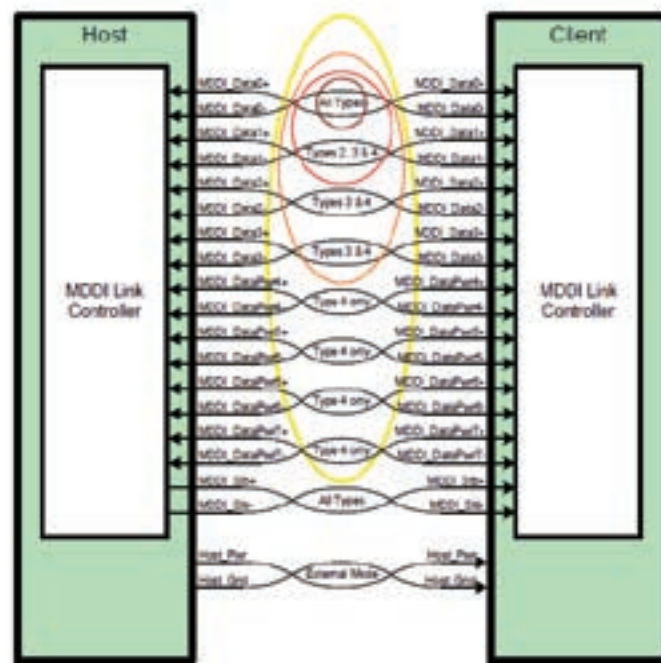


Figure 3: In the MDDI architecture, Types 1 to 4 vary the number of data connections to 2, 4, and 8 bits.

The MDDI's uniform architecture and specification requirements lend it to the use of differential current-mode drivers. The current-mode architecture provides mask eye clarity across all types and in all speed ranges. Although nominally consuming more power, the host can dynamically scale the operating speed from 1 kbps to 1 Gbps as required by battery/AC power constraints and other system operating conditions.

MIPI's Camera Serial Interface (CSI) and Display Serial Interface (DSI) both use the MIPI-defined D-PHY

architecture for their PHY layer. That architecture supports uni- or bi-directional data flow as part of the configuration options that are outlined in the specification as shown in Figure 4. The D-PHY's architecture requirements make them well suited to the implementation choice of voltage mode drivers, which offer power savings. Interestingly, both MDDI and MIPI provide a form of cyclic-redundancy checking (CRC) at the PHY to detect common errors caused by noise in transmission. MIPI goes beyond MDDI in defining error-correcting code (ECC) at the protocol layer, although it's unclear whether such error recovery at the block level is required in an intimate system like that of a cell phone.

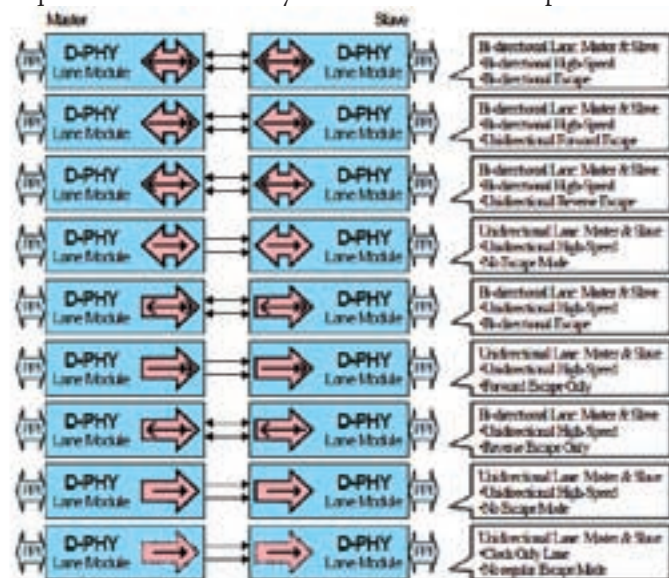


Figure 4: The MIPI D-PHY architecture shows configurations in bidirectional and unidirectional with varied escape modes.

So which interface is preferred? The common denominator in the proper choice is power and area efficiency. Here, both standards do a good job with little or no discernable difference. There are many variations of PHY architectures in MIPI. In the end, however, the voltage-mode driver preference as an implementation preference offers the best chance for optimal power savings. However, efficient implementation of the MDDI architecture leaves very little room for substantial power improvement. The true power preference will come when the new MIPI M-PHY architecture is defined and implemented.

The M-PHY will slot into either the camera or display interface without any changes to the protocol layer. The M-PHY is specified with an encoded clock and offers final speeds approaching 5 Gbps per data lane. The M-PHY also has aggressive targeted power consumption with transfer-rate goals defined at 20 mW at 5 Gbps. If that target can be reached at those speeds, it would be welcome in chips on many power-limited, data-intensive applications running on mobile

products. But the M-PHY is still a ways off, as it's just entering its final stages of specification definition in MIPI's PHY group. And the argument is easily made that today's displays and sensors don't need the extra bandwidth.

At the detailed implementation level, neither MIPI nor MDDI has a technical advantage. The market sharing between GSM and CDMA means that both of these standards will most likely coexist for some period of time. Just recently, QUALCOMM joined the MIPI Alliance—a move that shows the momentum of MIPI standards. Supporting both standards will be a requirement for display and sensor manufacturers as well as for the companies developing the platform and application processors on mobile devices.

For suppliers that have already qualified products (displays or sensors) using one type of interface, a bridge chip like that from California Micro Devices (CM5160) or a CSSP from QuickLogic (based on its ArcticLink VX II solution platform family) allows them to retarget qualified products to a different market (GSM or CDMA) or mix and match various processor and display technologies. For companies developing application processors or peripheral chips, the IP from Mixel can help them to target their new products to run either interface. Today, the choice of MDDI or MIPI is all about which market will buy the chip. Targeting products for both markets expands their selling potential. As the market moves to next-generation solutions like the M-PHY, convergence to one standard seems more likely. ♦

Ashraf Takla is President and CEO of Mixel Inc., which he founded in 1998. Before Mixel, Mr. Takla was Director of Mixed-Signal Design at Hitachi Micro Systems, and also worked at AMI and Sierra Semiconductors. Mr. Takla has 29 years of experience in analog and mixed signal design, and holds 5 patents. Mr. Takla received his BSEE & MSEE degrees from San Diego State University.



Timothy Saxe is a CTO and Senior Engineering Executive for QuickLogic Corporation. Prior to joining QuickLogic in 2001, he held senior-level engineering positions at Actel Corporation and GateField Corporation. He holds a B.S.E.E. degree from North Carolina State University, and an M.S.E.E. degree and a Ph.D. in electrical engineering from Stanford University.

