

New standards embrace the principles of boundary scan while extending its reach to complex ICs, PCBs, and systems.

MOVING BEYOND IEEE 1149.1

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FIGURE 1. Boards like this Mixed Signal I/O Module PXI 5296 that plugs into the PXI bus can turn a conventional PC into a multipurpose test instrument.

Courtesy of Goepel electronic.

When the JTAG (Joint Test Action Group) standard that became IEEE 1149.1 first emerged some two decades ago, it launched a paradigm shift in the way that electronics manufacturers looked at both control and test issues on PCBs (printed-circuit boards). In the ensuing years, additional standards (and standard proposals), as well as changes in the way that companies have applied 1149.1, have improved the usefulness of boundary scan and have widened its acceptance. At the same time, JTAG-related tools and their implementation have considerably surpassed the original intent of the standard's creators.

The evolution of boundary scan

Many in the industry regard IEEE 1149.1 to be synonymous with “boundary scan.” Yet, boundary scan predates JTAG, originating as LSSD (level-sensitive scan design), which was devel-

oped by IBM in the late 1960s. The technique provided a way to conduct functional tests on PCBs where the logic was no longer accessible from the edge connectors. But LSSD never received universal acceptance.

Peter van den Eijnden, president of JTAG Technologies, commented, “Boundary scan isn’t a solution, it’s a method. In that respect, it’s like built-in self-test [BIST]. The *concept* of BIST is pretty much universally accepted. How to accomplish it is not.” IEEE 1149.1 provided a standard structure for the method’s implementation.

CJ Clark, president and CEO of Intellitech and past IEEE 1149.1 chair, explained, “While the focus by some has been on boundary scan, the first half of 1149.1 is the Standard Test Access Port, or TAP. The TAP has provided a uniform method for accessing on-chip test resources at the component, board, and system levels. We use the TAP to give us boundary-scan capability and the ability to emulate CPUs for functional test and silicon debug, as well as the ability to perform FPGA [field-programmable gate array] programming, flash programming, on-chip and external memory BIST, logic/PLL [phase-locked loop] BIST, and even things like system-level SerDes test. Because 1149.1 is low contact, structured, and reusable at different phases of integration, it’s the only test method that can be easily embedded in the PCB and thereby give the engineer the data needed to correlate failures at these different phases.”

Much of the initial clamor for adopting boundary scan and incorporating the TAP stemmed from the disappearance of conventional bed-of-nails access to PCBs for in-circuit test. Andrew Levy, director of strategic business development for Corelis, put it this way: “Boards and systems containing BGA [ball-grid array] components and other dense packaging have

become dependent on boundary-scan-based structural testing because it provides electrical access even when physical access is either not cost-effective or not feasible at all.”

Once IEEE 1149.1 and the TAP emerged as test tools, engineers soon found other ways to use their capabilities. “Over the years, JTAG has become the standard method for performing on-board device programming,” Levy continued. “Programming flash memories, EEPROMs, CPLDs, FPGAs, and other devices after board assembly helps assure proper version control and therefore correct board function.”

Other test standards emerge

Since the inception of IEEE 1149.1, additional standards have broadened engineers’ ability to apply its principles in the real world (Table 1). IEEE 1149.4 addresses the test of analog circuits. IEEE 1149.6 covers advanced digital networks requiring high-speed interconnects. Where adding the four or five pins necessary for the TAP proves excessive—in commodity parts, for example—proposed standard P1149.7 describes a more compact version that requires only two extra pins while adding test functionality.

IEEE 1500 deals with chip-level test, aiming specifically at the current crop of systems-on-a-chip. IEEE 1532 defines unified programming commands for programmable devices (mainly CPLDs) and defines a language format for describing programming algorithms and accompanying data. Van den Eijnden commented, “Using 1532, a manufacturer can program PLDs from different vendors simultaneously, reducing the total programming time for the board.”

Proposed standard P1581 offers an economical alternative to boundary scan for memory devices by minimizing the overhead required to implement it. Proposed IEEE P1687—also known as IJTAG (Internal JTAG)—specifies a methodology for automating, accessing, and analyzing the output from embedded instrument functions on the chips themselves. There is even an ongoing effort to use the TAP capabilities at the system level, although this so-called SJTAG is only in the very earliest stages. “Besides,” van den Eijnden added, “it is quite feasible to perform system-level

boundary-scan operations using the existing structures of 1149.1 and a variety of standard off-the-shelf system-level devices such as National Semiconductor’s Scan Bridges.”

Elaborating on P1687, Al Crouch, chief technologist for core embedded instruments at ASSET InterTech and vice-chairman of the IEEE P1687 working group, observed, “The latest, and perhaps the most significant, application for JTAG is emerging now as semiconduc-

more automation with EDA tools and test tools, allow instrument providers the ability to provide descriptions and operational behavior at the instrument level and not the IC level, and allow plug-n-play operation for the engineer at the PCB or system level. What I see happening is more focus on using these IEEE standards for test and less on ad-hoc test methods.”

“The technology of JTAG has proven an efficient and cost-effective method

Table 1. IEEE standards related to boundary scan

Number	Title	Date
1149.1	Test Access Port and Boundary-Scan Architecture	1991
1149.4	Mixed-Signal Test Bus	1999
1149.6	Testing Differential and AC-Coupled Interconnections Between ICs on Circuit Boards and Systems	2003
P1149.7	Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture	Proposed
1500	Testability Method for Embedded Core-Based ICs	2005
1532	Boundary-Scan-Based In-System Configuration of Programmable Devices	2000
P1581	Static Component Interconnection Test Protocol and Architecture	Proposed
P1687	Access to Embedded Test and Debug Features Via the Test Access Port	Proposed

tor vendors and system manufacturers embed instrumentation functionality into chips. This embedded instrumentation can be defined as logic that is designed into semiconductors and which is used for design validation, test, debug, yield analysis, and other activities. The goal of the P1687 IJTAG working group is to develop a standard way of connecting, accessing, analyzing, and describing embedded instrumentation intellectual property regardless of where it comes from, such as a chip supplier, third-party provider, EDA tool, or an in-house design group.”

Intellitech’s Clark provided historical perspective: “There isn’t a new concept with IJTAG. We’ve been working with on-chip instruments for years, just with a bit more pain. What we’re doing in P1687 is standardizing on the register-access mechanisms, standardizing on the hierarchical description language that describes how to access the registers, standardizing on a procedural description language for describing the scans to the on-chip registers, and standardizing on a high-level language to describe the instrument operation using Tool Command Language. The goal is to allow

for accessing registers, functions, and memory inside today’s microprocessors,” said Levy at Corelis. “Most processors already include a TAP for CPU emulation. It is used primarily for real-time firmware debug and development as well as for device test. There are even CPU-based devices that contain a debug TAP, but the implementation doesn’t provide conventional scan-chain support to permit a true boundary-scan test and is therefore technically not 1149.1 compliant. Once the processor is installed on the board, however, the TAP pins can permit control by off-board software, thereby facilitating board-level real-time software/firmware debug.”

Levy added, “We proved that TAP-based structural and functional testing can be combined by seamlessly integrating boundary-scan and at-speed CPU functional testing into a development environment where the test engineer is not required to have embedded software-development skills and both boundary-scan and functional tests are generated automatically.”

Such applications of JTAG principles help companies cope with the realities of manufacturing in today’s environment.

“Ever-shorter life cycles and a shift from making high-mix products at low volumes to high-mix at higher volumes driven by customer calls for ‘customization’ have spurred the drive for cost-effective test solutions, as well as higher test coverage and faster programming times,” commented Raj Puri, VP of US marketing and sales for Goepel electronic.

Options for test setups

One trend driving the adoption of boundary-scan techniques is manufacturers’ search for viable alternatives to “big box” testers. Companies are seeking to control costs and maintain profit margins despite the perpetual shrinking of components and their circuit features. The cost and time necessary for constructing test fixtures along with the vanishing node access discourage reliance on conventional in-circuit test, while the rising cost of test development similarly dampens enthusiasm for comprehensive functional test. The efforts expended to test complex products are adding to development times and creating bottlenecks that threaten throughput. As manufacturing cycles continue to get shorter and pressure to cut costs continues to accelerate, even desktop instruments begin to feel like luxuries.

A migration toward multipurpose and more versatile instruments provides one solution. Tools like National Instruments’ LabView enable conventional PCs to perform a plethora of instrument functions using plug-in boards (Figure 1). Recently, system manufacturers have begun to incorporate instrument functions into the products themselves.

Glenn Woppman, president and CEO of ASSET InterTech, saw the advantages of getting his company to enter the embedded instruments arena as early as possible. “If the instrument function consists of intellectual property residing in the product itself, you can use it early on for design validation,” he said. “You can then apply that same capability during manufacturing and throughout the product life cycle for such activities as functional validation, silicon debug, and structural testing. This ability to reuse the same set of tools represents a considerable cost savings over the more traditional approach where you develop one test strategy for the manufacturing step and another one for implementation after the product ships to customers.”

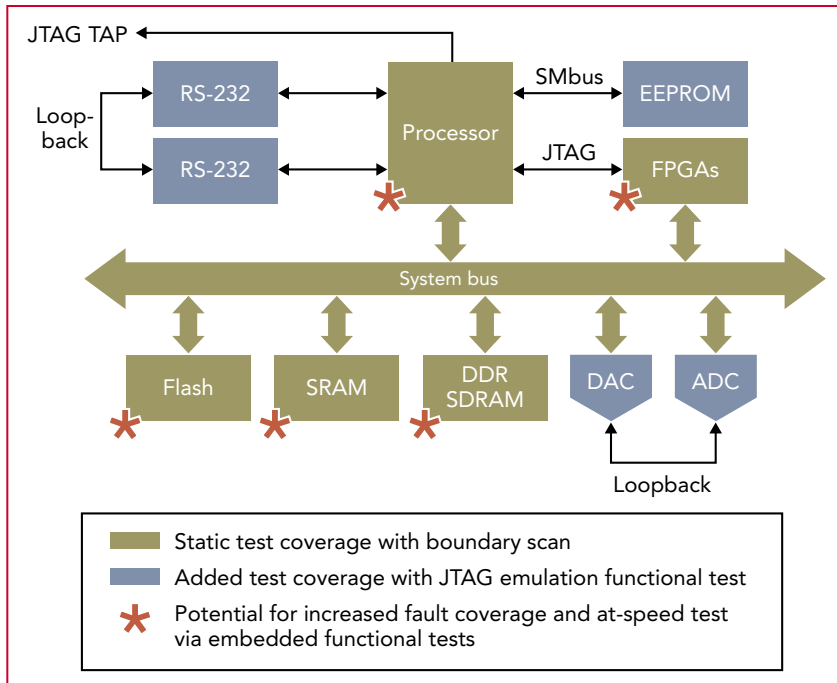


FIGURE 2. Even noncompliant microprocessors often include a TAP that can be used to emulate the function of an entire board. Courtesy of Corelis.

other one for implementation after the product ships to customers.”

Levy at Corelis commented, “In fact, test commonality means that anyone’s contributions to the product’s test or debug become intellectual property that can be used by everyone throughout the life cycle. The ability to use such tools for field repair can reduce those costs considerably, such as by reprogramming and repairing units in the field while at the same time cutting the number of faulty boards that you have to ship back to the factory for rework.”

Simon Payne, CEO of XJTAG, emphasized the advantages of interoperability and reuse from very early in the design cycle. “Suppose you have created a design and it is ready to send for layout. Ideally, you would like to accurately assess test coverage before committing to the manufacture of physical boards.

“It could prove disastrous if, say, your scan-chain circuitry is hooked up incorrectly, particularly for those who rely on the JTAG chain for debugging, testing, and programming. If you don’t discover such an error until you get the hardware back, a respin of the board may be required that—when added to long component lead times—could set your project back for months. Since software

teams generally depend on having a physical board to complete software development, that delay pushes their portion of the project time line back as well. If before the boards are manufactured you could say to the vendor, ‘the test-data-input and test-data-output lines are wrong. Can you uncross them for me?’ That simple step substantially reduces your development cycle.”

Payne continued, “By providing reusable code, tests can be developed rapidly to cover both JTAG and non-JTAG devices. That way, by the time you get the prototype back from the vendor, you have already written the tests—not only for verifying that the design is valid but [for] giving you a means to test the components installed by contract manufacturers.”

Another approach takes a page from in-circuit emulation, which in generations past exercised a microprocessor-based board by overriding or replacing the processor’s functions. Although today’s boards do not permit such indignities, boundary-scan architectures allow engineers to use the existing TAP on even noncompliant processors to provide the same level of control (Figure 2).

JTAG Technologies’ van den Eijnden put it this way: “If microprocessors and

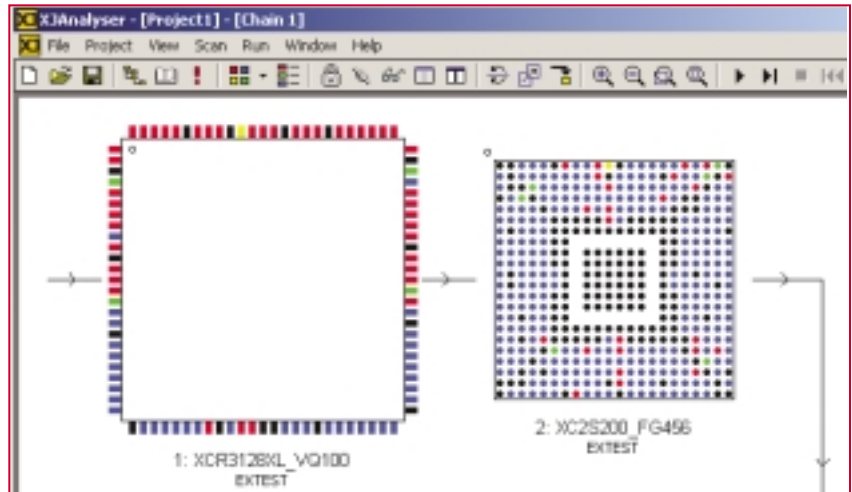


FIGURE 3. This graphical visualization of a BGA chip comes from XJTAG's XJAnalyser. Courtesy of XJTAG.

complex peripheral devices were equipped with boundary-scan registers, emulation test would not be necessary. The peripherals, including all I/O, could easily be tested by manipulating the interconnected boundary-scan cells. But when a boundary-scan register is not available, testing for proper connections—that is, manufacturing defects—is only possible through a quasi-functional test that uses the microprocessor to write to and read from the peripheral devices in a controlled way.

“At the same time,” he continued, “a processor that includes a boundary-scan register permits more extensive testing of that portion of the board. And if the peripheral devices, including memory devices, are JTAG compliant as well, the testability level increases dramatically. With a relatively small investment in silicon, chip vendors could have a major beneficial impact on board-level testability.”

Where boundary scan is headed

Critical to the success of JTAG-based standards is their acceptance by designers as well as manufacturing people. Yet, designers still resist any constraints on their creations that look like test. “Designers have knowledge that can be useful to test engineers,” Payne commented. “If testing starts with what you already know at the design stage, it gives you a head start. We have clients who have achieved test coverage of over 90%.”

He added, “XJTAG has taken several steps to get designers onboard. We’ve abstracted the process away from ‘test vec-

tors’ in favor of the more familiar environment of a programming language. We are so convinced that boundary scan is the future of hardware debug and testing that we allow engineers to freely try our system. That way, they can see firsthand what is possible using the JTAG scan chain on their own designs [Figure 3]. To increase awareness, we have produced a large number of case studies with design companies and contract manufacturers to demonstrate the benefits of using boundary scan throughout the product life cycle.”

Likewise, Woppman at ASSET Inter-Tech sees the teaming of boundary-scan companies with EDA vendors as critical. “In terms of embedded instrumentation, it is very critical for us to partner with EDA vendors, and that’s what we’ve done with all three of the big EDA companies,” Woppman said. “The EDA suppliers are at the beginning of the embedded instrumentation ecosystem, and tool vendors, like us, facilitate the effective deployment of embedded instruments later in the cycle.”

Goepel’s Puri emphasized the flexibility of the hardware and software test architectures to accommodate the new standards as they emerge. “The architecture has to be designed from the ground up to be scalable, modular, and integrated. At the same time, providing a single synergistic open platform is key. You partner with IC manufacturers, EDA companies, and ATE suppliers to find solutions for all stages from design validation to field repair.”

Van den Eijnden speculated, “Boundary-scan equipment must also be able to deal with reduced pin count and mixed 1149.1 and 1149.7 chains, including the system-level characteristics of systems-on-a-chip, where a single device might include multiple TAPs.

“Internal JTAG—P1687—tries to standardize access to instruments embedded in silicon,” he continued. “That effort resembles development of the SCPI [Standard Commands for Programmable Instruments] language that unified instrument commands in the days of IEEE 488. SCPI allowed commands to become independent of the instrument vendor. P1687 will have to define a similar approach.”

Levy predicted tighter coupling of boundary-scan capability into other test equipment. “Boundary scan has existed primarily independent of other board-test steps. Better integration will make it easier for customers to justify purchase of those larger test systems. There is still room to further optimize integration with IC and board testers to leverage the respective strengths of the boundary-scan and the host test systems.

“In general, more IC manufacturers are including test-access ports because their device packages prevent other approaches to structural testing. They are also adopting IEEE 1149.6, which supports testing AC-coupled and differential signals. As a result, boundary scan will find its way into a number of applications that until now have resisted it.”

Van Eijnden concluded, “Of course, it is important to understand the capabilities of any standard, but you also have to keep its actual application in mind. Ultimately, deciding to adopt a standard or a combination of standards should be based on the application, not on the standard itself. What may prove useful to you or your tools vendor for one application may turn out to yield no benefit somewhere else. In the final analysis, your judgment should always depend on what is best for your company and your customers.” T&MW

FOR FURTHER READING

For more about the history of the standards mentioned in this article, see:

Bonnett, David, “IEEE 1149.1 yields new standards,” *Test & Measurement World*, April 2002. www.tnworld.com/article/CA202501.html.