



Delivering Quality FPGA IP

Jason Lawley
Staff Engineering Manager

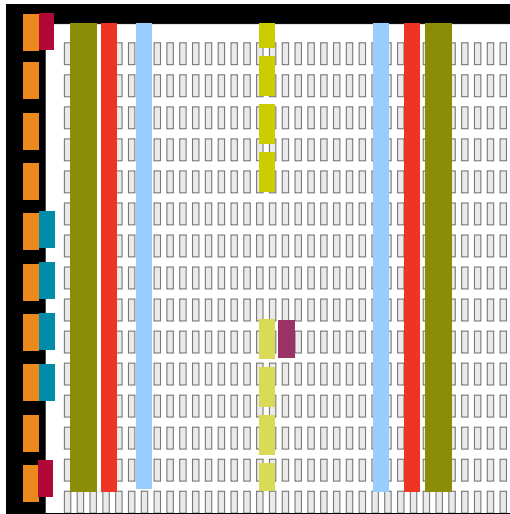
February 8, 2010











Agenda

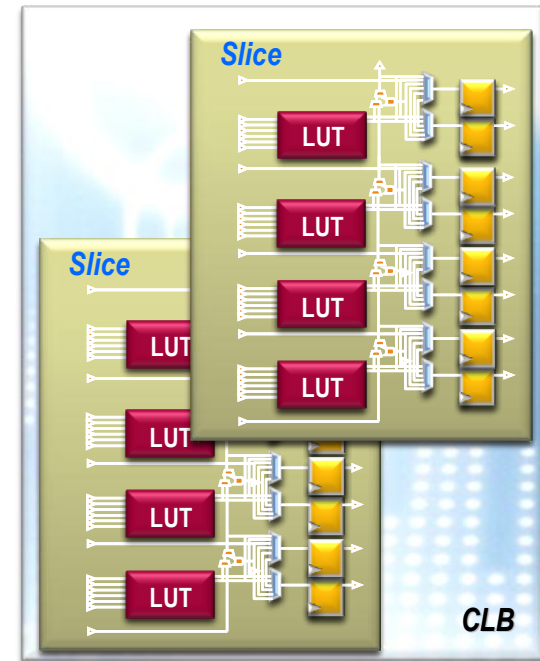
- **What is an FPGA**
- **Need for High Quality Verification for FPGA IP**
- **Hardware Validating FPGA IP**
- **Unique Challenges for FPGA IP**

What is an FPGA

FPGA

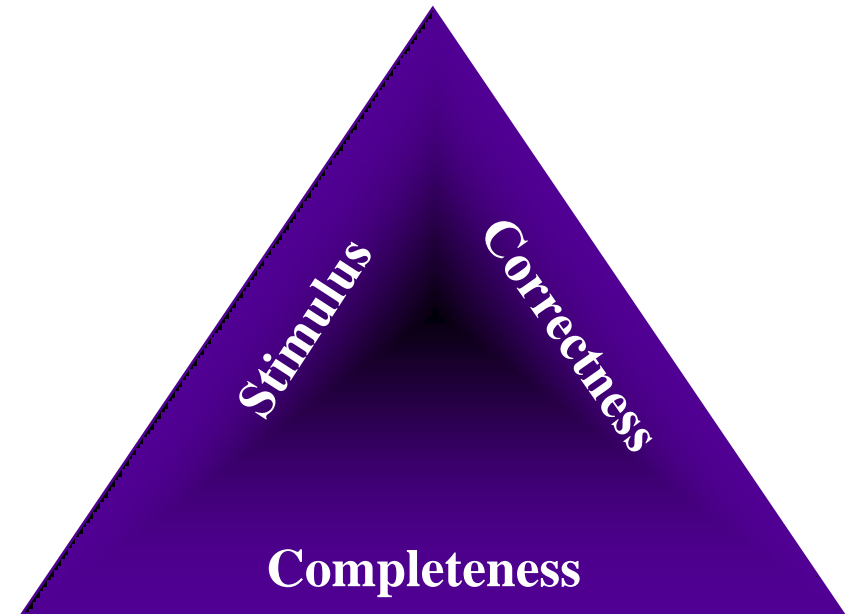


- | | | | |
|---|---------------------------|---|-------------------|
|  | LUT-6 CLB |  | FIFO Logic |
|  | Block RAM |  | Tri-mode EMAC |
|  | DSP Slices |  | System Monitor |
|  | High-performance Clocking |  | HSS Transceivers* |
|  | Parallel I/O |  | PCIe® Interface |

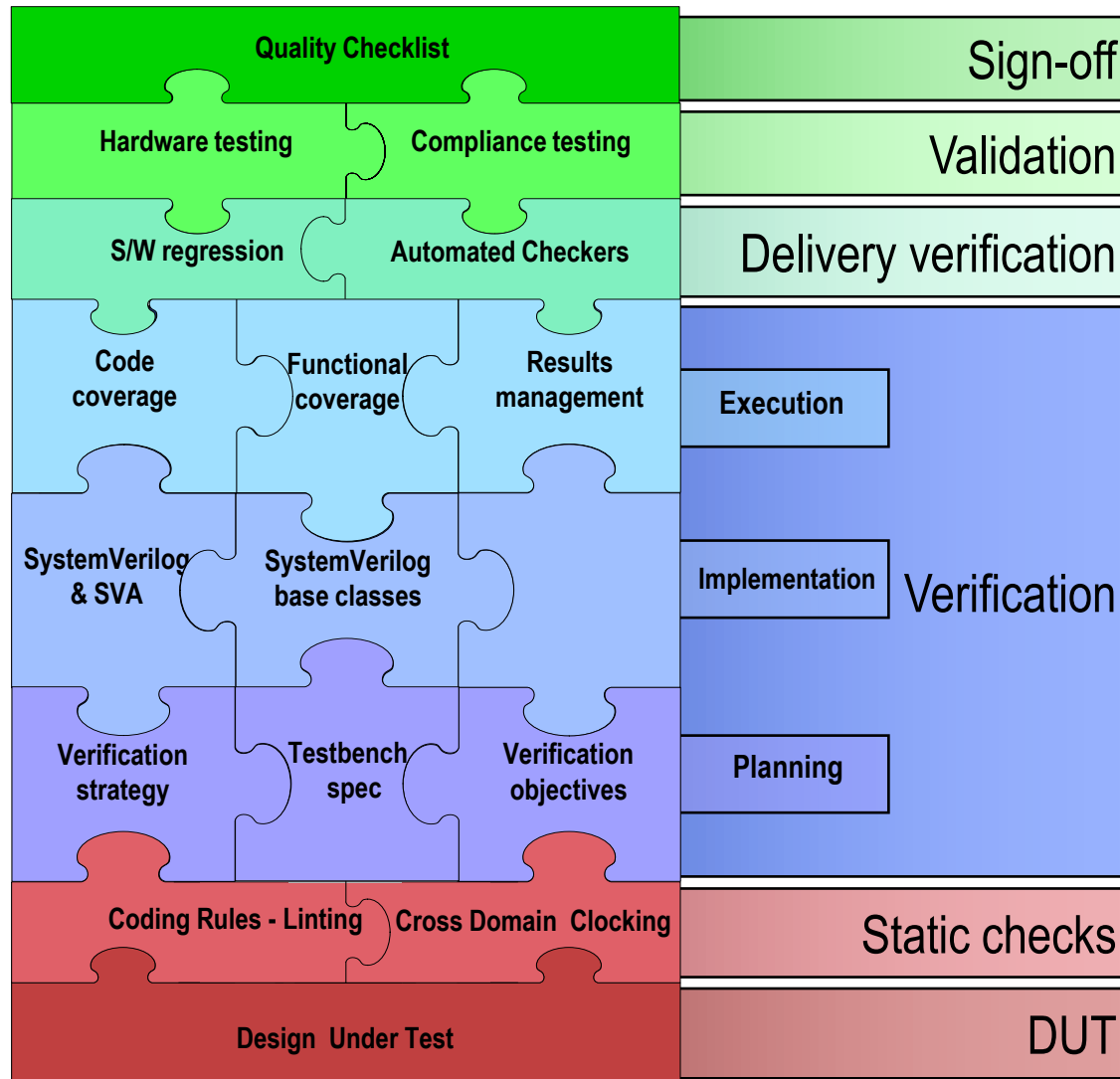


Fundamentals of RTL Verification

- **DUT meets intended functionality**
- **Importance of FPGA Verification**
 - Implementing in hardware is NOT verification
 - Same flows as ASIC or ASSP
 - Bug free mindset



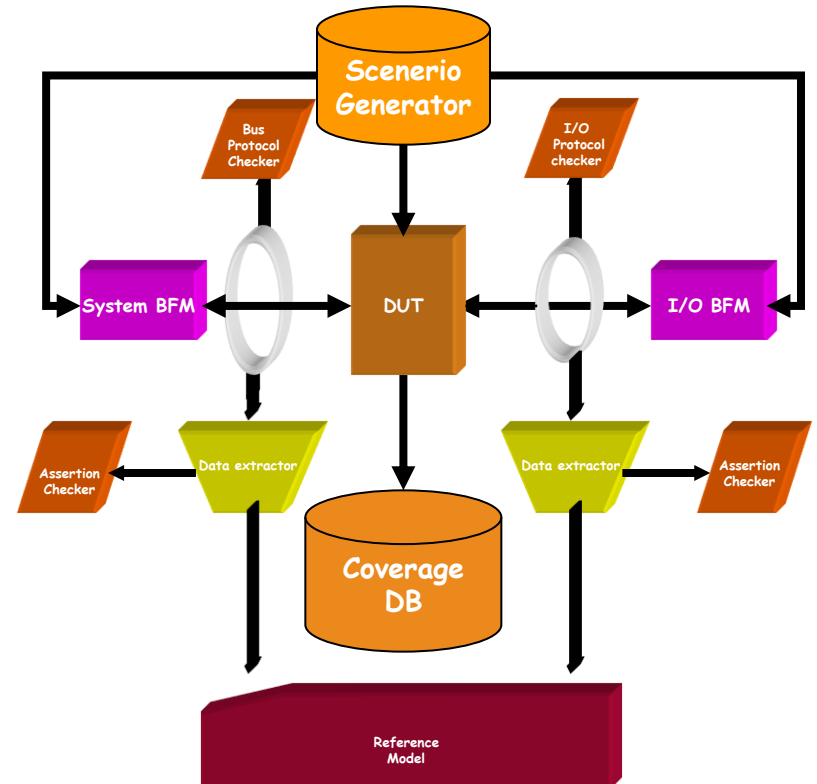
Verification is a Process



Putting it all together . . .

■ IP RTL verification methodologies

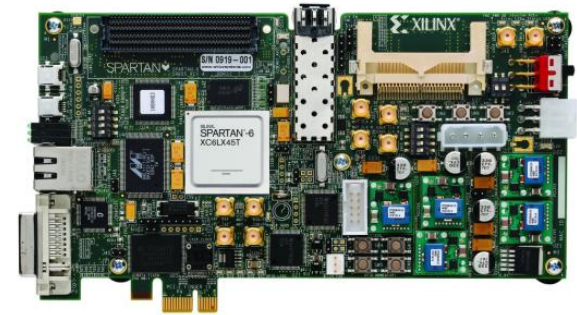
- Industry standard methodologies (OVM, VMM, etc.)
- Constrained Random stimulus
- Functional Coverage
- Assertions actively document assumptions
- Standardized coding rules checked with lint
- Clock domain crossing checks
- Track key metrics



Hardware Validation of IP

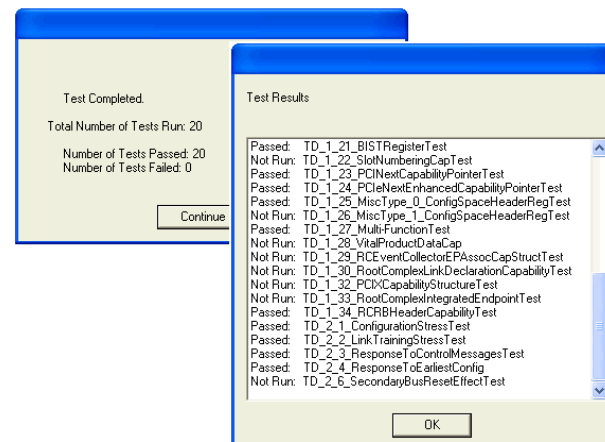
■ FPGAs allow for easy hardware validation

- Inexpensive development platforms
- Pseudo-randomly insert errors in hardware
- Increase customer confidence – show working hardware
- Increase your own confidence too!



■ Take advantage of industry standard testing

- PCI-SIG Plugfest
- RIOLAB
- UNH-IOL



Parameterization Challenges

- **FPGA IP typically highly parameterized**
 - FPGA logic is expensive
 - All valid parameter combinations must be supported
- **Simulation implications**
 - Coverage space growth is non-linear
- **Synthesis implications**
 - Parameters resolved at compile time
 - FPGA flexibility allows pre-synthesis parameter settings

Performance Challenges

- **IP architecture can change mid cycle or across FPGA families**
 - Transaction accurate simulations allow flexibility
- **IP timing closure sensitivity**
 - Targeted device
 - IP parameters interaction
 - System integration
- **Randomized implementation runs**
 - Implement IP across different part/package combinations
 - Verify timing closure

Conclusion

- **FPGA IP RTL verification must be best in class**
 - Zero bug mentality
- **Hardware validation ensures quality products**
 - But it is not a substitute for verification!
- **FPGA verification challenges**
 - Parameters, performance and parts
- **Questions?**