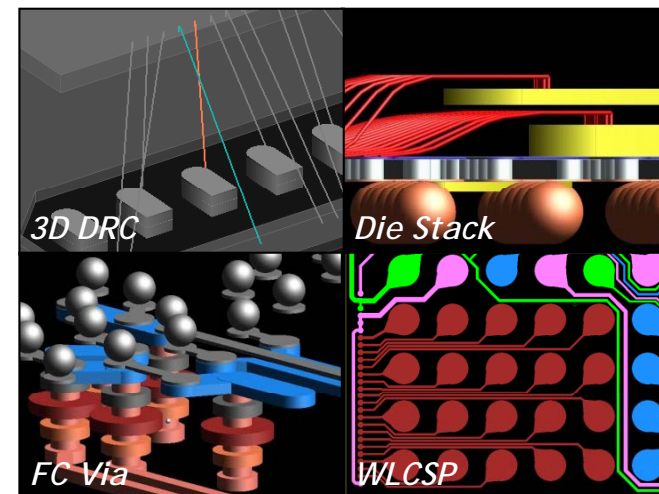
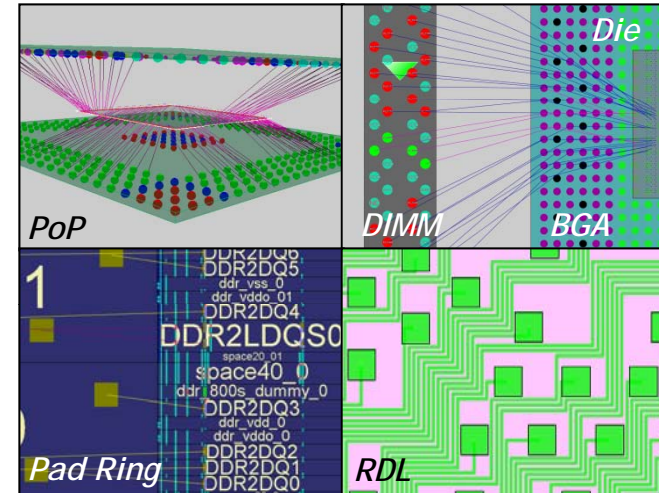




Sigrity for 3D Design and Analysis

- OrbitIO (codesign)
 - Comprehensive codesign solution for pad ring and system planning
 - Define/optimize IO device placement, pin/net assignments, and connectivity across multiple substrates
- UPD (package implementation)
 - Performance driven layout addressing the broadest range of advanced IC packages
 - Integrated 3D design and DRC





Sigrity for 3D Design and Analysis

- **XcitePI (chip-centric analysis)**
 - Chip/system co-simulation for time and frequency domain analyses
 - Chip-Power and Chip-IO Model extractions
 - Power Planning analysis – system codesign
- **XtractIM (package extraction and assessment)**
 - Extraction and display of RLCK and broadband package models
 - Rapid assessment of power delivery and signals
 - Automated model connectivity to third party chip and system co-simulation
- **SpeedXP Suite (system-centric analysis)**
 - Whole-package/board simultaneous analysis of power delivery and signal nets
 - Static and dynamic IR drop, impedance, delay, resonance, crosstalk, SSO, emissions

