3D Design using 2D tools

John Barth
IBM, Distinguished Engineer
Burlington, Vermont
February 25, 2011

© 2011 IBM Corporation

Outline

- **3D Motivation – It's all about memory**
  - http://www.youtube.com/watch?feature=player_detailpage&v=cU-AhmQ363I
- **TSV Processing and Options**
- **Design Tools**
  - Simulation
  - Layout and Verification
    - DRC
    - LVS Prototype
  - Extraction, PTN (Power, Thermal, Noise) Modeling
- **Standards Opportunity**

© 2011 IBM Corporation

Why Now ?

Early Work Dates Back 20 Years
Bertin et al 1993

This did not materialize !
What has changed ?

- Scaling Challenges
- Power
- Insatiable Appetite for Memory

US005202754A

United States Patent [19]
Bertin et al.

[11] **Patent Number:** 5,202,754
[45] **Date of Patent:** Apr. 13, 1993

[54] THREE-DIMENSIONAL MULTICHIP PACKAGES AND METHODS OF FABRICATION

[75] Inventors: Claude L. Bertin; Paul A. Farrar, Sr., both of South Burlington; Howard L. Kalter, Colchester; Gordon A. Kelley, Jr., Essex Junction; Willem B. van der Hoeven, Jericho; Francis R. White, Essex, all of Vt.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 760,041

[22] Filed: Sep. 13, 1991

[51] Int. Cl.⁵ H01L 29/78; B44C 1/22
[52] U.S. Cl. 257/684; 257/777; 257/723; 257/725
[58] Field of Search 357/75, 80, 74, 71, 357/72

[56] References Cited

U.S. PATENT DOCUMENTS

3,564,358	2/1971	Hahnlein	317/235
3,679,941	7/1972	Lacombe et al.	357/75
4,525,921	7/1985	Carson et al.	29/577 C
4,612,083	9/1986	Yasumoto et al.	156/633
4,646,627	3/1987	Abernathey et al.	29/571
4,717,448	1/1988	Cox et al.	156/643
4,807,021	2/1989	Okumura	357/75
4,829,018	5/1989	Wahlstrom	437/51
4,937,659	6/1990	Chall, Jr.	357/75
4,939,568	7/1990	Kato et al.	357/75
4,954,458	9/1990	Reid	437/51
4,954,875	9/1990	Clements	357/75
4,967,393	10/1990	Yokoyama et al.	365/185
4,989,063	1/1991	Kolesar, Jr.	357/75
5,091,762	2/1992	Watanabe	357/75

FOREIGN PATENT DOCUMENTS

0314437	3/1989	European Pat. Off. .
0374971	6/1990	European Pat. Off. .
3233195	3/1983	Fed. Rep. of Germany .
58-43554	3/1983	Japan .
60-79763	5/1985	Japan .
61-22660	1/1986	Japan .
1326758	8/1973	United Kingdom .

OTHER PUBLICATIONS

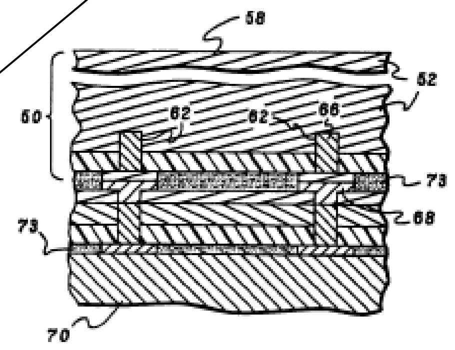
Lasky, J. B., "Wafer Bonding for Silicon-on-Insulator Technologies," Appl. Phys. Lett., vol. 48, No. 1, pp. 78–80, Jan., 1986.
Lineback, J. Robert, "3D IC Packaging Moves Closer to Commercial Use," Electronic World News, pp. 15 & 18, May 21, 1990.

Primary Examiner—Eugene R. LaRoche
Assistant Examiner—Viet Q. Nguyen
Attorney, Agent, or Firm—Heslin & Rothenberg

[57] ABSTRACT

A fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips interconnected at least partially by means of a plurality of metallized trenches are disclosed. The fabrication method includes providing an integrated circuit chip having high aspect ratio metallized trenches therein extending from a first surface to a second surface thereof. An etch stop layer is provided proximate the termination position of the metallized trenches with the semiconductor substrate. Next the integrated circuit device is affixed to a carrier such that the surface of the supporting substrate is exposed and substrate is thinned from the integrated circuit device until exposing at least some of the plurality of metallized trenches therein. Electrical contact can thus be made to the active layer of the integrated circuit chip via the exposed metallized trenches. Specific details of the fabrication method and the resultant multichip package are set forth.

6 Claims, 8 Drawing Sheets

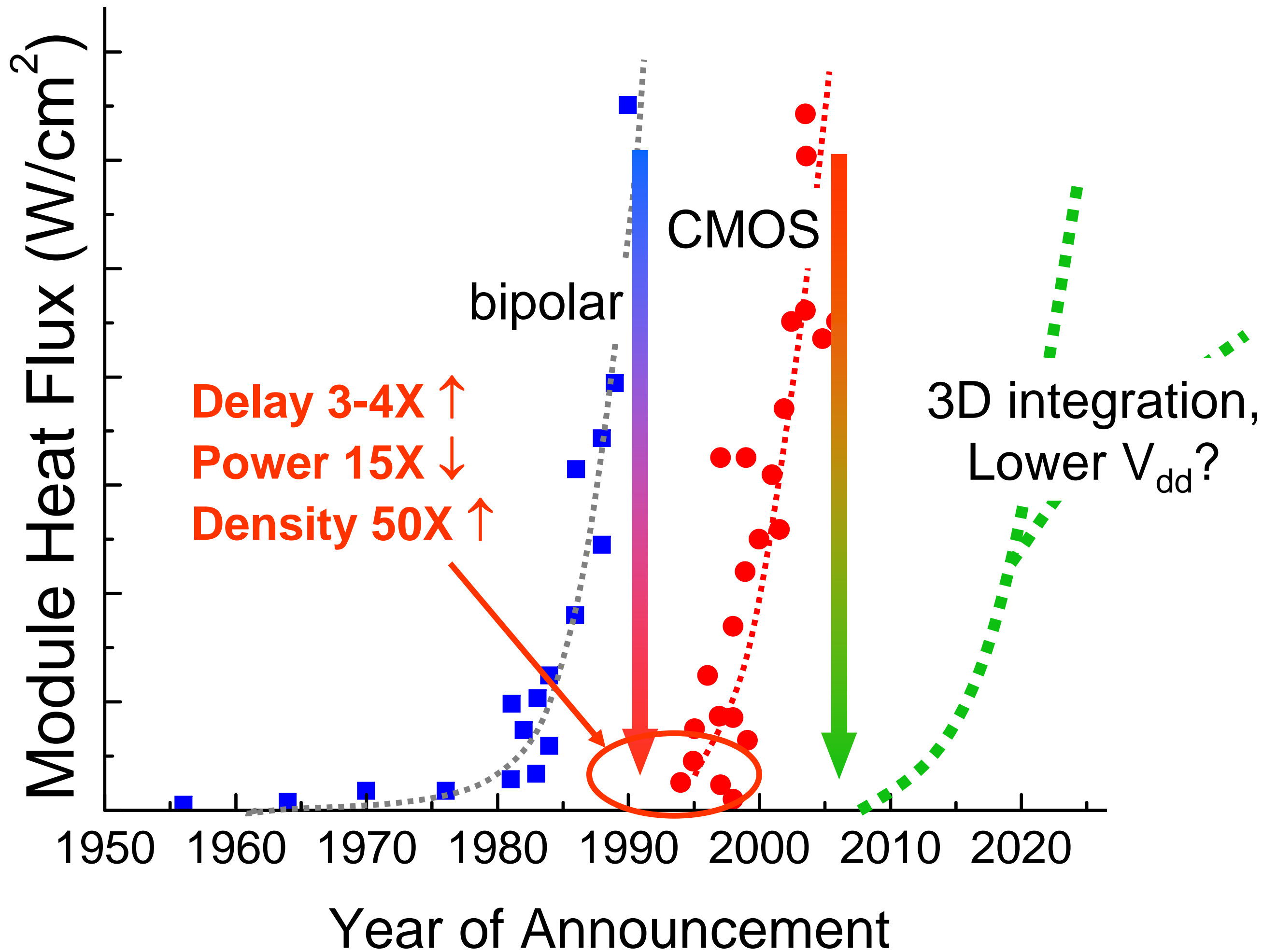


78–80, Jan., 1986.
Lineback, J. Robert, "3D IC Packaging Moves Closer to Commercial Use," Electronic World News, pp. 15 & 18, May 21, 1990.

Primary Examiner—Eugene R. LaRoche

© 2011 IBM Corporation

Scaling and the Power Crisis



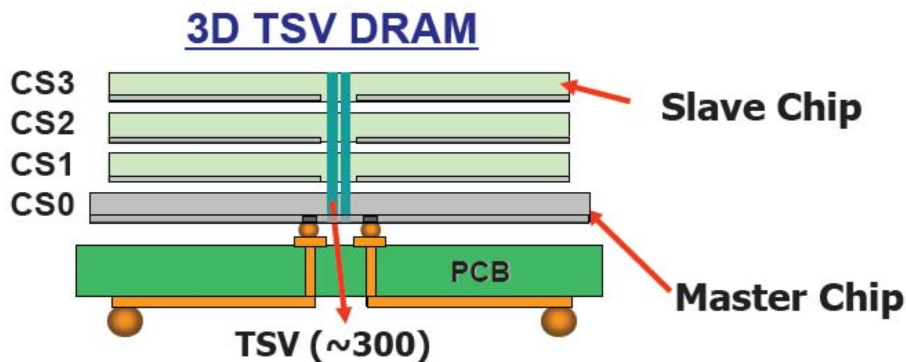
After: R. Schmidt *et al.*, IBM J. R&D, (2002).

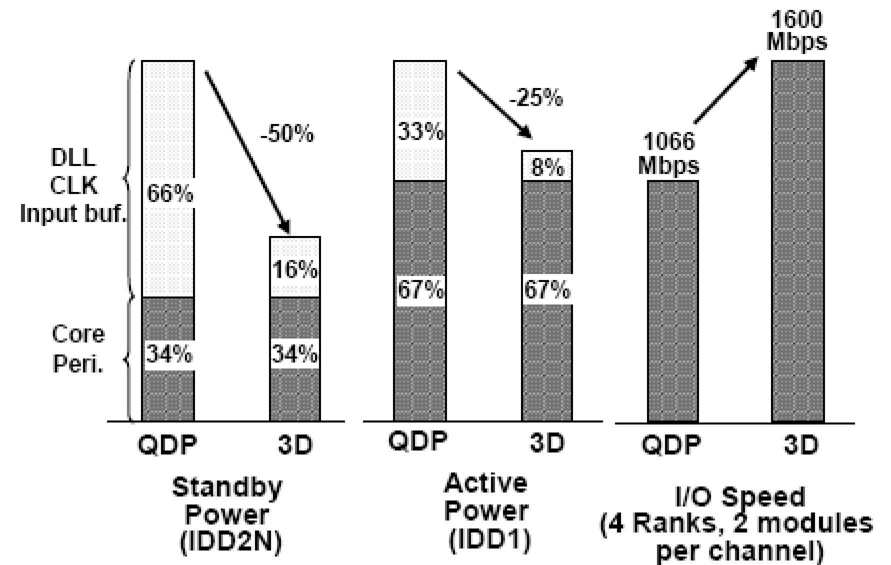
© 2011 IBM Corporation

Stacked DRAMs to increase capacity without increasing power

- **I/O ckts drive considerable power requirements**
- **These do not need to be duplicated on multiple DRAMs**
- **Master – Slave approach to share I/Os, PLLs etc**
- **Enabled by TSVs**

- **Must compete with conventional scaled 3D chip**





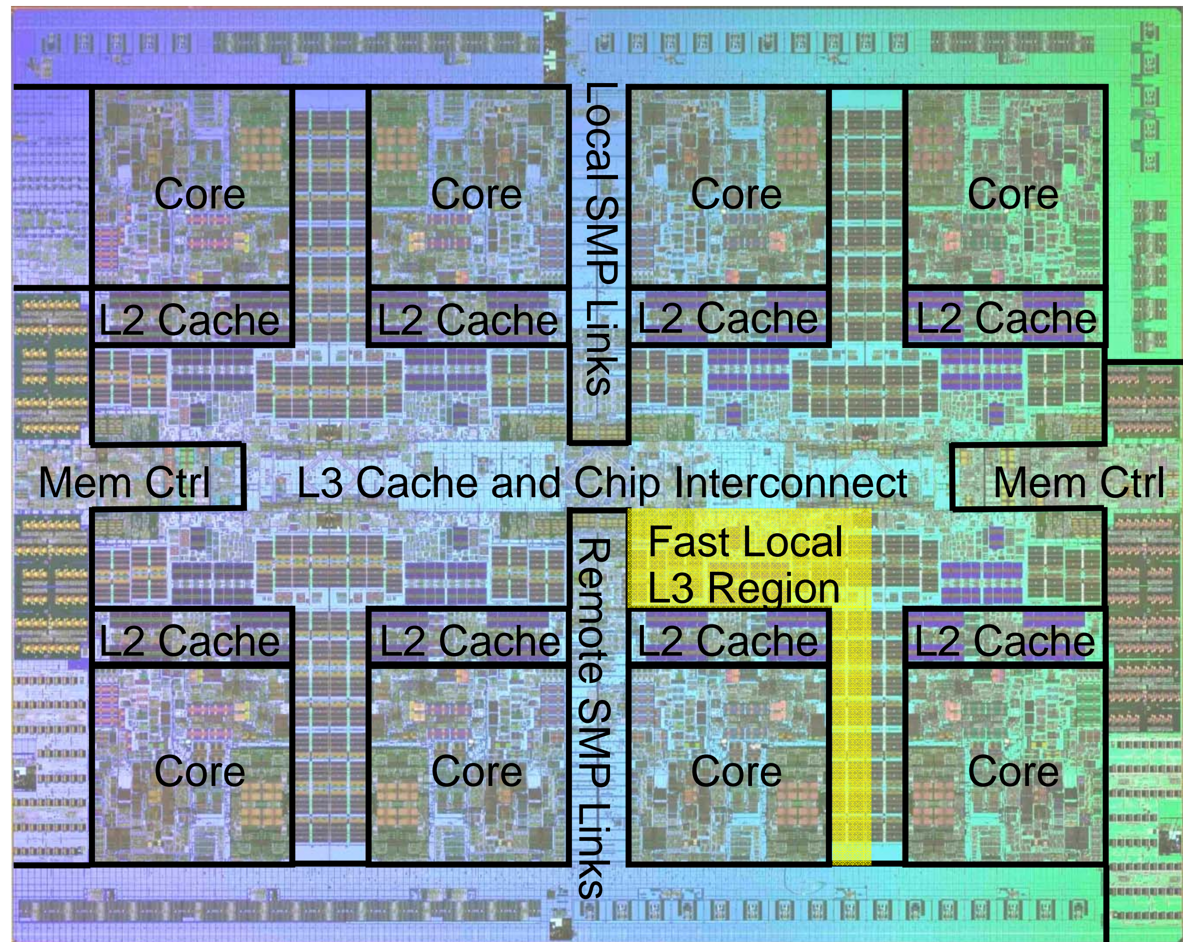
Kang et al, ISSCC 2009

© 2011 IBM Corporation

Power7™ Processor

- 567mm²
- 32MByte on chip eDRAM
- 1.2B Transistors
  - Equivalent to 2.7B
  - eDRAM Efficiency
- Eight Processor Cores
- eDRAM ~11% Die Area
- Balanced Performance
- Dual DDR3 Controllers
- SMP Links

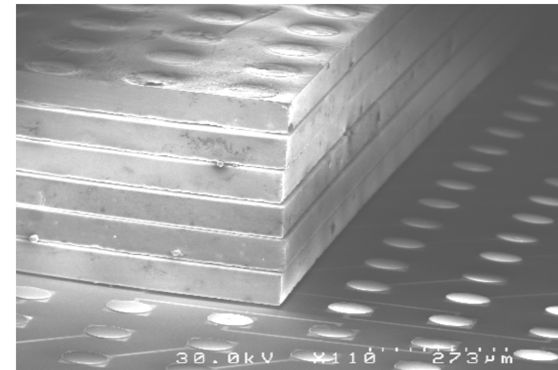
  20k Coherent Operations
- 590 GB/s Total Bandwidth



Power7 Described in Sessions 5.4, 9.3 and 19.2 at ISSCC 2010

© 2011 IBM Corporation

Opportunities to Add System Value Through 3D Integration



Leverage 3D for:

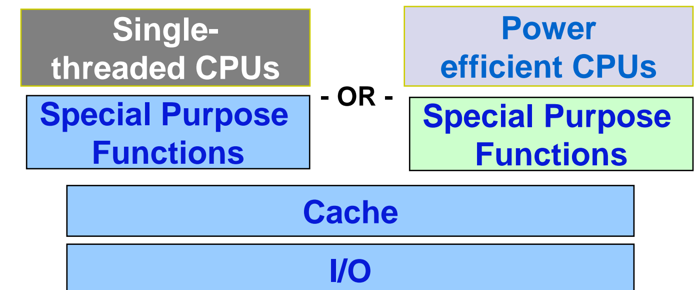
Power efficiency
- Reduced interconnect power (chip-chip)

Form factor
- Higher effective density by stacking

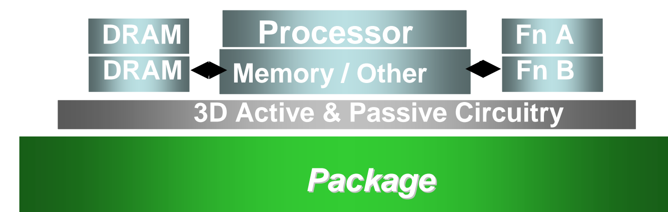
Modularity / Re-use
- Separate IP macros (memory, analog, logic) on to different layers; reuse IP in new applications

Optimized system design
- Restructure systems to leverage added bandwidth, capacity, lower latencies, and capabilities enabled by 3D

Modularity



Optimized System Design

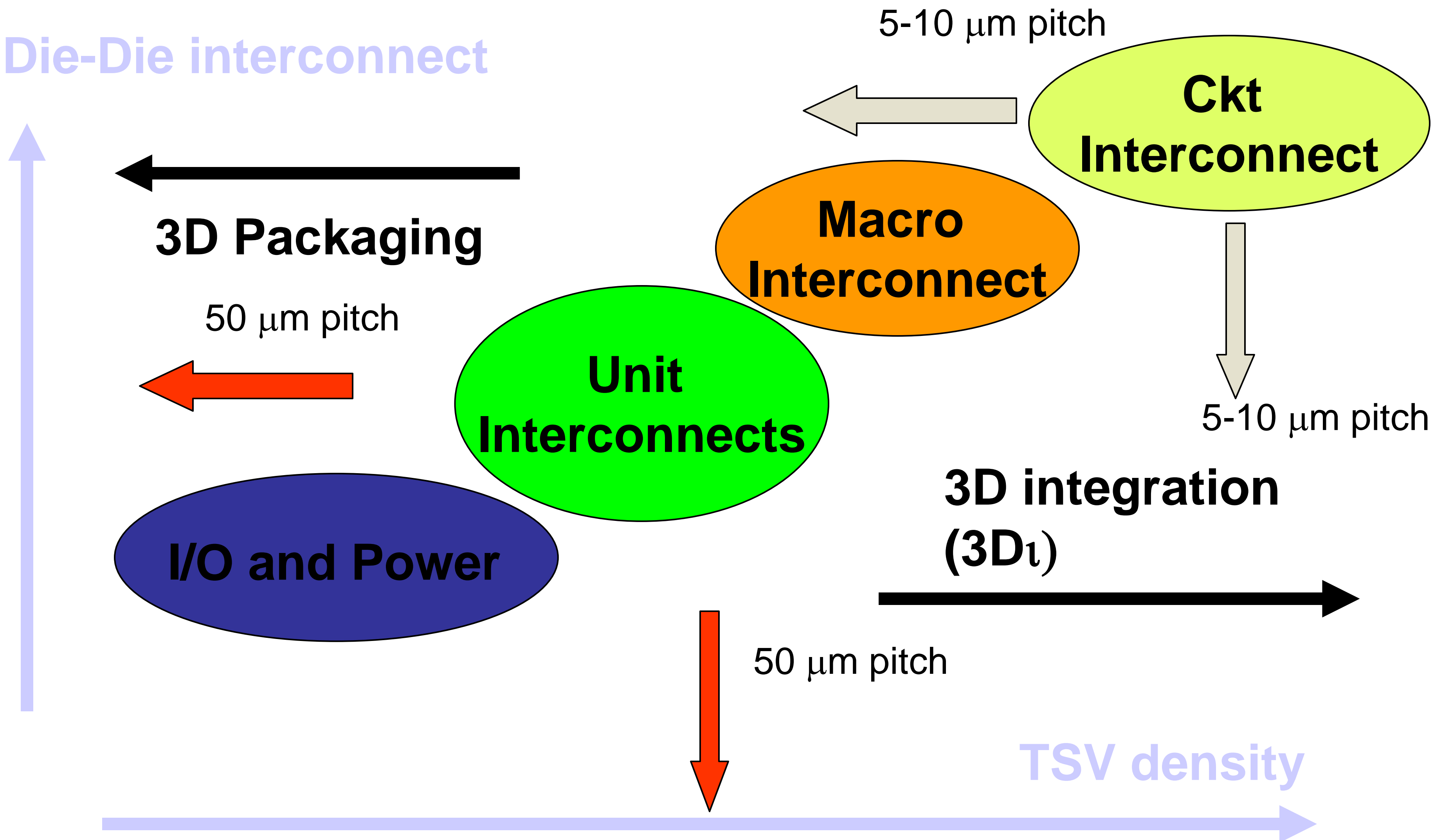


© 2011 IBM Corporation

3D Technology

© 2011 IBM Corporation

3D Packaging Vs Integration

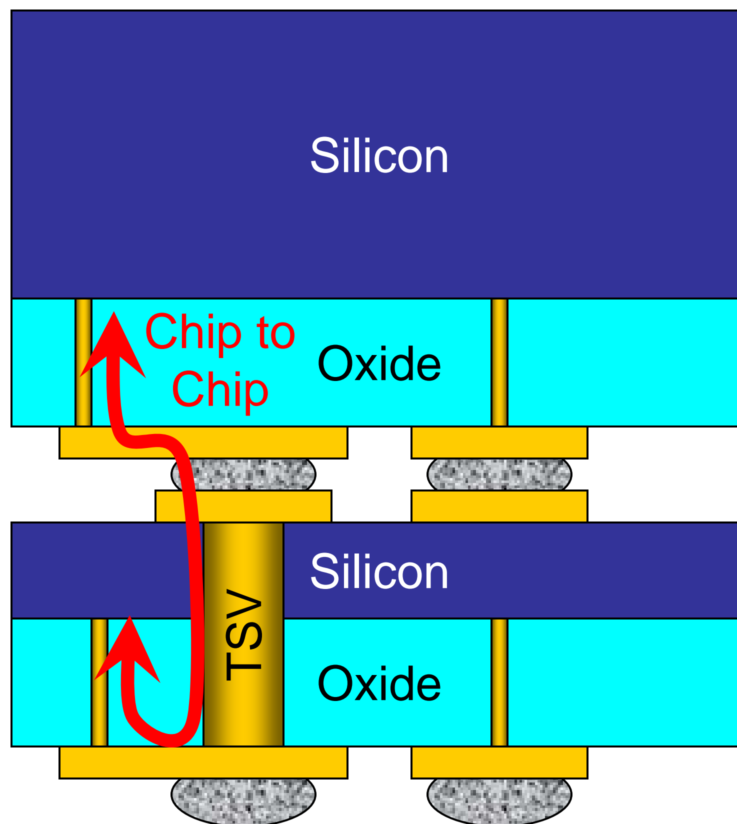


© 2011 IBM Corporation

Multiple Assembly Processes – Wafer to Wafer / Chip to Chip

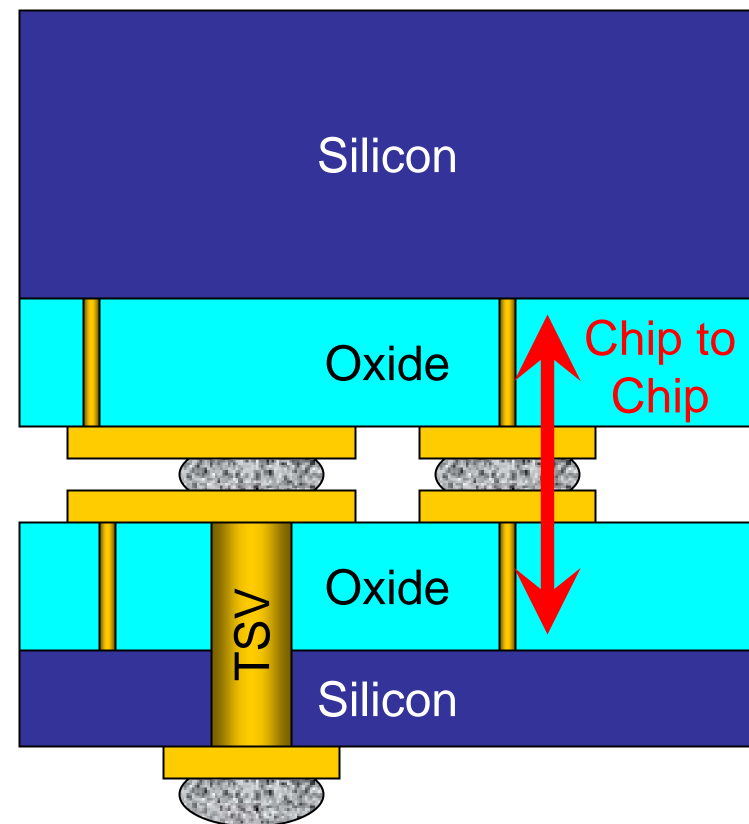
Face to Back (F2B)

- Easier to Design (No Mirror)
- Chip to Chip requires TSV



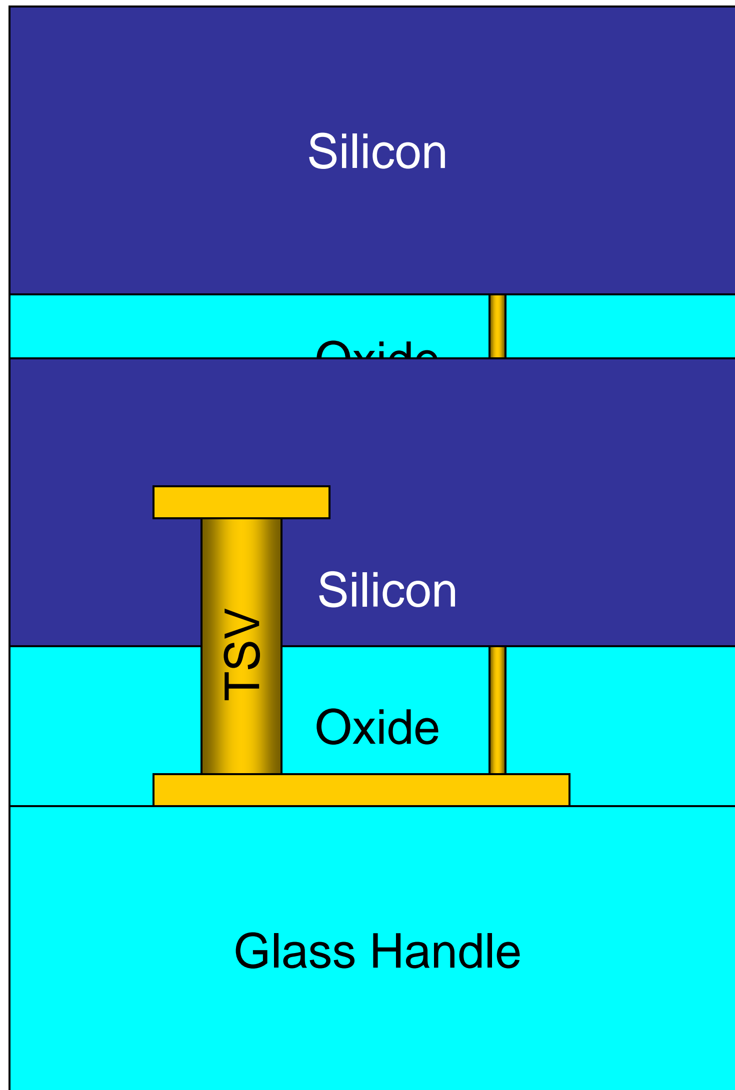
Face to Face (F2F)

- Easier to Process
- Chip to Chip w/o TSV



© 2011 IBM Corporation

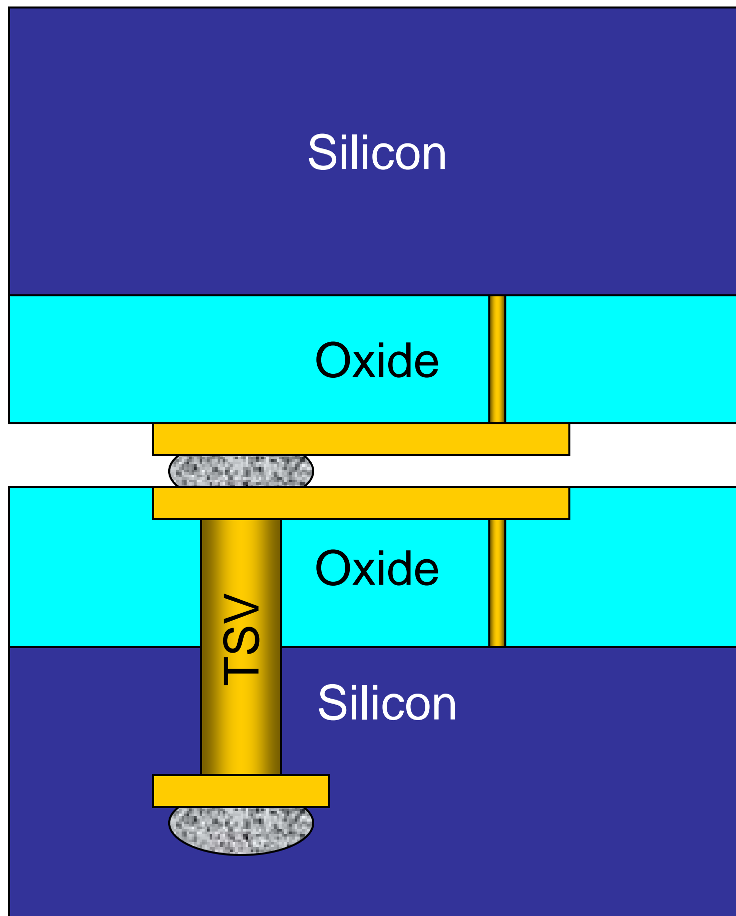
F2B – Processing Requires Glass Handle Wafers



1. Build Transistors and Back End Metal / Flip

© 2011 IBM Corporation

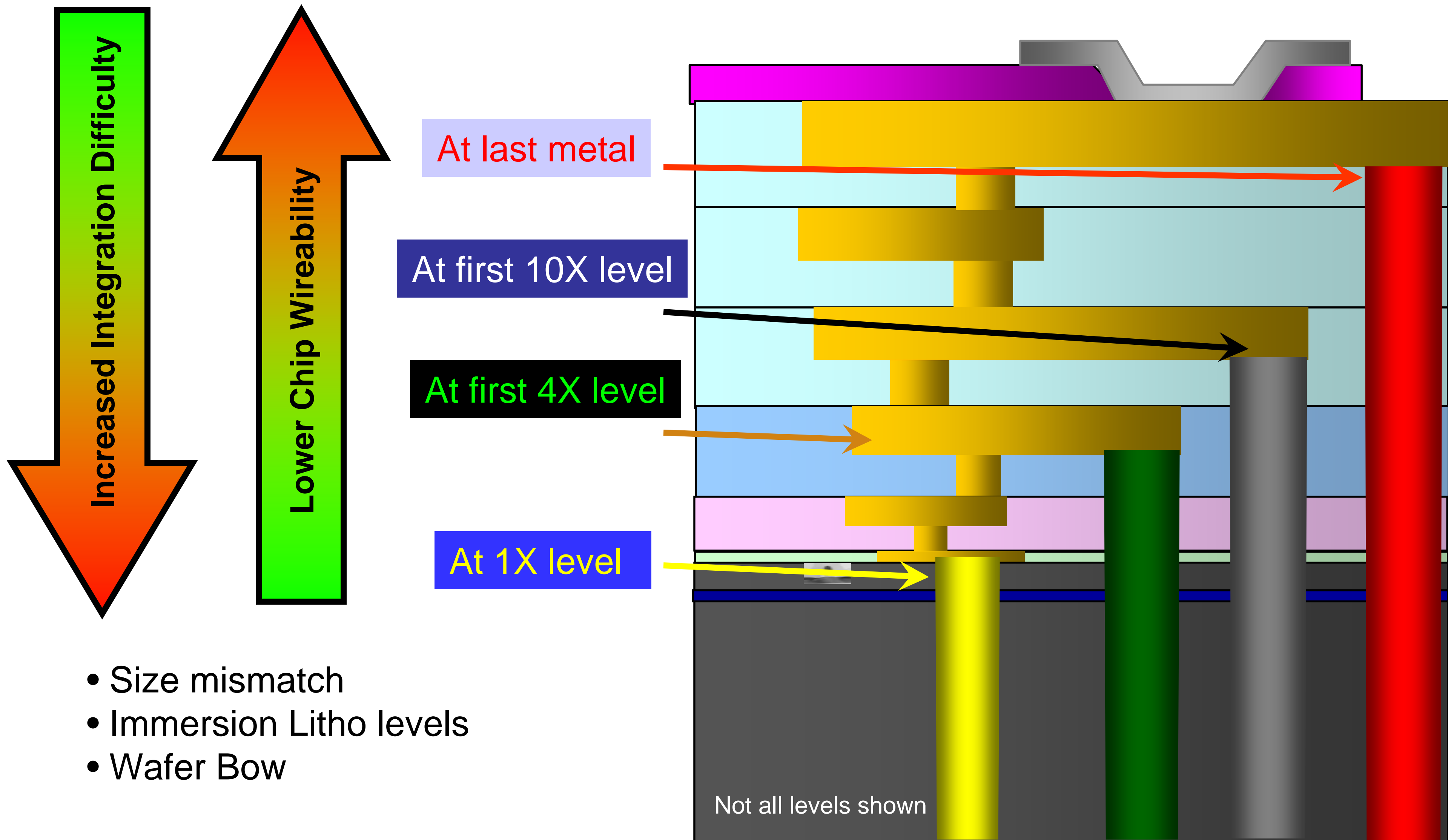
F2F – Requires 1 less Glass Handle wafer



1. Build Transistors and Back End Metal / Flip

© 2011 IBM Corporation

Where TSVs Connect in a hierarchical wiring scheme



- Size mismatch
- Immersion Litho levels
- Wafer Bow

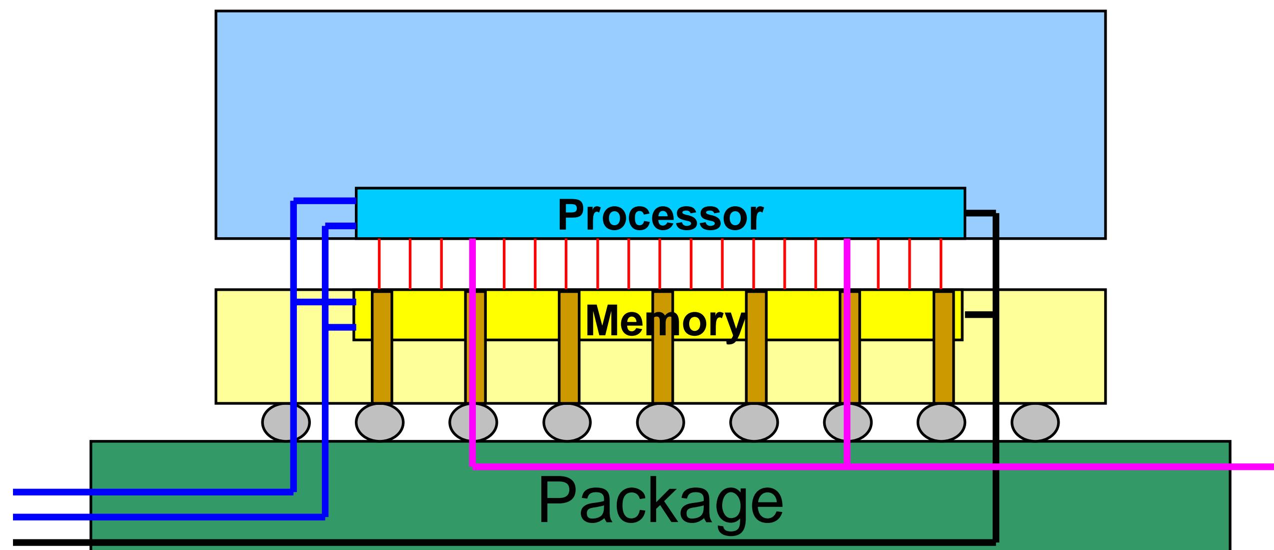
© 2011 IBM Corporation

3D Design

© 2011 IBM Corporation

3D Fundamentally Affects VLSI Design

- **3D designs will require 3D-compliant and optimized:**
  - Chip infrastructure elements:
    - Clock, power, and ground distribution
  - IP blocks:
    - SRAM, eDRAM, and non-traditional arrays
    - Custom and random logic
    - Within-stack and off-socket bussing and I/O
    - Analog, special functions, new materials
  - Design know-how, and supporting methods and tools:
    - Early and detailed planning and partitioning
    - Electrical and physical optimization and design
    - Checking and verification
    - Capture of power & thermal effects



© 2011 IBM Corporation

3D Design Methodology: New Considerations

- TSV & Stack Design Planning
- Early Power, IR Drop Analysis
- Early Clock Structure Design
- Stack Thermal Analysis

- Finalize TSV & Stack Networks
- Clock Design Across Stack
- TSV-Aware Logic, Circuit, Physical Design

- 3D Timing
- 3D-Aware Layout-to-Schematic & Schematic-to-Logic
- Stack Continuity Analysis
- TSV Design Rule checking

Planning/High Level Design Phases

- Additional architectural and physical planning needed for shared stack resources during HLD of individual layers

Design Development Phase

- Partitioning of shared stack resources to allow individual layers to proceed independently
- Additional constraints/contracts and crosschecks to ensure design closure at both the stack level and system level

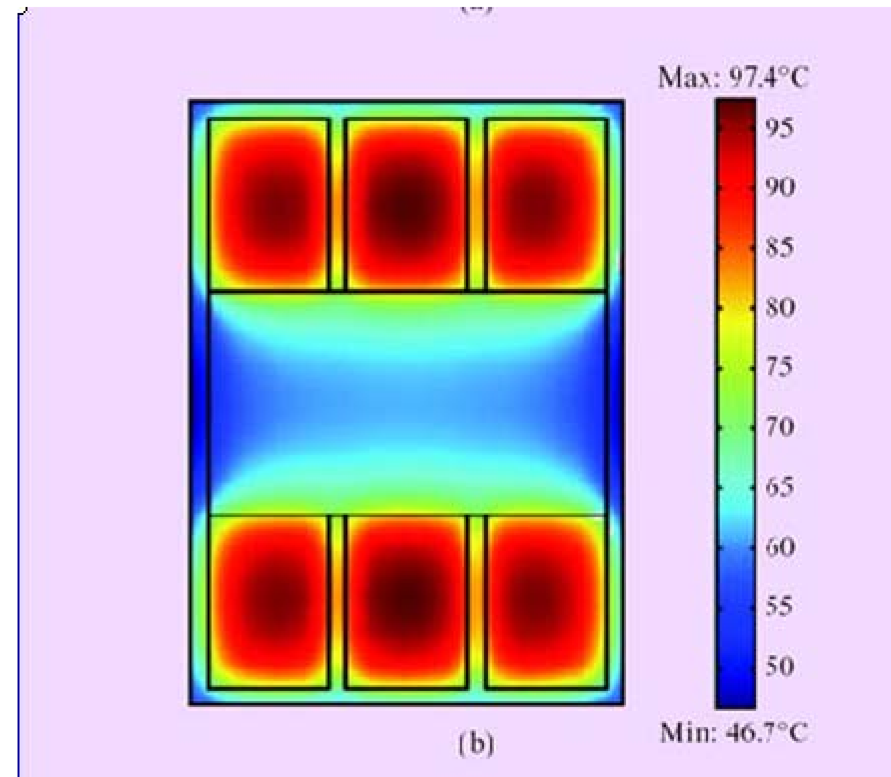
Chip-Release Phase

- Planning of release data or abstracts for checks
- Closure on stack level verification (e.g. functionality, timing, thermal) against other layers or stack contracts

© 2011 IBM Corporation

Thermal constraints become circuit level design issue

- **Stacking a memory die over a high power processor die causes**
  – Mean Temperature increases by 4-5 C deg.
  – Hot spots can increase by >10-12 C deg.
- **More thermal resistance to Heat sink**
- **Thinned die do not spread heat as well as thick die**
- **Thermal Analysis tools need to be easier to use by average User**



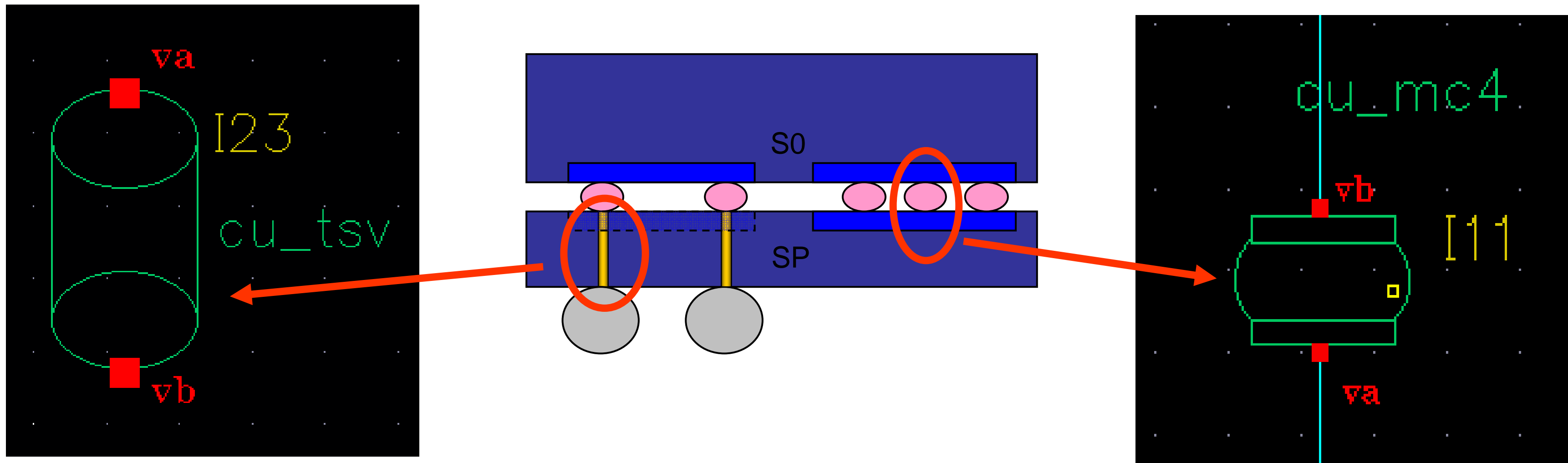
Sri-Jayantha *et al*

© 2011 IBM Corporation

3D Simulation

© 2011 IBM Corporation

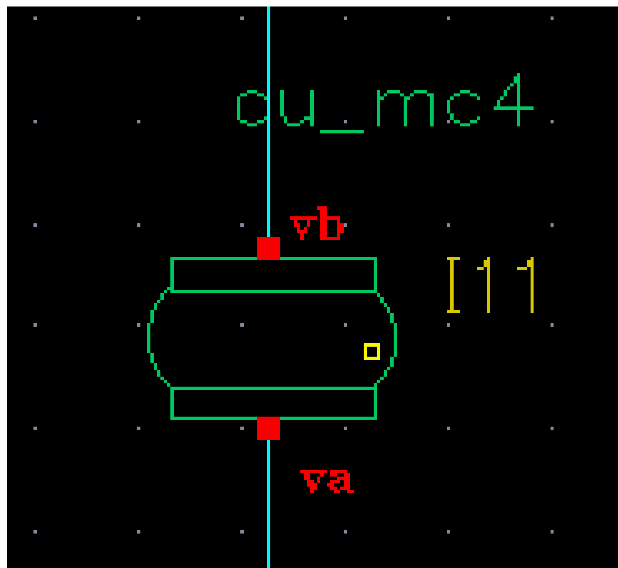
Schematic Entry



Rachel Gordin / Haifa Team - 2010

© 2011 IBM Corporation

Standard Schematic Entry



Apply To: only current | instance

Show: ☐ system ☑ user ☑ CDF

Browse | Reset Instance Labels Display

Property	Value	Display
Library Name	22SOI_cu_mc4_model	off
Cell Name	cu_mc4	value
View Name	symbol	off
Instance Name	I11	value

Add | Delete | Modify

CDF Parameter	Value	Display
Corner factor [-1,1]	-1	off

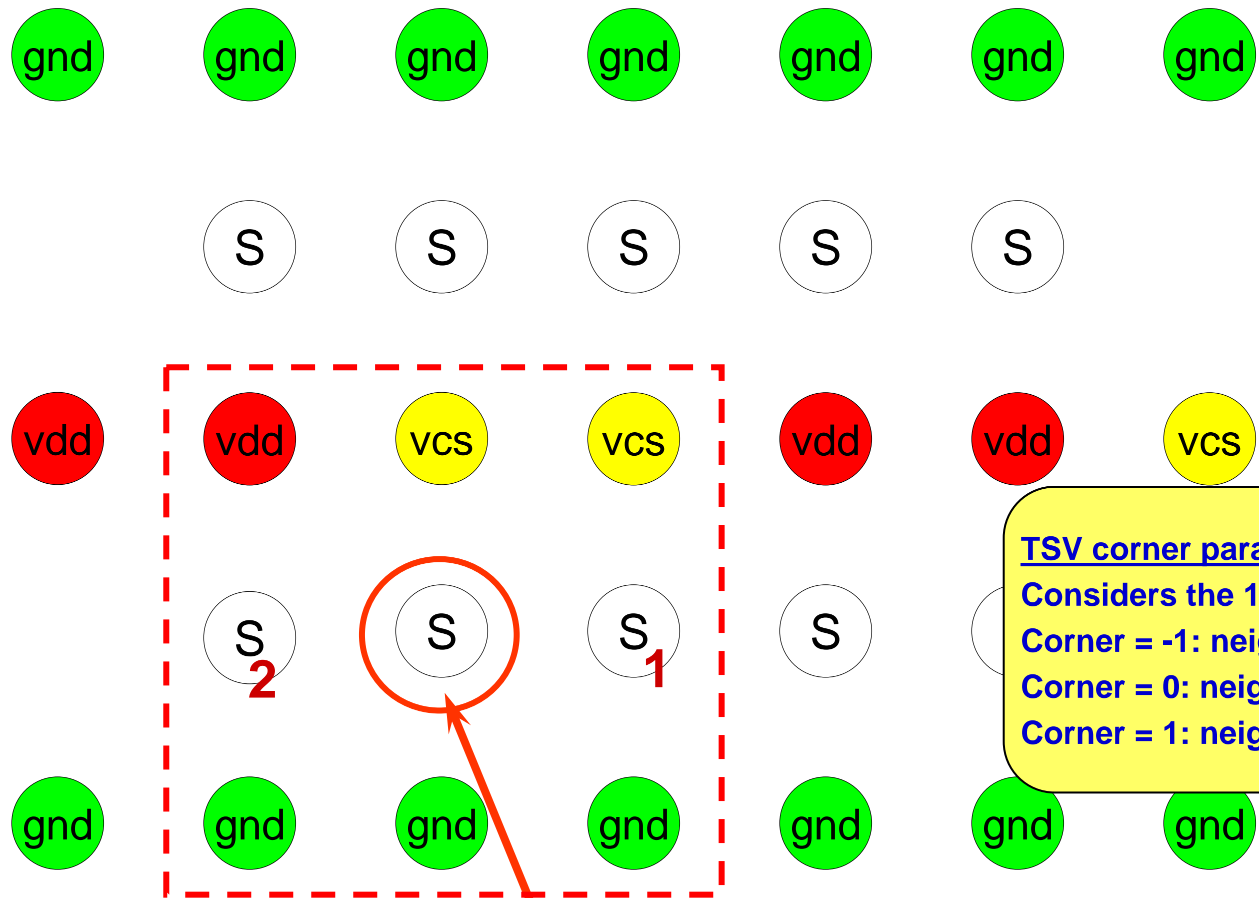
OK | Cancel | Apply | Defaults | Previous | Next | Help

Corner factor

Rachel Gordin / Haifa Team - 2010

© 2011 IBM Corporation

TSV connection to C4: Horizontal model domain



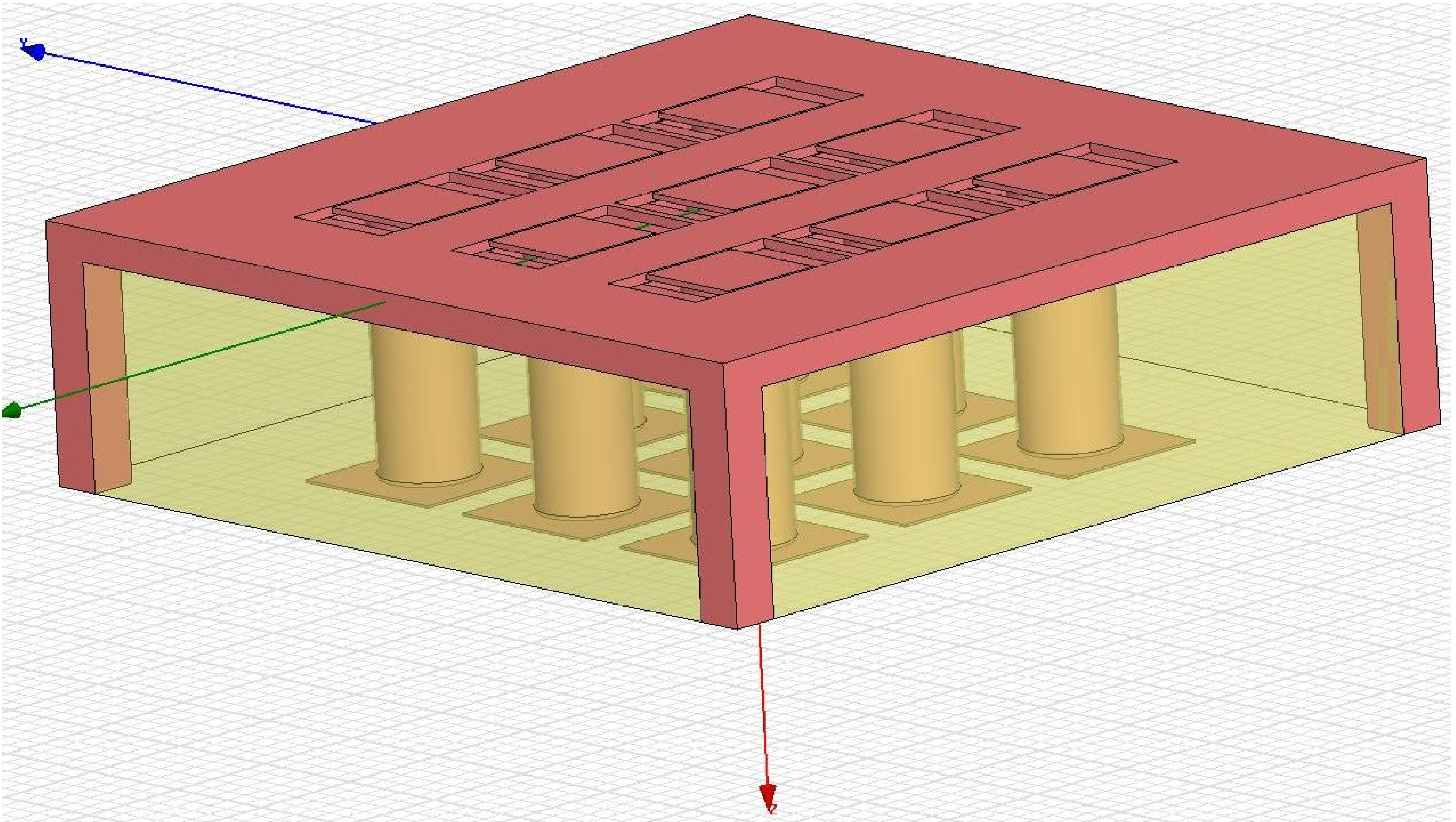
TSV corner parameter [-1 ..1]
Considers the 1 and 2 neighbor TSVs impact
Corner = -1: neighbors bear “hostile” signals
Corner = 0: neighbors are ground/VDD
Corner = 1: neighbors bear “friendly” signals

Signal TSV to be modeled

© 2011 IBM Corporation

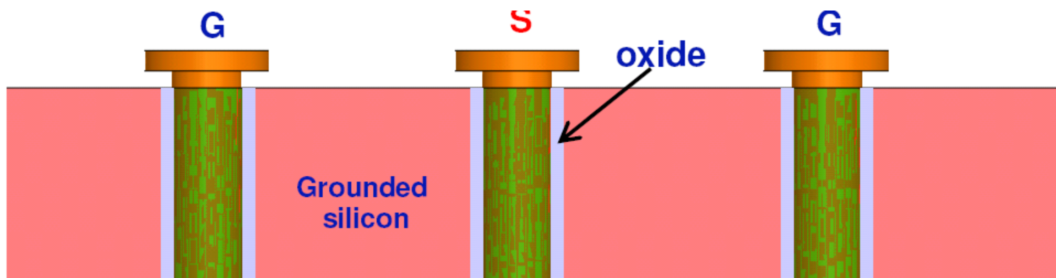
TSV pattern – problem definition

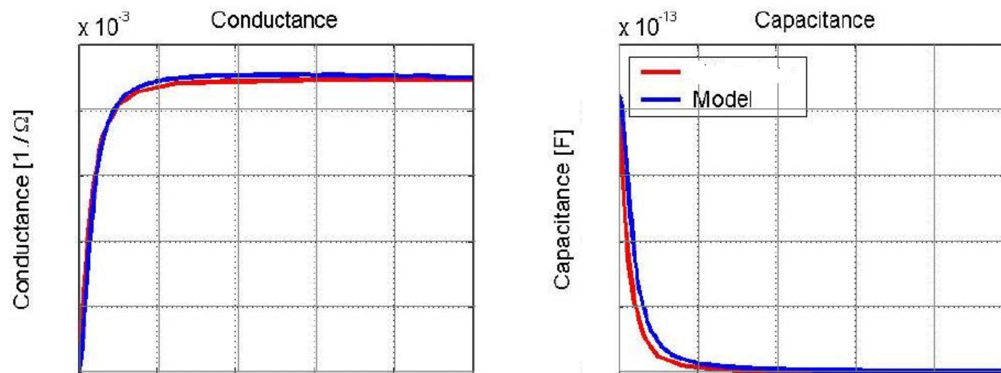
EM Field Solver – works for TSVs



© 2011 IBM Corporation

TSV and μ-bump enablement





Apply To: only current | instance
Show: system | user | CDF

Browse | Reset Instance Labels Display

Property	Value	Display
Library Name	22SOI_3di_models	off
Cell Name	cu_tsv	value
View Name	symbol	off
Instance Name	I10	value

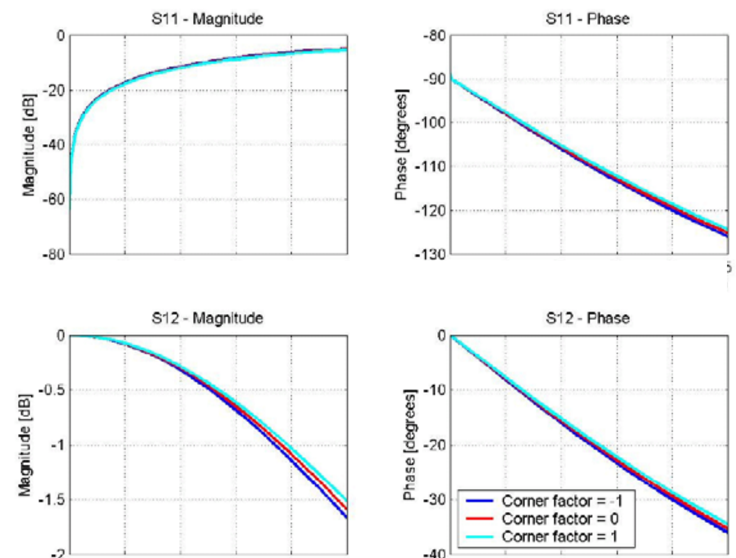
Add | Delete | Modify

CDF Parameter	Value	Display
Corner factor [-1,1]	0	off
Temperature	25	off

OK | Cancel | Apply | Defaults | Previous | Next | Help

- TSV models developed – node agnostic
  - Silicon dielectric relaxation dominates at high frequencies
- TSV placement and connectivity tools
- inter-strata μ-bump rules and models

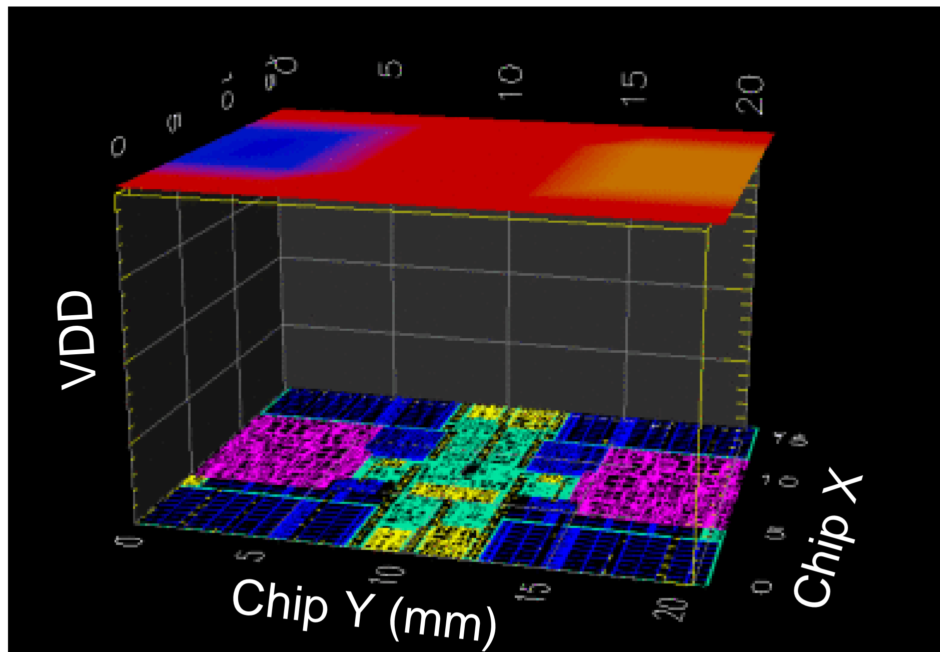
R. Gordin et al., "Design and Modeling Methodology of Vertical Interconnects for 3DI Applications", IEEE Transactions on Components, Packaging and Manufacturing Technology



TSV + μ-bump S-parameters

© 2011 IBM Corporation

Noise Traveling Across Chip (Connected cores)



P. Restle ISSCC 2007

- Decoupling today is mostly an afterthought but Transient voltage droops due switching activity is a serious problem
- Planar Caps are large and leak tremendously
- So we cannot isolate this noise and must increase power supply to overcome
- Can be a serious issue in high performance multi-core applications

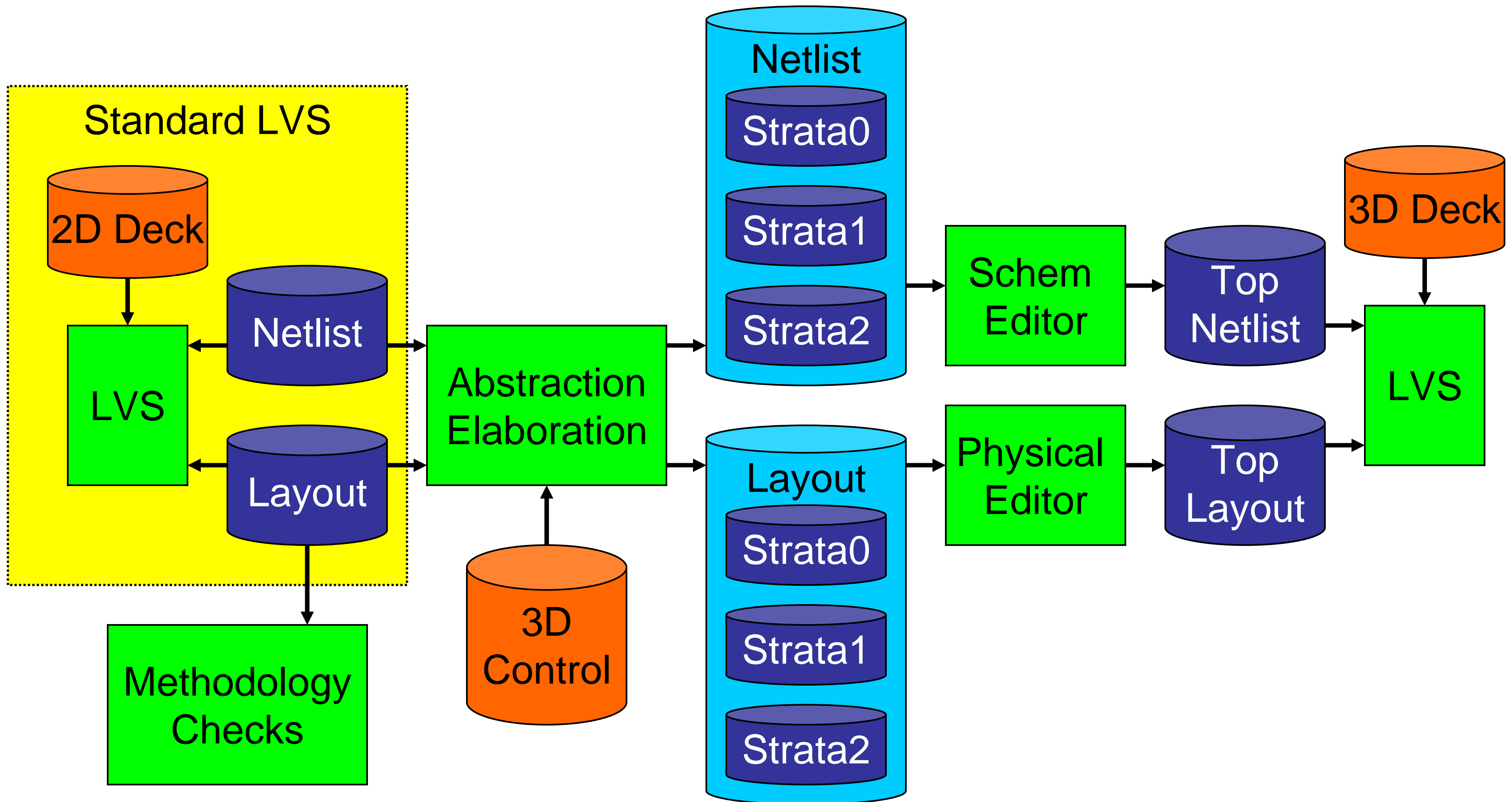
© 2011 IBM Corporation

3D LVS Checking

- **LVS compare against real schematic view**
- **Manipulate and View 3D Layers in Physical Editor**
- **Maximize Re-Use of known, Industry LVS tools**
- **Multiple Strata, Chips and Orientations**
  - Face to Face, Face to Back, Inter Poser and Hybrid Chips

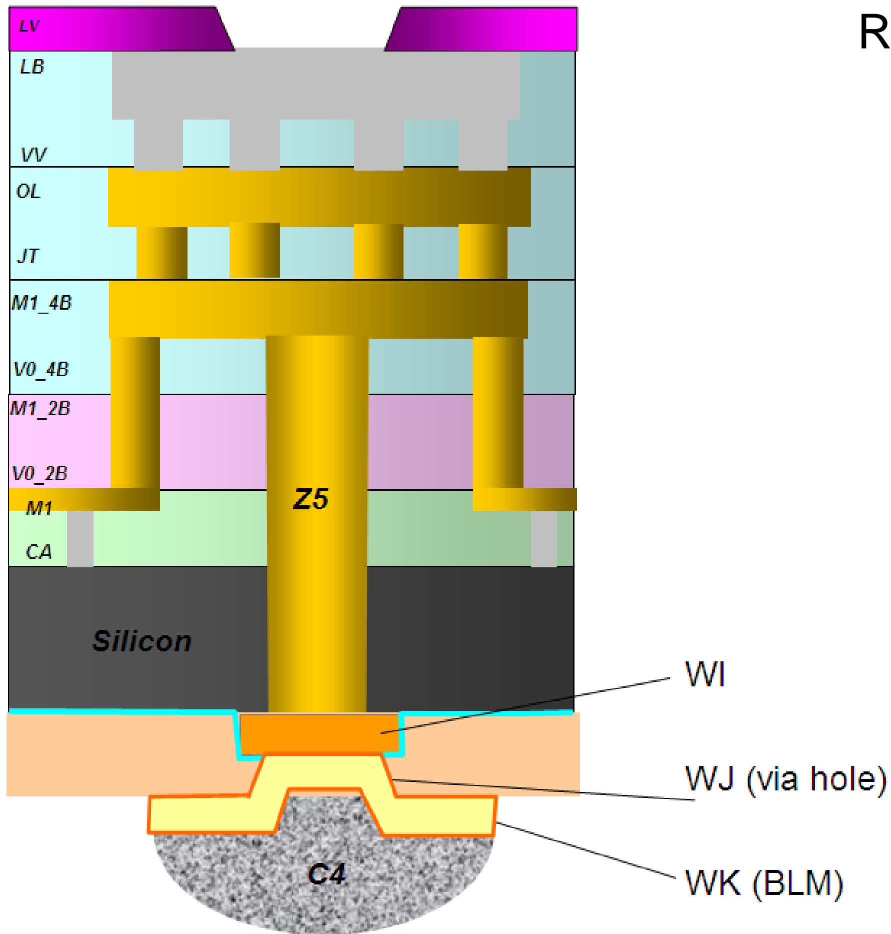
© 2011 IBM Corporation

3D LVS Flow

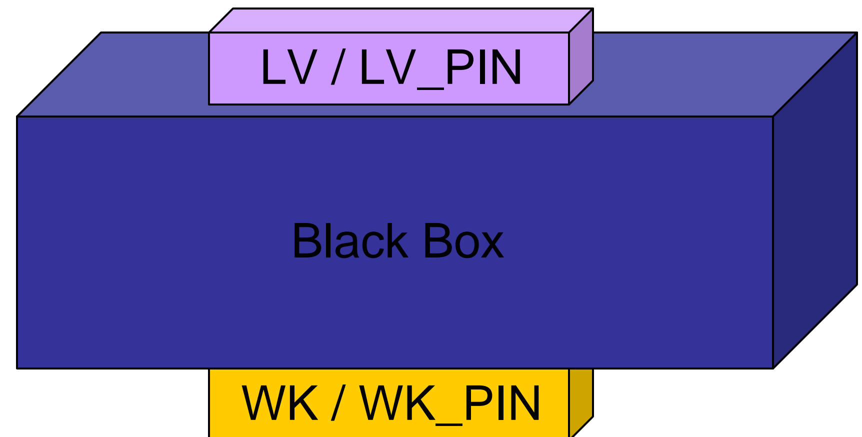


© 2011 IBM Corporation

3D Abstraction



Remove as many layers as possible



© 2011 IBM Corporation

3D Layout Assembly

- **Import Elaborated 3D Data**
- **Build top cell**
  – Place all instances
  – Align
  – Mirror / rotate as appropriate
- **3D DRC to check alignment**

© 2011 IBM Corporation

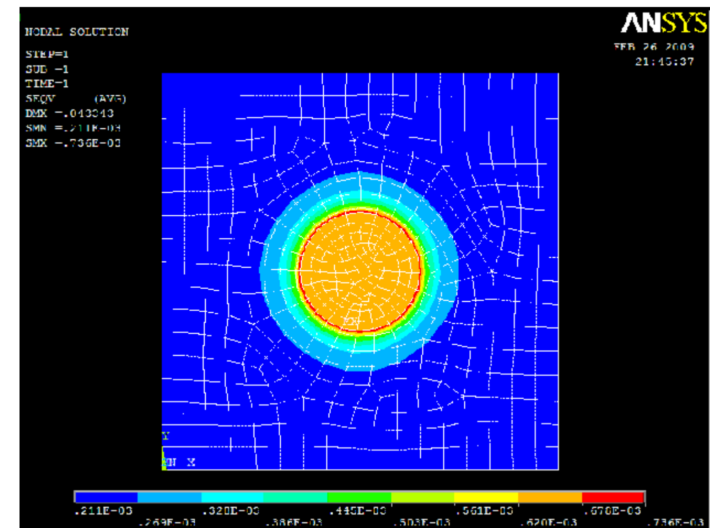
Working Prototype

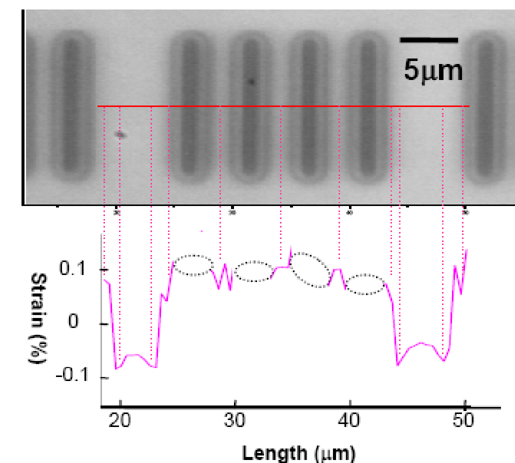
```
Device/Net Summary:

Schematic     Layout     Schematic     Layout
Matched       Matched    Unmatched     Unmatched
---------     -------    ---------     ---------
1             1          0             0            3d_test_S0
1             1          0             0            3d_test_S1
---------     -------    ---------     ---------
2             2          0             0            Total Devices

3             3          0             0            Total Nets

END Device/Net Summary

<> Cell 3d_test_top is Okay! <>
//End Cell//

++++++++++++++++++++++++++++
```


© 2011 IBM Corporation

TSV Keep out areas

- **Wiring Constraints**
- **TSVs punch holes in expensive Silicon**
- **Stress field from TSV can extend one characteristic dimension from TSV**
- **ESD with TSVs ?**
  – Chip to Chip vs Off-Package
- **Standard DRC works**
  – Level Grouping makes Coding easier i.e. All Levels minus TSV levels
- **Extraction Needs More Global Awareness**



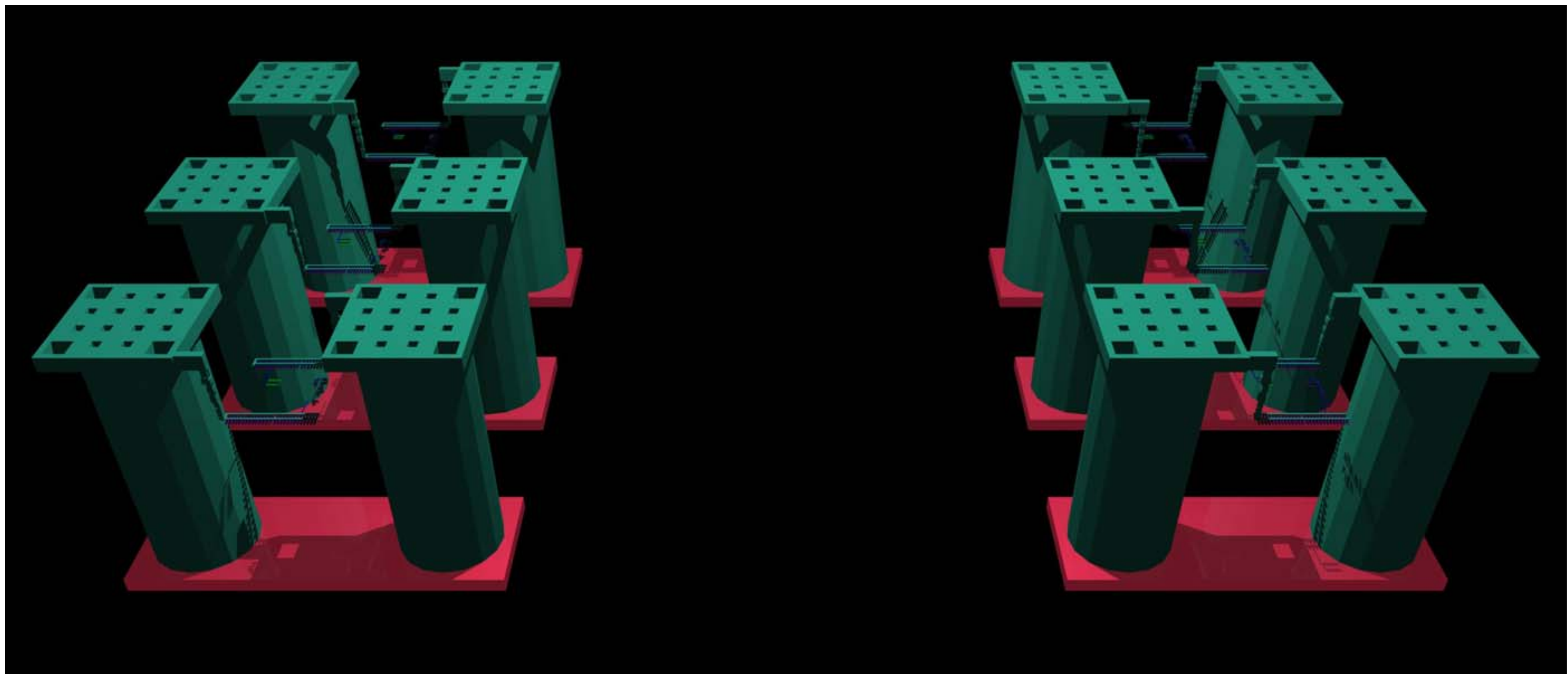


Liu *et al*

© 2011 IBM Corporation

Visualization

- Multi-Level Designs can be difficult to visualize without automation assistance
- Need Standardized Technology Description format (Film Thickness, Z Offset)



Todd Weaver / Jack Golz - 2010

© 2011 IBM Corporation

Closing remarks

- **3D is here, Multiple applications exists**
- **Design Automation Required**
- **Many 2D tools can be re-mapped**
- **Need larger capacity to enable Full 3D**
- **Need Extensions to improve enablement**
- **As Always …**
  Need Standards to enable tool inter-operability and new tool insertion

© 2011 IBM Corporation

Acknowledgement

Thank you to my many colleagues in IBM Research and IBM Systems and Technology Group for their collaboration and contributions, specifically Subu Iyer, Jeff Burns and Pat Williams.

© 2011 IBM Corporation