



ATRENTA®

3D Planning Solution

GSA-SI2 3D Workshop

Oct 1, 2009



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The Move Towards 3D IC's

■ Issues with 2D IC design (performance and TAT)

- Performance is dominated by interconnects in DSM technologies – Moore's law hitting a brick wall at 40 nm and below
- Need for migration of legacy IPs into new processes

■ 3D IC's are one way to solve the problem

- Performance improvements of up-to 60% by transferring floor-planning and placement from 2D to 3D
- Eliminate long wires – faster, smaller, fewer repeaters, lower power and less congestion
- Heterogeneous integration of different technologies on a single chip
 - Different components such as digital, analog, memory, RF and different technologies on a single stack
- Prolongs Moore's law momentum

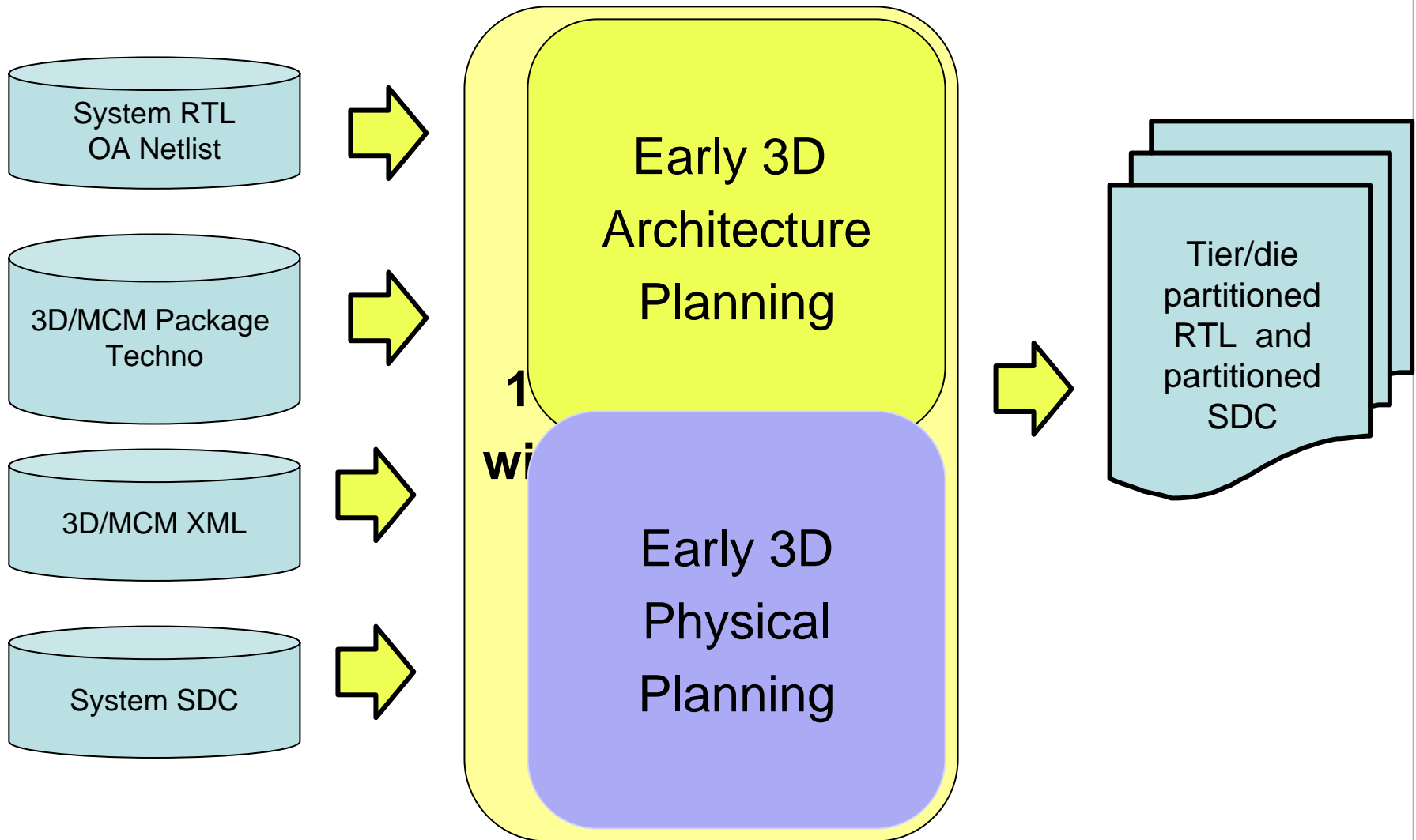
Advantages of 3D ICs

- **Heterogeneous integration of different process technologies**
 - Shorter TAT – no need to migrate legacy blocks to newer process
- **Improved performance**
 - Reduction in interconnect delay – better timing
 - Reduction of wire length – reduced capacitive power (lower power)
 - Increased Integration density (smaller die size)

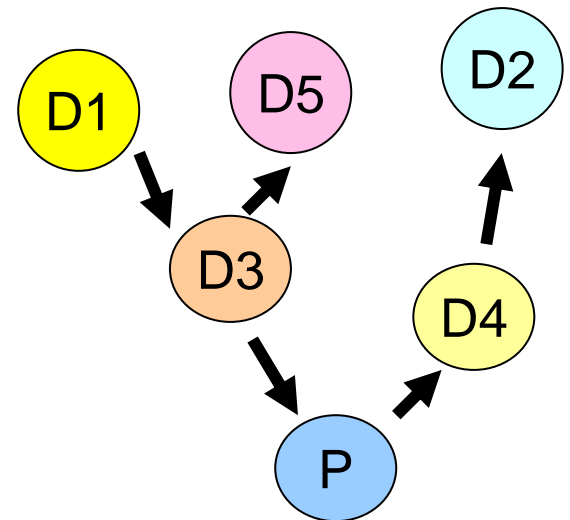
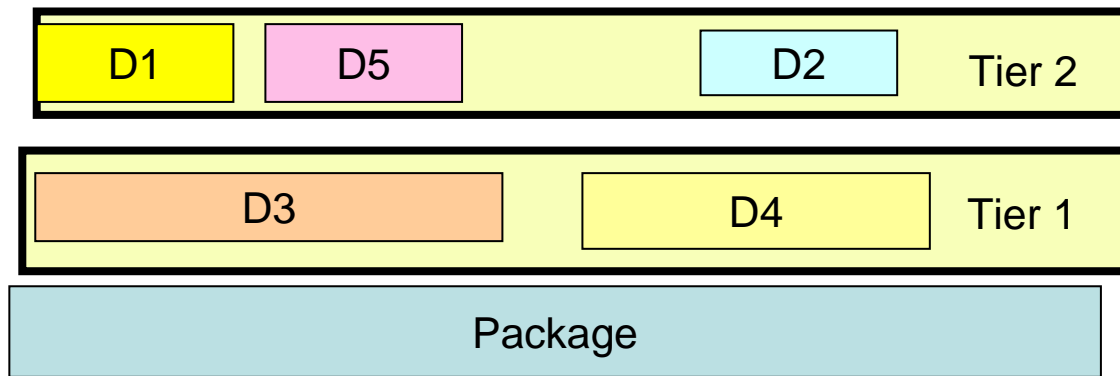
Main Issues with 3D Design

- **Through silicon vias (TSV) for interconnect between layers**
 - Significantly larger than normal vias
- **Increased density of devices (overlapping layers) leads to increased power consumption**
- **Increased heat dissipation due to increased power consumption and poor conductivity of the insulating layer between the active layers**
- **Management of heat dissipation by the introduction of special heat sinks (thermal vias)**
- **Thermal aware floor-planning, placement and routing**
- **All design planning and analysis tools (area, timing, congestion, power) should be 3D aware**

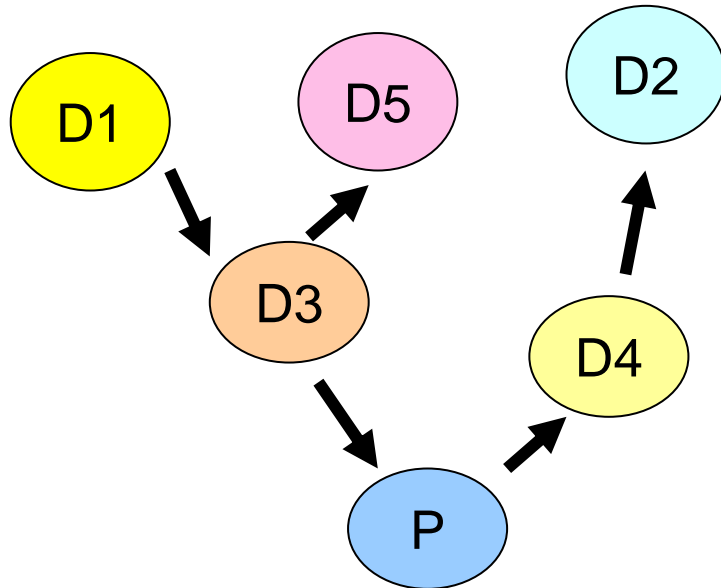
3D Planning And Assembly Solution



3D Planning Cockpit



3D Planning



- Allow user guided partitioning of IPs to different tiers/dies
- User customized cost function calculator for the different scenarios
- Drag and drop of IPs across different tier/die to – Dynamic updates of cost function to support efficient what-if's
- Understand the “true” cost of connection – for e.g. a D1 to D2 will have to go through D3, package, and D4, similarly a D1 to D5 connection will have to utilize D3
- Write out partitioned hierarchy and partitioned constraints

3D – Need for Standards

- **3D Inter-Tier technology information**
 - TSV's, Pillar Bumps, Package Info
 - Cost Metrics
 - Area, Timing, Power Modeling
- **Early stage modeling and estimation of thermal effects – aid in better “PathFinding”**
- **3D Tier/Package Info – XML? How do you pass information to downstream implementation tools?**



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Thank you!

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