

TSV based 3D integration:

Mentor's Verification Solution and Requirements for Standards

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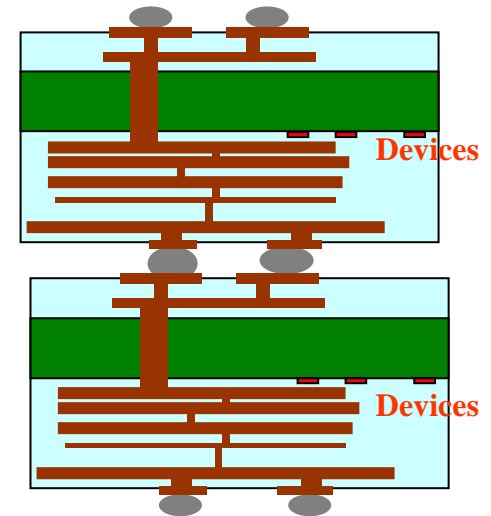
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Mentor's Response to 3D EDA Challenges

- **Objective**
 - Provide production quality stacked chip verification solution for Calibre customers
 - Deliver functionality for 3D system verification in phases
- **Internal investigation and prioritization**
 - 3D Verification was natural first step
 - Analysis tools to investigate Impact of new phenomena (electrical, mechanical, thermal)
- **Collaboration**
 - Design houses
 - Foundries
 - Universities
- **Evolutionary development**
 - Roadmap defined
 - Big EDAs are unlikely to develop radically new solutions; Extension and incremental modification of existing 2D methodologies and tools to minimize complexity for designers

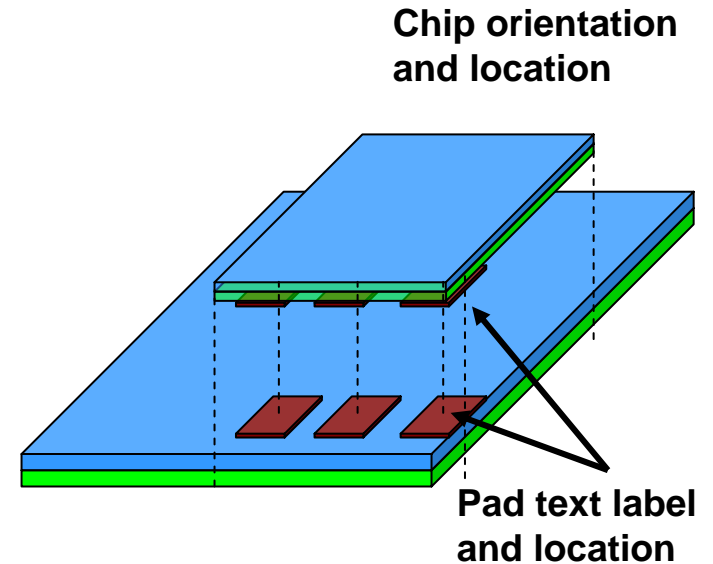
Mentor's Verification Solution

- LVS, DRC, Extraction with limited awareness of other dies
- DRC/LVS of the whole double sided die stack including TSV, backside metal, micro-bumps locations of other dies
- TSV as LVS Device;
Spice model of arbitrary complexity used for TSV device in simulation
- Double sided die metal stacks specification in mipt and double sided die calibration
- Double sided die front (regular) and back metal extraction
- Single net-list for double sided die including front metal parasitics, TSV and back metal parasitics.

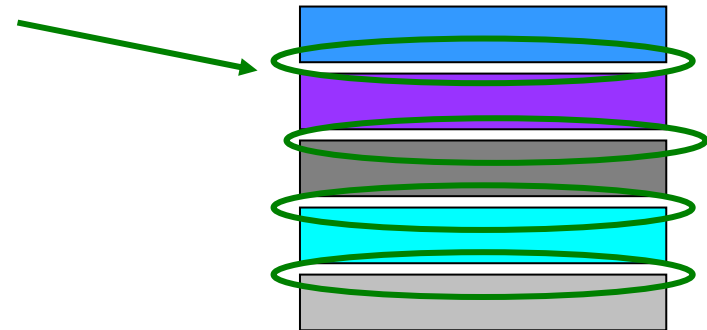


Multiple-die Stacks

- Reading two GDS files and checking connectivity using text ports at micro-bump/pad locations

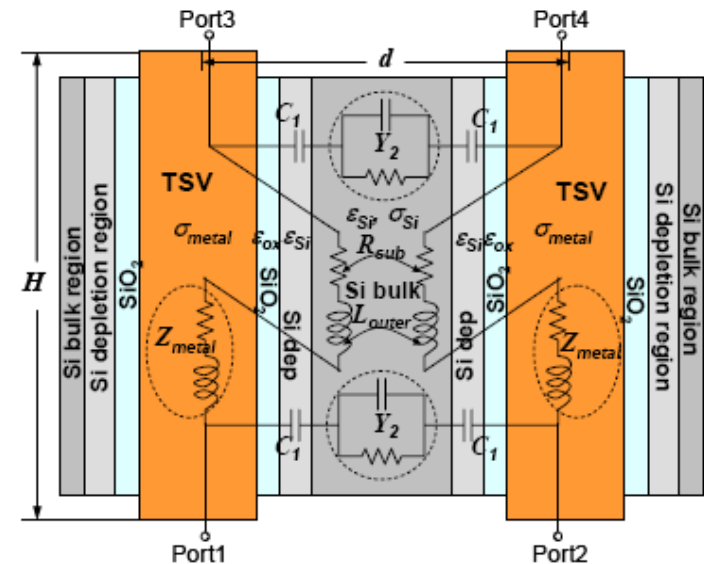
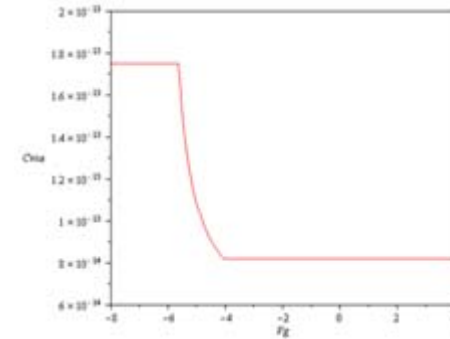
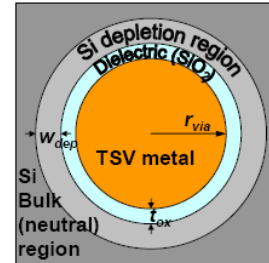


- Multiple dies can be verified by considering the pairs of neighboring dies and their interface individually (as above)



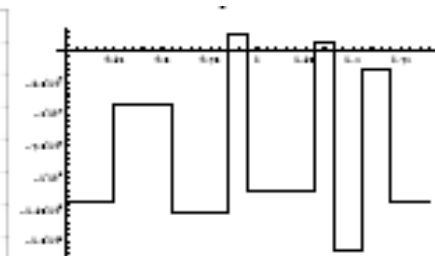
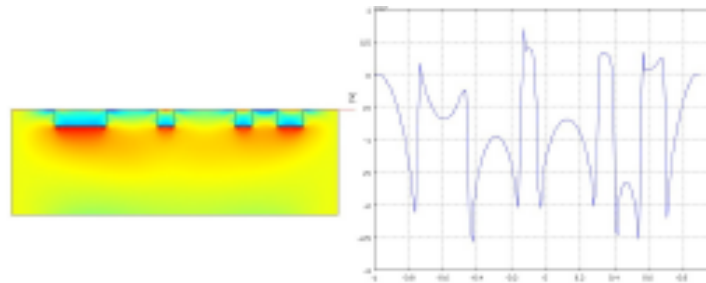
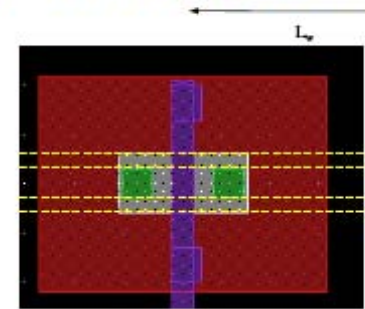
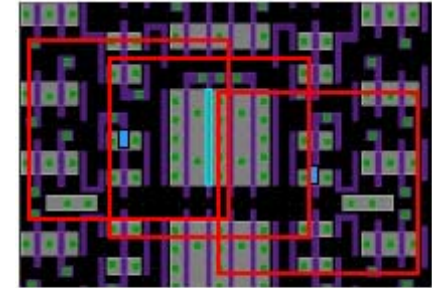
TSV Modeling Issues

- Lumped models are not sufficient
- Should model:
MOS effect in silicon, AC conduction in silicon, skin effect, eddy currents in silicon substrate,...
- Compact models for TSVs
- Full 3D EM model for modeling high density TSVs and their interactions



Impact of Global Stress Load on Electrical Performance

- Mentor graphics has developed a prototype of the full-chip EDA tool which provides capability to account for a global stress load caused by TSVs, bumps, silicon thinning,...
- Prototype generates the stress distribution using approximate analytical solution (compact models)
- Developed calibration module transforms simulated stress into the transistor characteristics by introducing a number of parameters into the annotated SPICE netlist



Requirements for Standards

- Standards are useful in processes, materials, modeling , interfaces, flows, ... but should not slow down further innovation and development in those areas
- Standards needed for interface with foundry data and downstream simulation tools
- TSV Modeling
 - Format of compact model, for various flows
 - Standard set of parameters for material properties and geometry
 - Interactions with other TSVs and devices
- Chip Stacking
 - Die stack information and die to die interface information
 - Location, shape and size of connection points
 - Model for chip interfaces (bumps , pads)
- Stress
 - Major material parameters (Young's modulus, Poisson factors, thermal expansion coefficients, etc) should be passed to the model in standard form
 - Strain distribution caused by the global load is an additional input to the compact model of layout-dependent (intentional/unintentional) stress
 - Calculated and calibrated stress variation should be converted into instance parameters (MULU0, DELVTH0, etc) that offset model elements and modify the spice netlis

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