

Prototyping in 3D-ICs: Design Flow Needs

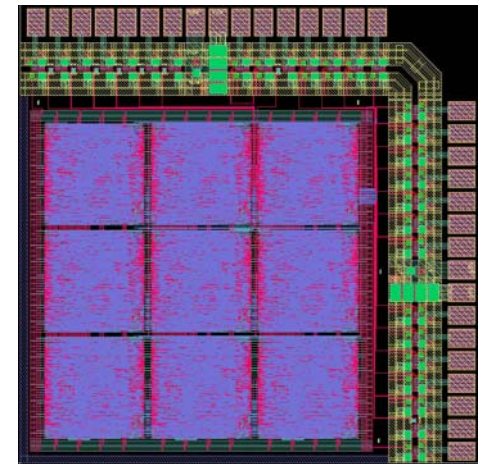
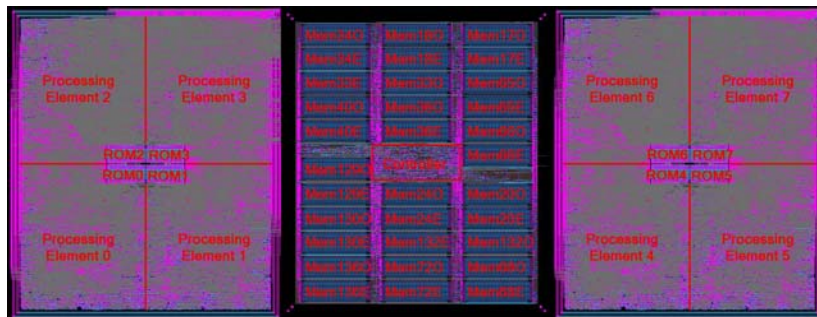
W. Rhett Davis
North Carolina State University
rhett_davis@ncsu.edu

*Si2-GSA Workshop on Requirements
for 3D Design Flow Interoperability Standards
October 1, 2009*

My Background

- DARPA 3DIC Project – July '04 – Aug. '09
 - » 3D LEF/DEF Standard & OA Extension Spec. available
- CAD Support for MPW Runs
 - » MITLL 3-tier, 180nm FD-SOI (2005, 2006, 2008)
 - » Tezzaron 2-tier, 130nm Bulk (2009)
 - » Predictive Design Kits (SRC Project)

Thorolfsson
& Franzon,
3D-SAR



Mineo & Davis,
3D-NoC, CICC'08

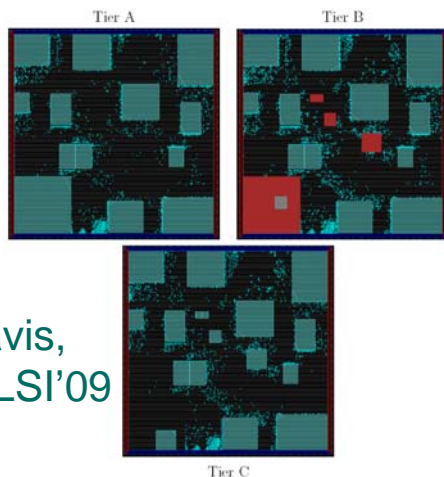
- Best Designs to date
 - » 3D NoC chip, 360K transistors (see CICC 2008 paper)
 - » 3D SAR chip w/ Paul Franzon (in fab)

Issue #1: Layer Representation

- 1 identifier
e.g. layer “M1_A”
 - » (+) Works well with existing EDA tools
 - » (-) Leads to further expansion of technology information
 - » (-) 3D Integrators take on more risk
 - » (e.g. our PDKs)
- 2 identifiers
e.g. layer “M1”, tier “A”
 - » (+) Much simpler PDK
 - » (+) Reduced risk for 3D Integrator
 - » (-) Requires re-write of existing EDA tools
 - » (e.g. R3Logic’s Max3D)
- Solution – Mapping between the two in data model
- OA Extensions needed for “2 identifier approach”
 - » Instances: need to specify the tier and constraints on allowed tiers
 - » Vias: should represent as combinations of vias in different techs.

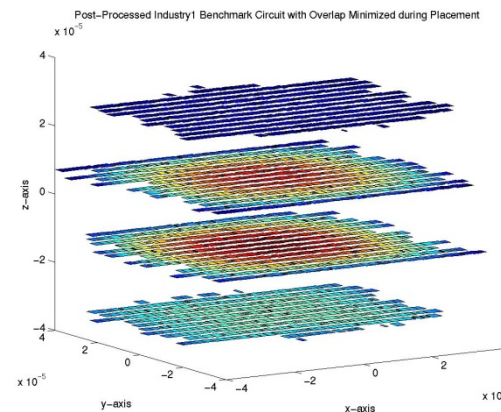
Issue #2: Partitioning & Placement

- Our approach:
 - » TSV's represented as standard cells
 - » Step 1: Partition
 - » Step 2: Floorplan & Place on middle tier
 - » Step 3: Constrain TSV placements on other tiers before placement
 - » Approach favored by Industry



Sule & Davis,
3D-FFT, TVLSI'09

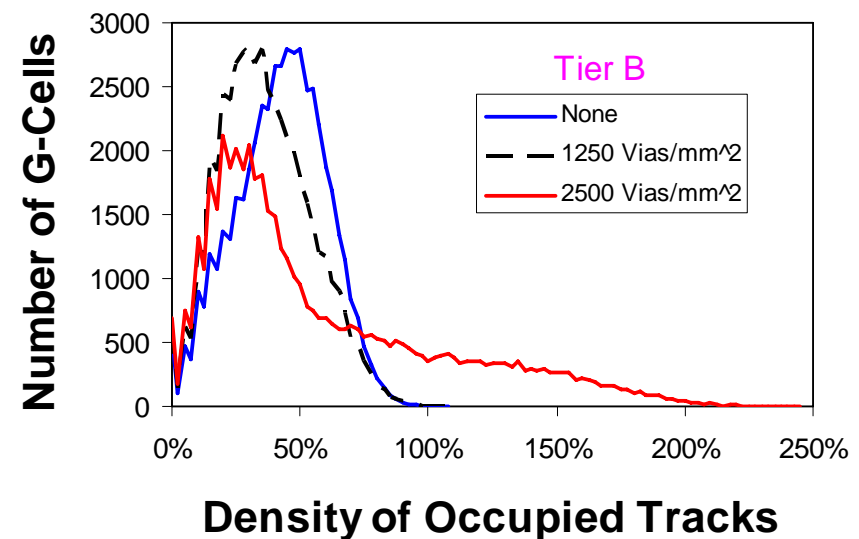
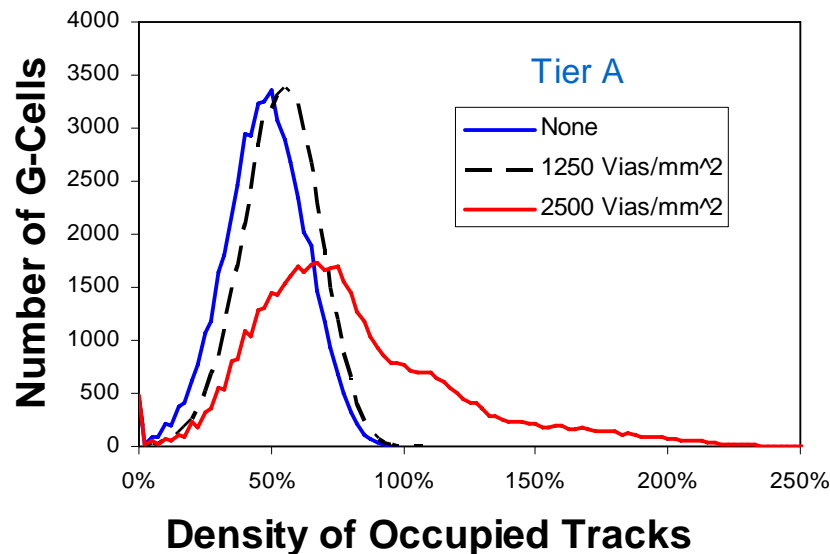
- Others' approach (Sapatnekar, UMN, 3D ADOpt)
 - » Partitioning & near-optimal placement done in one step
 - » Input & Output represented with multiple DEF files
 - » Approach favored by academia



Sapatnekar (UMN)
3D ADOpt, 2009

Issue #3: Congestion Analysis

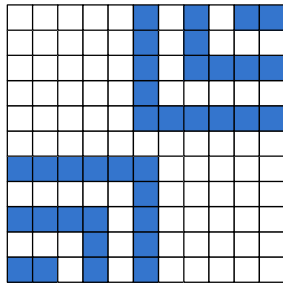
- Need Global routers and congestion analysis that can easily work with a variety of TSV options
- Example: design with 250 TSVs/mm² in MITLL 3-Tier process
 - » Design becomes unroutable with more than 2500 “thermal” TSVs/mm²



Hua & Davis, 2006

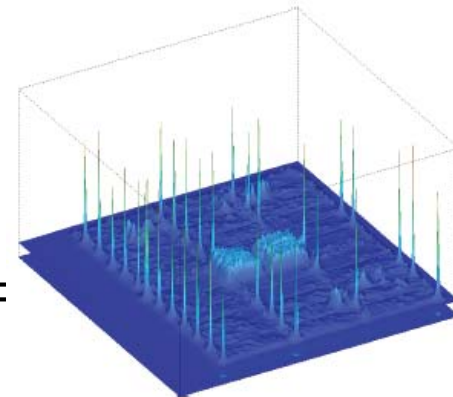
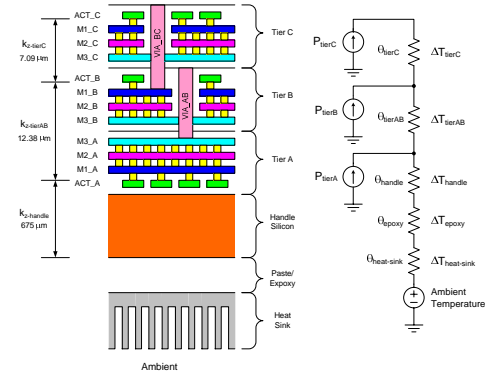
Issue #4: Thermal Analysis

- “1D” Analysis good for global average temperature prediction
 - » Need thicknesses, heights, thermal conductivities for tiers in Techfile



- Detailed hot-spot analysis depends heavily on metalization, substrate, bonding (Franzon et al, DAC'08)
 - » “Average conductivity” approach can over-predict spreading by up to 100X

- Commercial Tools (e.g. Gradient) can provide very detailed analysis in a couple of hours (Melamed, Davis, 3D-SIC'09)
 - » In addition to above, also need integration with Power Intent (CPF/UPF in Data Model to improve usability



Issue #5: TSV Characterization

- Capacitance extraction works reasonably well
 - » Calibre xRC caps were ~30% larger than Ansoft Q3D caps in our experiments
- Biggest issues in parasitic extraction
 - » Coupling to many more layers, much longer run times (10X to 15X in our trials)
 - » Coupling to conductive planes above & below leads to convergence problems in field solvers.

