



Si2-GSA Workshop on Requirements for 3D Design Flow Interoperability Standards

Sumit DasGupta

Sr. Vice President, Engineering

Silicon Integration Initiative (Si2)

Herb Reiter

Chair, EDA/Design Advisory Panel

Global Semiconductor Alliance (GSA)

Interoperability – Standards – Collaborative Technology

Innovation Through Collaboration





About Si2

- **Si2 Mission**
 - Improve *interoperability* and *integration* across silicon design flows (Includes integration with manufacturing)
- **Membership**
 - 95 corporate members (37% user, 16% system, 47% EDA)
- **Philosophy**
 - Collaborative approach to delivering customer-centric, business focused solutions leveraging strong supplier partnerships
- **Projects**
 - OpenAccess: Open, industry-standard API & Reference Implementation with significant collateral for rapid adoption
 - Open Modeling: Standard interfaces to support characterization and modeling for analysis tools and DFM
 - DFM: Standard interfaces between design and manufacturing to support DFM
 - Low Power: Flow-based standards (incl. CPF) to support low-power design flows
 - **3D Design: Natural next step, design flow-based standards based on customer/member request**



Workshop Goals

- Accelerate adoption of 3D/TSV technology by establishing STANDARDS for Design, Modeling, and Manufacturability
- Specific focus on following topics:
 - Define key interfaces in design flows where standards will facilitate 3D design and manufacturing
 - Enlist participating standards organizations and EDA & user companies
 - Enlist likely early adopters among the IC design and manufacturing companies
 - Identify areas that do not require attention, i.e., standards exist or others are working on them
 - Engage academics already pursuing 3D R&D efforts, with interested industry players for very specific projects





Workshop Demographics

- > 40 organizations/companies present
- Representation from end-user, EDA, IP, foundry, IDM, and system companies



Workshop Agenda

- 09:00am - 09:20am: Introductory remarks from Si2 & GSA
- 09:20am - 12:00pm: Presentations by invited speakers
Order of presentations:
 1. IMEC, SPIRIT, SEMI
 2. IBM, Qualcomm, ST, SUN, Xilinx
 3. NC State, PRC – Ga.Tech.
 4. Atrenta, Cadence, Gradient, Magma, Mentor, R3 Logic, Synopsys
- 12:00pm – 01:00pm: Working lunch (cover spillover from above)
- 01:00pm – 03:00pm: Discussion/consolidation of standards recommendations
- 03:00pm – 04:00pm: Alignment, prioritization of requirements, follow-up AI's
Concluding remarks