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3D (TSV) IC Standardization Insights

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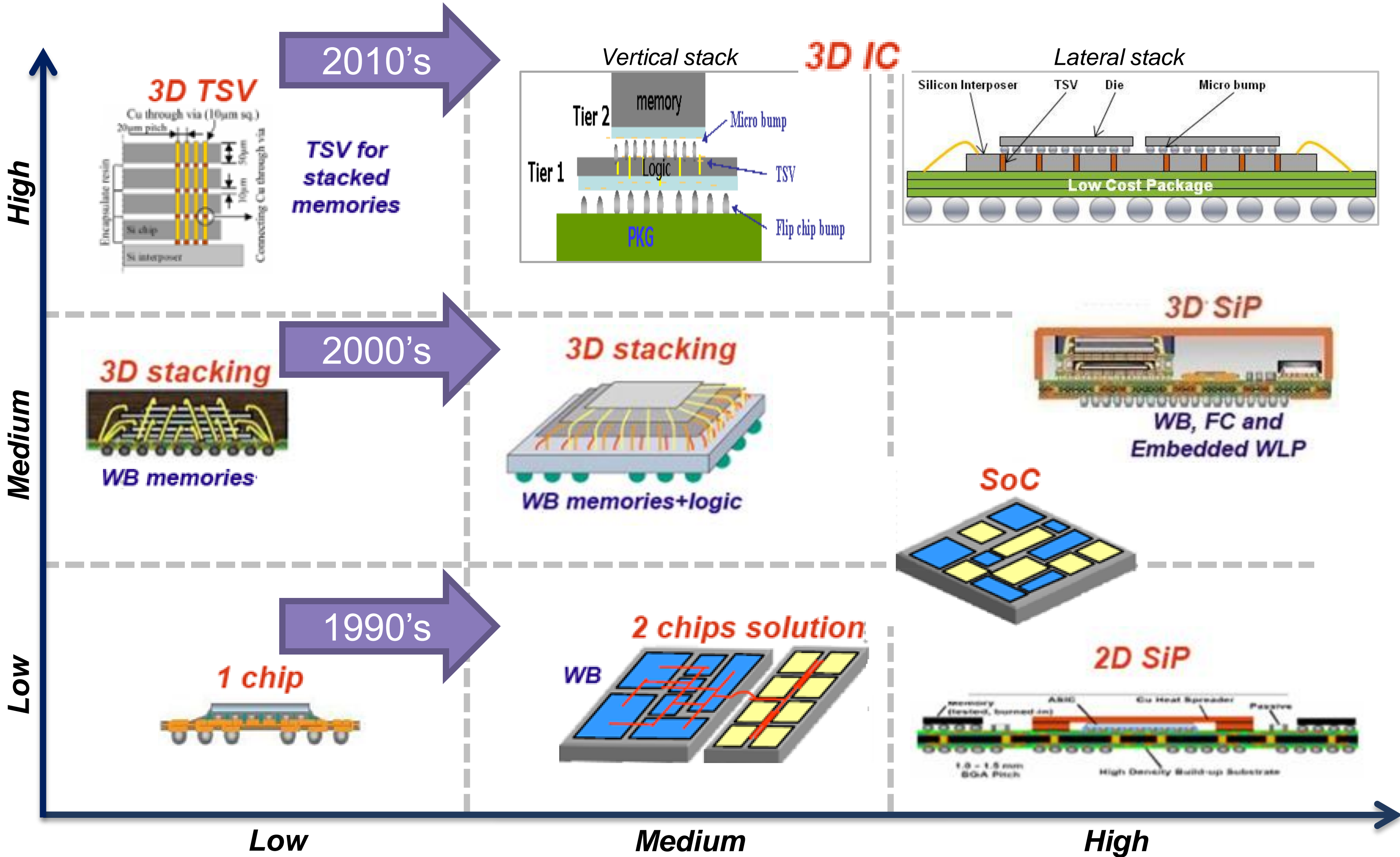
3D TSV Is An Emerging Technology

Packaging Technology Evolution



*Source: Yole Development, 2008

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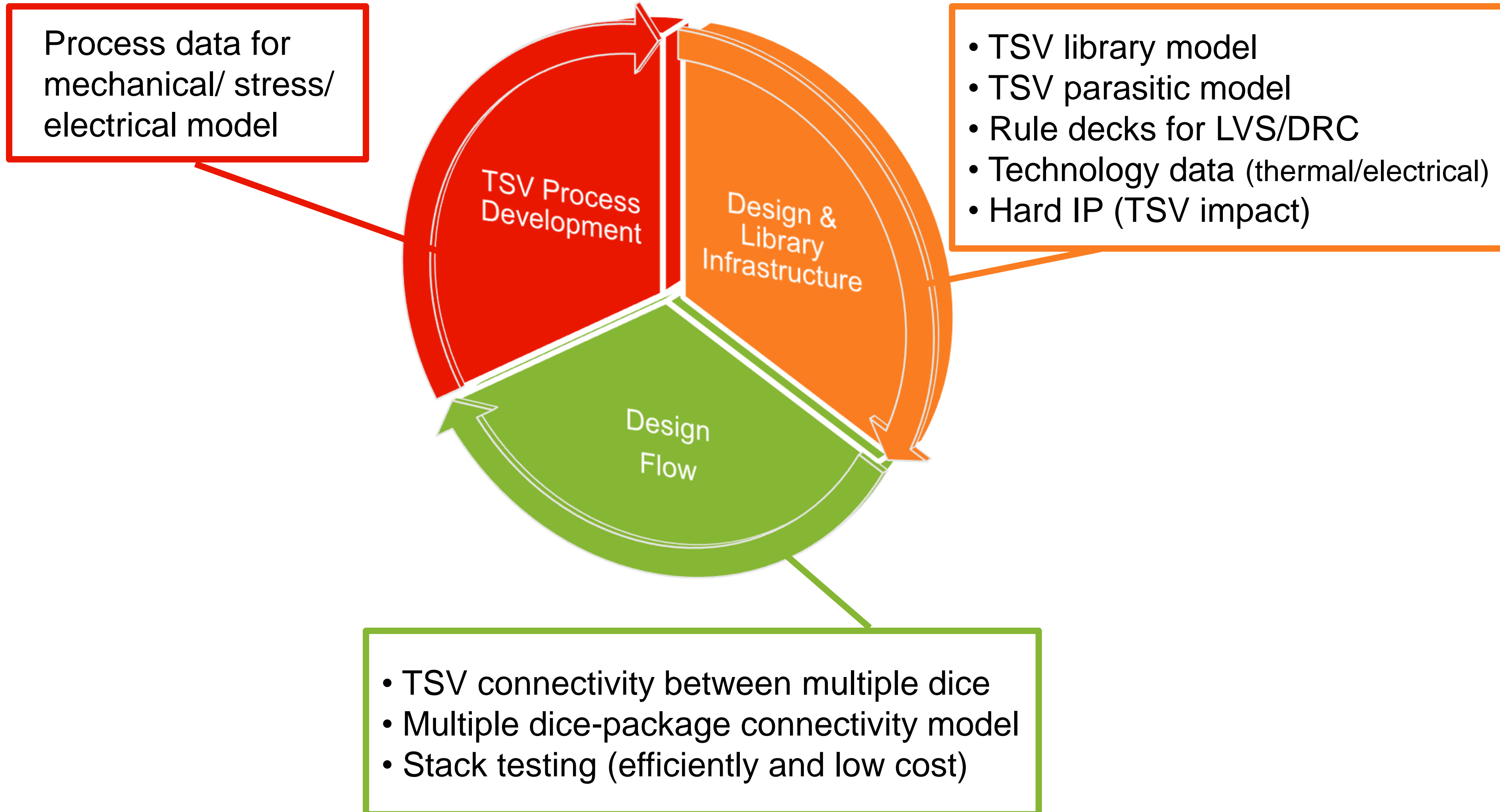
3D (TSV) IC Standardization Landscape



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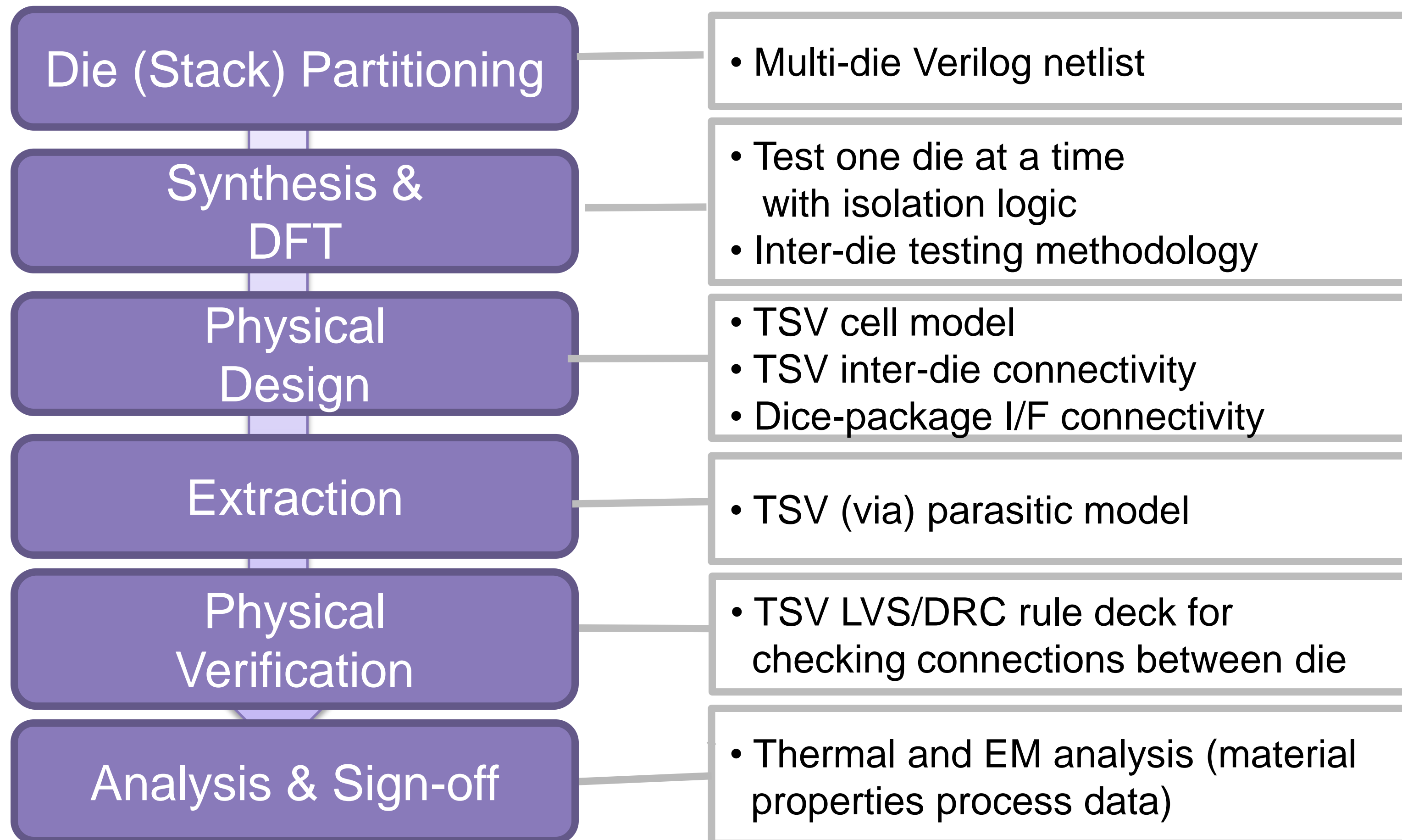
3D (TSV) IC Impact on EDA Design Flow



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3D (TSV) IC Standardization Options

Scope	Information	Current Use	Owner	Next Step
Cell Modeling	Library data	.lib/Liberty	IEEE-ISTO	Extend for TSV model
Test	Single & Inter-die testing methodology	IEEE 1149, 1500	IEEE	Extend IEEE standards
Physical Design	Inter-die connectivity	LEF/DEF	Si2	Create a 3D LEF/DEF
Package Design	Multidie-to-package interconnection	AIF BGAF Ad-hoc	Amkor Zuken Proprietary	Create a standard
Parasitic Extraction	Technology file	ITF	Synopsys	Extend ITF

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