



Si2-GSA 3D EDA Standards Workshop

October 1st

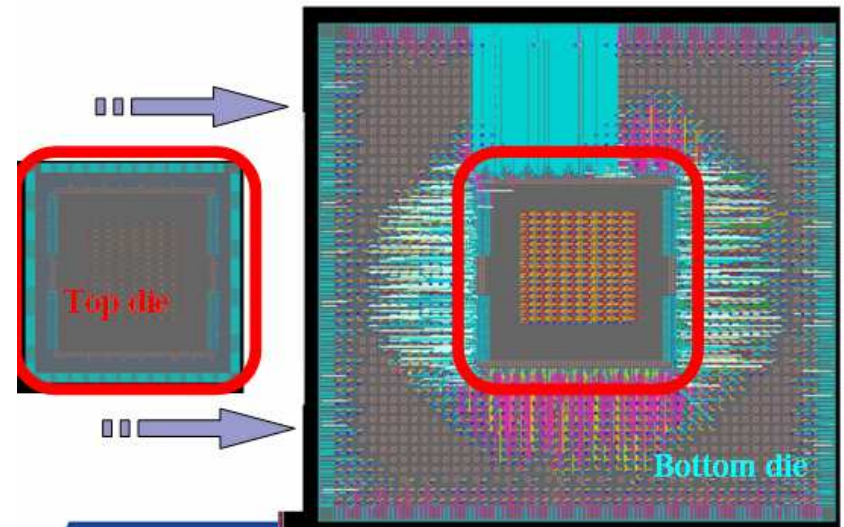
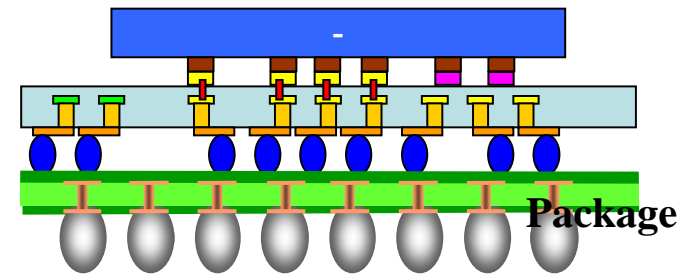


STMicroelectronics

Real case 3D Designs implementation analysis



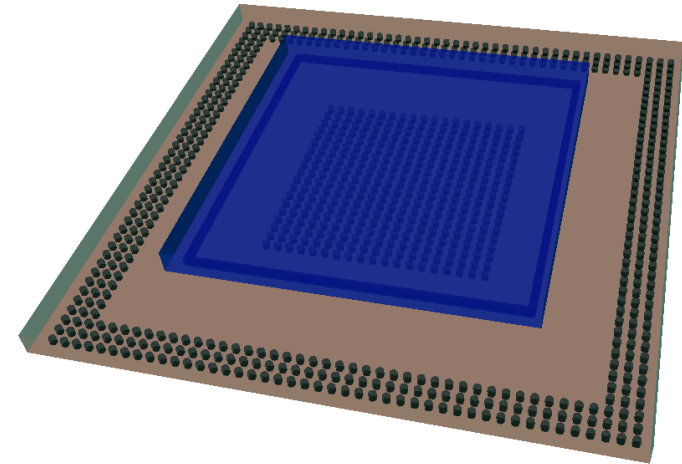
- F2F Digital Top/Bottom die
 - Use of TSV for bottom die
- System netlisting is a nightmare, need to be share between ICs/Package/LVS/Extraction tools
- Impact of package design is major on system design
 - Near to near constraint propagation from board to top die
 - Mandatory smooth link
- Physical database are not standardized exchange between tool is almost impossible
- 3D LVS is mandatory
- 3D netlisting of parasitic is mandatory for system simulation.



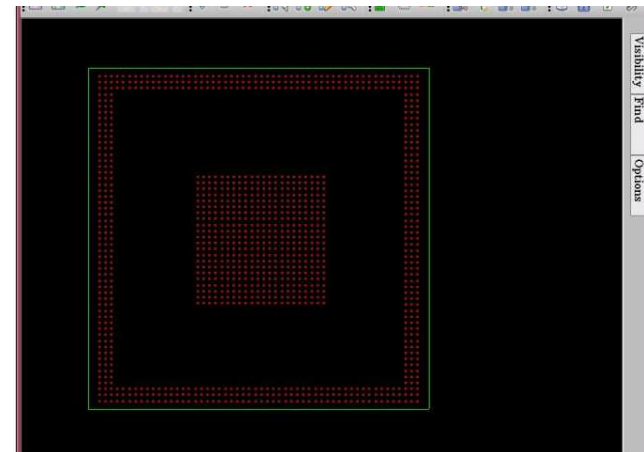
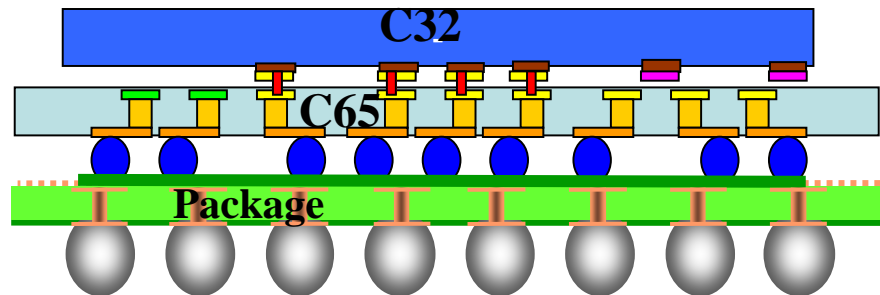
ICs-Package 3D co-design flow



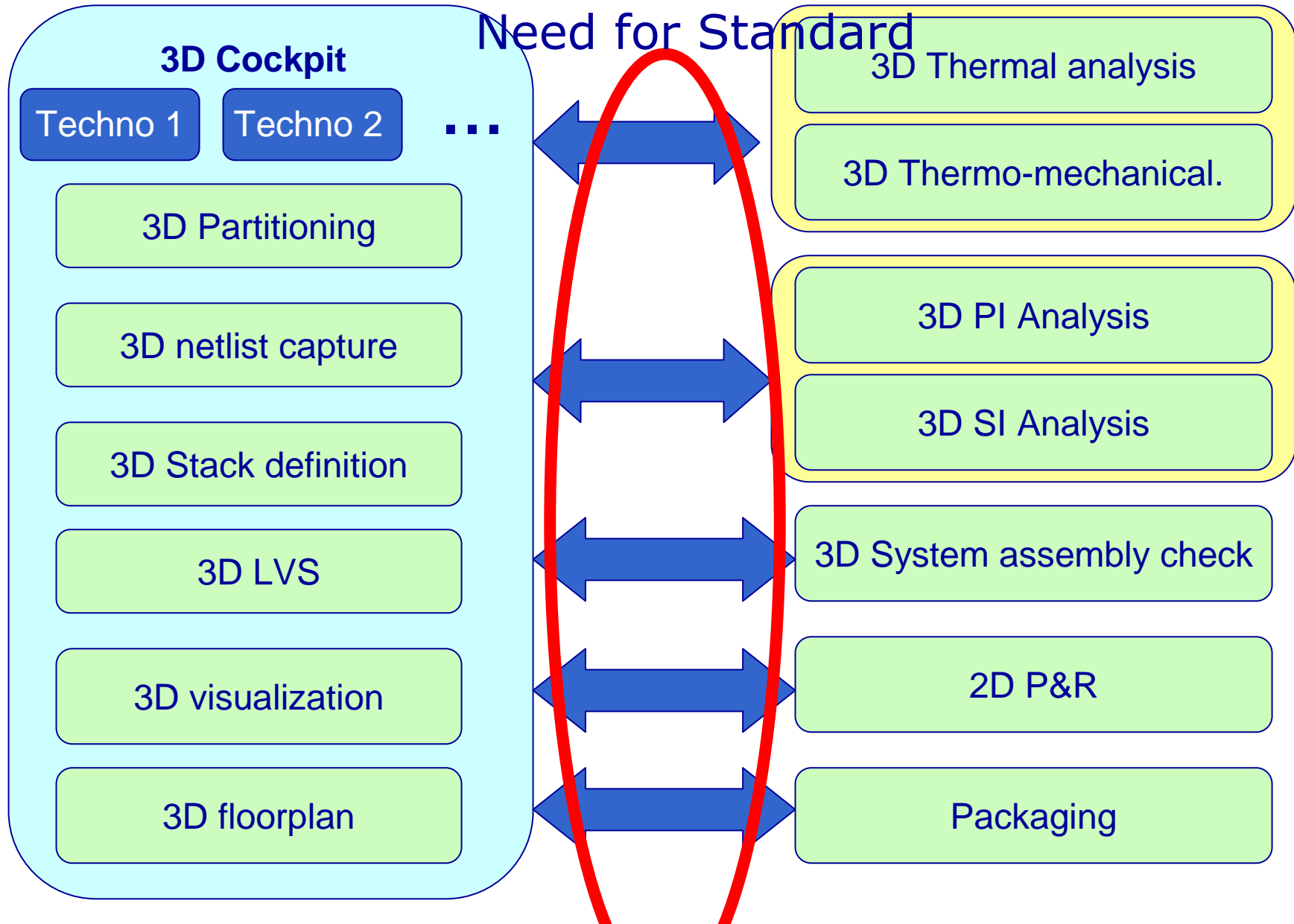
- need integrated IC-package link thru extension of existing SIP flow
 - Back-side bump management



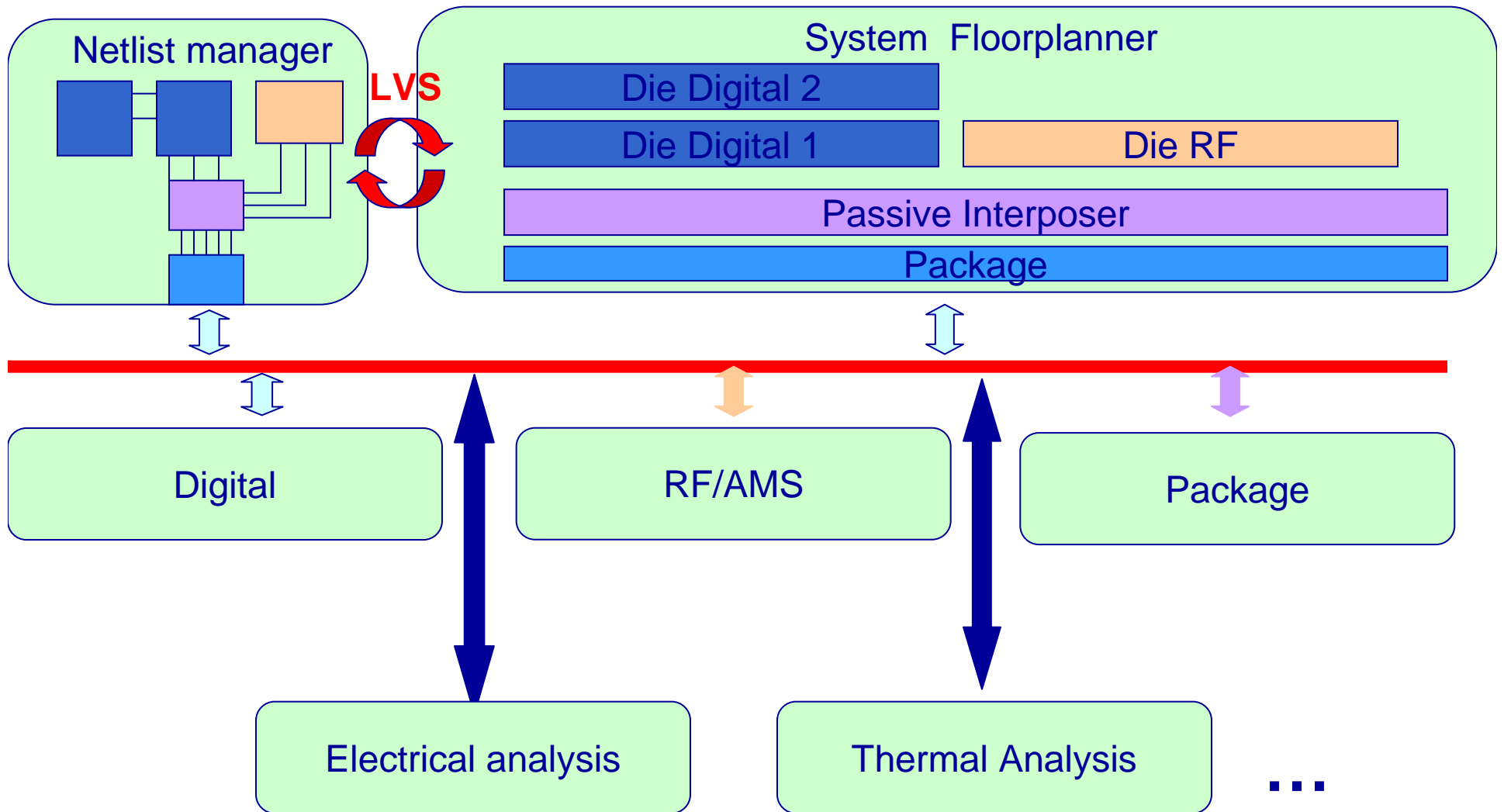
3D view of system in package tool



3D System flow organization target



Generic 3D Solution overview



Key item to be standardized



- 3D System netlist (Signal + power): IC(s) + Package + Board
- Stacking description (F2F, F2B, die offset)
- Interface between Die/Package/Board world
- TSV/Back-side geometry geometry description (LEF,DEF,OA)
 - TSV is Via
 - Purpose thermal, extraction, thermo mechanical