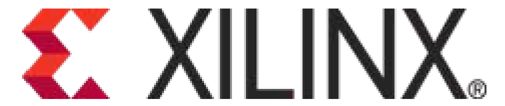


# Interoperable 3D IC Standards

**Arif Rahman**
**Xilinx, Inc.**

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# Outline

- **Background**
- **Scope of 3D IC Standard**
  - – Design
  - – Manufacturing
  - – SiP Integration and test
  - – Reliability
- **Summary**


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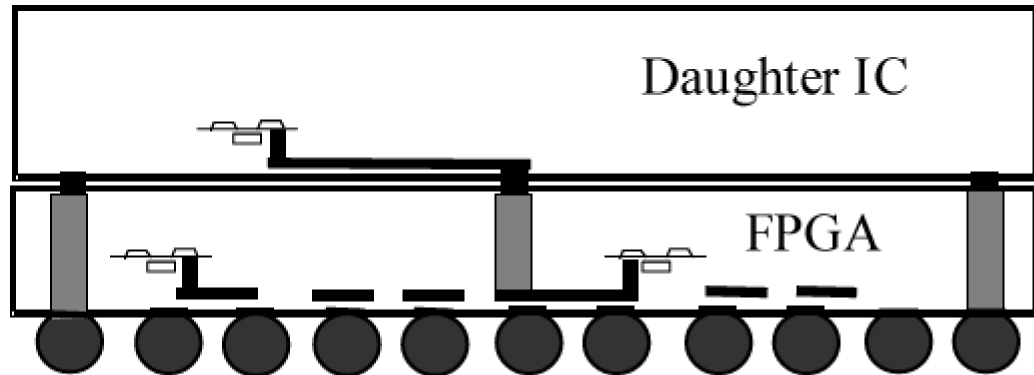
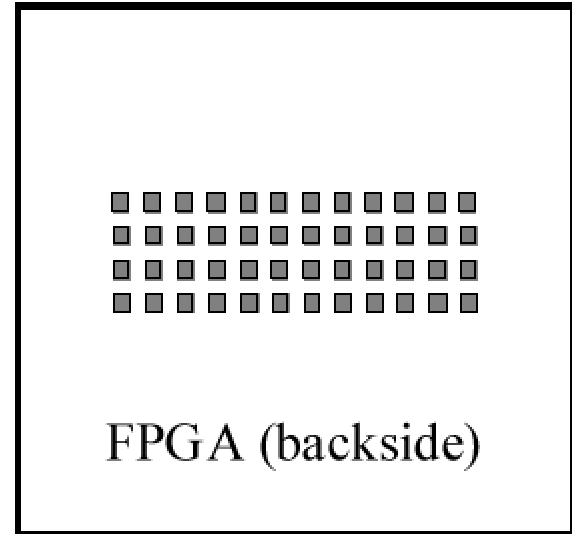
# Scope of 3D IC Standard for Stacked-Die SiP




- Heterogeneous integration
- Stacking-enabled chip design



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# Design

- **A generic physical design flow for heterogeneous integration**
- **Support for multiple technologies (i.e. techfiles)**
  - Viewing of databases from different technologies in Layout Editor
  - Single vs. multi-die DRC
  - Verification of chip-to-chip interface
  - LVS (single chip, multiple chips, black box, etc.)
  - Extraction support for different techfiles/technologies
- **Multi-Chip Electrical Analysis**
  - IR, signal integrity, EM, etc.
- **Compatibility of different CAD flows in diff. chips**
  - What to expose and what to abstract out
- **Ability to integrate PDKs from multiple manufacturers**
- **Floor-planning**


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# Manufacturing

- **Should reflect manufacturing requirements and constraints**
  - Via first, via middle, and via last (design rules)
  - Material standards
    - Interoperability of ICs
- **Physical attributes (die size, thickness, warpage, etc.)**
- **DFM rules**
  - Micro-bumps (dummy, corner/edge rules, etc.)
  - TSVs (AR, keep out, etc.)
  - Interoperability of ICs from different fabs


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# SiP Integration and Test

- **Physical specification**
  - Chip-to-chip contact spacing, pitch, and physical locations
  - Compatibility of alignment keys for bonding
- **Electrical specification of chip-to-chip drivers and receivers**
  - Signal types and voltage levels (signals, control, test, registered vs. non-registered, etc.)
  - Termination requirements
  - Performance attributes/models (IBIS model?)
  - ESD requirement
- **Functional specification**
  - Verification, debugging, and testing
- **Testing**
  - Scan chain & loopback
  - SiP testing


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# Reliability

- **Common lifetime and reliability criteria**
  – Monolithic vs. heterogeneous integration
- **Power delivery**
- **Power budget and thermal effects**
  – Cooling requirements
- **Design for reliability (DFR)**
  – EM for micro-bumps
  – Chip-package and package-board interaction
  – Redundancy (TSV & micro-bumps)
- **Die thickness**


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# Summary

| Scope of Standardization | Focus Areas |
|---|---|
| Physical Design | -Layout, DRC, LVS<br>-Extraction |
| Manufacturing | -DFM<br>-Materials & design specs |
| SiP Integration & Test | - Physical, logical, and functional specs of chip-to-chip interface |
| Reliability | - Lifetime/reliability criteria<br>- Design for reliability |

## Stakeholders

IDMs, Fabless, and EDA companies
Equipment Vendors
Fabs and OSATs


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