3D Ecosystem Panel

Moderated by:
Matt Nowak
Senior Director, Engineering – QCT Technology Development
QUALCOMM
3D TSV Types

Direct Through Silicon Stacking (TSS)

TSV Interposer

ASIC chip with TSVs

ASIC chip
High Density Through Silicon Stacking (TSS)

- Small diameter (~5um) high aspect ratio (~10:1) thru silicon via (TSV)
- Via-middle process flow (TSV formation after FEOL)
- Backside wafer interconnect processing
- High density (10’s um pitch) tier to tier microbump connections
- >1000’s of TSVs & microbumps per chip
- Includes design and test enablement, tools, & methodologies
Panelists

**Bill Chen**, Senior Technical Advisor
ASE Group

**Kyowon Jin**, Vice President, Product Planning,
Worldwide Marketing & Sales Division,
Hynix Semiconductor

**Paul Kempf**, Vice President, Silicon,
Research In Motion (RIM)

**Suk Lee**, Director, Design Infrastructure
Marketing Division, Design Technology Platform,
TSMC NA

**Dave Noice**, Fellow
Cadence Design Systems, Inc.
3D Ecosystem
An OSAT Perspective

Bill Chen
ASE Group

March 31, 2011
Opportunities for OSAT

• Everyone says 3D is the “best thing since sliced bread.”
  • We must close the distance between the bread maker, the deli counter, and the sandwich served on the dining table.
  • Whether it is BLT, Roast beef, or peanut butter & jelly, we must deliver our best to the customer.

• When TSV wafers roll out from the foundries in the very near future, the OSAT Supply Chain must be ready with cost effective assembly and test, with good yield and cycle time.
3D at ASE

- **Internal development since 2006**
  - 3D R&D process team: drawn from FC wafer bumping and FC assembly core teams
  - R&D process line: Middle end and advanced assembly technologies
  - Fundamentals team: electrical-mechanical-thermal modeling; surface analysis, materials characterization, process mechanics, build EM database

- **Collaborations & Joint projects since 2007**
  - Joint development projects: diverse applications
  - R&D consortiums and academic research: knowledge base supply chain
  - Partnerships: from 3D ecosystems to 3D villages and 3D neighborhoods: System House - ICs - foundries - SAT - EDA, Materials & Tools

- **Infrastructure investment - people and equipment**

- **Business Models and Technology Progress**
3D Technology Building Blocks Today

- D2D/ D2S w/ microbump and Cu pillar
- D2S warpage process w/ bond processes
- Materials: fine gap NCF pre-applied UF
- ELK wafer dicing
- Thin (bumped) wafer handling
- Test
- Metrology
3D Integration

- 3D IC Package Assembly
- 2.5D Silicon Interposer
- 3D MEMs & Sensor Assembly
- Heterogeneous Integration
Thank you

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3D Ecosystem Panel

Kyowin Jin
Motivated by Technological Benefits rather than Cost

High Priority on UWIO development for HPC & Graphics purposes

- **Computing**
  - High Capacity
  - Low Power

- **Graphics**
  - High Bandwidth
  - High Capacity

- **Mobile**
  - High Bandwidth
  - Low Power

2013 - 2014
Notable Achievements and Developments in Hynix

• Year 2011
  8GB 3DS-RDIMM Prototype

• Year 2011
  World No. 1 2Gbx8High 3DS-DDR3 Development

• Year 2013
  UWIO Product Development with “3D Ecosystem” collaboration
Prerequisites for “3D Ecosystem”
Well-defined responsibilities of each player

Improving yield of “logic + stacked DRAM combined” becomes more important than improving “DRAM only yield”
3D Ecosystem Panel

Paul Kempf
VP, Silicon
Research in Motion (RIM)
What Mobile Devices Need

- Unconstrained use cases
- Low power for mobility
- System architecture improvements

[Diagram showing memory bandwidth (GB/s) with years 2007 to 2015 and memory technologies like LPDDR1, LPDDR2, LPDDR3, Wide IO SDR, and Wide IO DDR]
What we care about

• Performance
  – Reduce memory bottleneck
  – Full system access

• Power consumption
  – Standby and active

• Height
  – Below 1.2mm with density up to 2GB
What I worry about

- Standards
  - Portability of system architecture
  - Meeting broad set of requirements

- Supply Chain
  - Delivery of 4 die stack without large cost multiplier
  - Ownership of stack with processor
  - Lead time
Evolution and 3DIC

Suk Lee
Director, Design Infrastructure Marketing Division
Industry Driven by Integration

- Silicon, Packaging, PCB, Packaging, all driven by opportunity for integration
- Functionality
- Form Factor
- Performance
- Power Consumption
- Cost
Revolution is...

- Exciting
- Painful
Silicon Interposer Delivers High Interconnect Density

Typical Interconnect Density (1/mm²)

- **Intra Die Level**: 1M
- **Inter Die Level**: 10K
- **Package Level**: 100
- **PCB Level**: 10

Silicon Interposer-Enabled
System Migration Trend

- Sub-micron level interconnect reduces parasitic load and power for data transmission
- Higher degree of integration reduces system form factor

![Diagram showing traditional, silicon interposer, and 3D integration of analog, RF, passive, logic, and memory components](image)
Silicon Interposer

- Silicon interposer uses silicon substrate with TSV to integrate multiple chips, enabling higher density interconnects

**Benefits**

- Enhanced system performance (higher bandwidth and lower power) via high density interconnect
- Less stress to ELK with buffered CTE mismatch
- Logic die partitioning for yield enhancement
- Lower-cost organic substrate
- TSV independent of technology node, decoupled from platform technology

![Silicon Interposer Diagram](image-url)
In summary...
3D Ecosystem Panel

Dave Noice
Fellow
Cadence Design Systems
3D-IC EDA Design Tools
Plan->Implement->Test->Verify

- 3D Stack Die Editor
- 3D Floorplan – Optimized power Plan and TSV/Bump locations
- TSV /Bump RDL Routing
- Virtuoso for custom shape editing
- 3D IR Drop Analysis
- 3D Thermal Maps
- IC-Package Co design flow
- Back-side Bump Management

Cadence 3D IC Flow
Developed in close partner-collaboration

Multiple 3D-IC tape outs

Memory over logic (28 nm), logic over analog, logic over logic, 3-stack dies, Silicon Interposer

Production design mid-2010 tape-out
Steps to Mainstream 3D IC

Drive Cost and Yield Improvements
  Volume success in memory market
  Prove Performance/Power/Price competitive advantage
  Prove success in consumer application segment
  Helps broaden investment in tools and technology

Ecosystem collaboration: Standards & Business models
  Virtual IDM: Foundry/OSAT model: who builds it? Who owns reliability/yield?
  Standards in technology, in Applications, in design & in handoff