3DIC Enablement Panel
How to enable building the 3D ecosystem
Dr. Gishi Chung, SrVP & GM, Tokyo Electron
Ron Huemoeller, SrVP, Amkor
Dr. Toru Ogawa, Director, TSMC
Fumiyasu Hirose, VP, Cadence
Dr. Subramanian Iyer, Fellow, IBM
Tim Whitfield, Director, ARM
Herb Reiter, Consultant, SEMATECH
Dr. Gishi Chung

Senior Vice President & General Manager
SPE Process Development Division, Tokyo Electron, Ltd.

Executive Vice President, Tokyo Electron Miyagi, Ltd.

Chairman, TEL Technology Center America, LLC
Tokyo Electron Product Line-up & World Market Share (FY2011)
Semiconductor Production Equipment

Coater/Developer
Plasma Etch System (total dry etch)
Thermal Processing System
Single Wafer Deposition System
Cleaning System
Wafer Prober

TEL Survey
TEL New Tools for 3DI formation

Wafer Bond

TSV formation

Center Edge

Wafer De-bond

Device wafer
Adhesive
Carrier wafer

Tactras™ FAVIAS
TSV Etcher

CLEAN TRACK ACT™ 12
3DI Patterning

TELINDY PLUS™ VDP
Dielectric liner deposition

Synapse™ V
Wafer Bonder

CELLESTA™-i
Cleaning

Trias™
Metallization

35um thickness wafer

Synapse™ Z
Wafer De-bonder

Gishi Chung/ Tokyo Electron Ltd./ April 16th, 2012
Memory Scaling and Integration with Logic for System Optimization

Ron Huemoeller
Senior Vice President, TSV
Amkor Technology, Inc.
Amkor’s Role in the 3D/2.5D Ecosystem

• **My Role:**
  - Direct all Business / Customer & Technology Platform Develop activity

• **BEOL Assembly**
  3D Vertical Stacking
  - Supporting development for Memory and Application Processors
  - CSP focused on 28 & 20nm CMOS

2.5D Side by Side Stacking on Interposer
  - Supporting development for ASIC, FPGA, GPU and CPU
  - Large body package focused & large silicon interposer focused (retical size)

• **MEOL (back side wafer process)**
  - Wafer finish process flow being used almost exclusively; both organic & inorganic
  - Supporting both 200mm & 300mm wafer sizes
  - Providing wafer front side bump services
  - Ability to handle varying TSV wafer quality & ability to thin to 50μm
### 3D/2.5D Drivers & Benefits

<table>
<thead>
<tr>
<th>Memory Bus Speed</th>
<th>Lower Power</th>
<th>Fab Yield Improve</th>
<th>Cost</th>
<th>Time to Market</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide Parallel Busses</td>
<td>Wide Parallel Busses</td>
<td>Departition Fewer SoC Layers</td>
<td></td>
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<td>Wide Parallel Busses</td>
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<td>Departition Fewer SoC Layers</td>
<td>System Level Cost Reduction</td>
<td>✓</td>
</tr>
<tr>
<td>Gate to Gate Routing</td>
<td>Deconstruct into Smaller Die</td>
<td>Improve Fab Yield = Cost Redx</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Si Interp + Logic + Logic</td>
<td>Si Interp + Serdes + Logic</td>
<td>Deparition (e-DRAM)</td>
<td>System Level Cost Reduction</td>
<td>✓</td>
</tr>
</tbody>
</table>

- Focus process node development on specific application functionalities
- Improves performance, power, and area of each application functionality
3D/2.5D Challenges for Future Production

- **2.5D Sector Interest Growing Fast**
  - Many assembly challenges; very large thin die; primarily multiple die
  - Supply chain severely constrained today for interposers
  - A constrained interposer supply chain will negatively impact product proliferation

- **3D Sector Very Price Sensitive**
  - Improved performance is certain; however, at what cost?
  - Assembly and test yields improving rapidly; need more data on device time based performance to ensure reliability
  - MEOL portion of pricing needs to improve; skewing package pricing in this product sector
Thank You!
How to enable building the 3D ecosystem

Toru Ogawa
TSMC
2.5D/3D Application Trend

- Lower power
- Small form factor
- Very short interconnection length
- Low-power/Wide I/O memory
- The virtual SoC

Mobile (Homogeneous)

New appli. by “More than Moore”. (Heterogeneous)

- High speed for real-time processing
- Huge-scale wide I/O memory
- Almost same performance as SoC

Time line

GPU/Network (Heterogeneous)

FPGA (Homogeneous)
CoWoS (Chip on Wafer on Substrate) Infrastructure

Application
- Networking
- PC and Game
- Mobile

Design Ecosystem
- EDA - Implementation, DFT, Verification, Analysis
- Design Service
- IP - DRAM Model, Controller, PHY, Repair
- Standards – JEDEC (DRAM), IEEE (Test), Si2 (DB exchange format)

Memory
- High Bandwidth DRAM
- Wide IO DRAM

Manufacturing Infrastructure
- Substrate
- Assembly
- Final Test
Challenges Ahead

- Process technology
  - Already done

- Silicon interposer warpage control
  - Thermal/Mechanical modeling for impact analysis

- Design tool readiness
  - To be done

- Testability at supply chain hand-off point
  - Establish clear owner ship

- Low-power wide IO memory for 3D stack
  - Needs to lead by end-customer, as electronic industry
Memory Scaling and Integration with Logic for System Optimization

Fumiyasu Hirose
Vice President, Technology Executive
Cadence Design Systems, Japan
Short, medium and long term path to 3D-IC
EDA work starts at least 3-4 years earlier

Si Partitioning with TSV Interposer

- Market: FPGA
- Xilinx in 2010
- 2011-2012
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- MARKET: Server & Computing
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- **High performance computing**
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  - ~ 2015
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Standards & Ecosystem & Cost

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Cadence proven 3D-IC solution
~8 test chips and 1 production chip since 2007

Custom, Digital & Package need to understand 3D constructs
Modeling and database infrastructure to support TSVs, Micro bumps, backside metals
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Seamless Digital, Custom and Package co-design
Cadence is leader in custom with Virtuoso
Cadence has SiP solution spanning digital, custom and package for last 6 years
Cadence is leader in Mixed signal solution using OpenAccess
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Ecosystem partnership and Real Experiences/proofpoints
Cadence has been working with ecosystem partners since 2007 on 3DIC
8 testchips completed and 1 production chip done spanning industry short term, Medium term and long term
Several projects ongoing
Cadence 3D-IC solution is built with partnerships

3D-IC Ecosystem and Collaborations

EDA and IP

SoC Vendor

Memory Vendor

Interposer, Packages

3D-IC Ecosystem

IDM and Foundry

Mfg. & Test Equipment

OSAT

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Designers: Analysis Driven Design & Stacking Methodology
Cadence 3D-IC solution is built with partnerships: 3D-IC Ecosystem and Collaborations

3D-IC Ecosystem:
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Designers: Analysis Driven Design & Stacking Methodology

System House: Multi-Die Integrated Package Prototyping
Cadence 3D-IC solution is built with partnerships through a 3D-IC Ecosystem and Collaborations.

- **SoC Vendor**
- **Memory Vendor**
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**Designers:** Analysis Driven Design & Stacking Methodology

**System House:** Multi-Die Integrated Package Prototyping

**Foundry/IDMs/OSAT/Interposer/Package:** Rules, Stacking Layers & Modeling
Cadence 3D-IC solution is built with partnerships:

3D-IC Ecosystem and Collaborations

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- Memory Vendor
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Designers: Analysis Driven Design & Stacking Methodology

System House: Multi-Die Integrated Package Prototyping

Foundry/IDMs/OSAT/Interposer/Package: Rules, Stacking Layers & Modeling

Everyone:
Cost models, DFM/Yield/Reliability And Redundancy
Dr. Subramanian (Subu) Iyer

IBM Fellow, Microelectronic Division
IBM Systems & Technology Group
Enabling the 3D ecosystem

3D Integration is

But

3D Integration is more than Technology, Design & Test

Supply Chain Management will be the toughest nut to crack!!

GSA- Sematech Conference Panel (Iyer)
Ceramic and Organic interposers

How did we do this?

- Multi-Layer Ceramic technology introduced in the early 1970’s
  - Acceptable electrical properties
  - Excellent CTE match to silicon
  - Robust platform for thermal solutions
  - Cost effective for high end solutions

- Today Organic laminates being used across the full customer base from low-end applications through high-end Servers
  - Cost effective for low end solutions
  - Superior electrical characteristics (shorter vertical dimensions, Cu conductivity, lower k, tighter C4 pitch...)
  - CTE mismatch to silicon is high
3D Design Methodology: New Considerations

- **Planning/High Level Design Phases**
  - Additional architectural and physical planning needed for shared stack resources during HLD of individual layers

**Design Development Phase**
- Partitioning of shared stack resources to allow individual layers to proceed independently
- Additional constraints/contracts and crosschecks to ensure design closure at both the stack level and system level

**Chip-Release Phase**
- Planning of release data or abstracts for checks
- Closure on stack level verification (e.g. functionality, timing, thermal) against other layers or stack contracts

J. E. Barth – 3DIC Design  Feb 2011
Memory Scaling and Integration with Logic for System Optimization

Tim Whitfield
Director of Engineering
Hsinchu Design Centre, ARM
The IP Provider’s Role

- Design enablement
  - IP provision, reference designs and standards
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- Technology leadership
  - R&D crystal ball, exploiting the technology
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- Eco-system coalescence
  - Building the relationships: IP, EDA, SiP, foundry
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  - R&D crystal ball, exploiting the technology

- Eco-system coalescence
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- IP sales
  - Logical and physical IP, making it commercially viable
The Challenges

- What hasn’t been said before?!
The Challenges

- What hasn’t been said before?!
  - Supply chain
  - Standards
  - Thermal management
  - Cost
  - Design

- Where are the $$?$$
  - Need a compelling event/reason
  - Technology leadership – intangible and long term
  - IP provision – where is the value?
Panelists: THANK YOU !
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Panelists: **THANK YOU!**
Panelists: THANK YOU!
Panelists: THANK YOU!

Audience: QUESTIONS, PLEASE!