Innovation Exploration in Coming Heterogeneous Integration Era

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CEO, Chairman and Founder, Etron Group
GSA’s Asia-Pacific Council Leader, Board Director and Board Chairman from 2009 to 2011

April 16, 2012
One Afternoon at a Belgium Station
The Experience Economy*

- Experience ≡ Heart Touching
- Heart Touching Drives Service; Service Defines Products

Work is Theater & Every Business a Stage

Microelectronics and Semiconductor Technologies are Cornerstone and Enabler of Heart-Touching Experiences

- World Flat at Fingertips by Mobile Computing
- Sky Soar on Clouds through Communication & Data Center

Heart-Touching Devices

Experience Connected by Internet Networks

Heart-Touching Services

Suppliers of Advanced IC Technologies

Etron 鈺創科技
Design Technology Leader

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Etron, Intel, Qualcomm, Samsung, ST, Toshiba, TSMC

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Key Driving Forces for IC Industry Growth

- ’70s  Technology (Circuits): Pioneer or System House
- ’80s  Manufacturing & Automation: IDM*
- ’90s  VLSI Design: Fabless and Foundry
- ’00s  Diversified Applications: System Chip & Cluster Model

*IDM means Integrated Device Manufacturer
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- ’10s  Life Effectiveness: Ubiquitous Integration of Human-Machine-ICs
- ’20s  Fusion of Heart-Touching System into Life, Body, and Community: Heterogeneous Integrated Design & Architect

*IDM means Integrated Device Manufacturer
Moore’s Law – Homogeneous Integration

- The number of transistors per square-inch doubles each 18 months

Source: Intel

*Gordon Moore: Co-founder of Intel 1965
Heterogeneous Integration* (HI) is Happening

- New System Chip Architecture: mD-IC (multi-Dimensional Die Integration Chip); m= 2, 2.5, 3, 4…

*After Nicky Lu, ISSCC 2004 Plenary Talk
MDSC Analogy

- Metropolitan-like Die-Society Cluster
  - Conceptualized as land development and building construction
    e.g. Taipei World Trade Center versus one-story range at Texas

Like single die

Taipei World Trade Center
System Chip Needs Bare-Die Memories

After T.H. Tong (ASE Corp.) 2004
3D Integration Technologies

After John Lau, IEEE-ECTC PDC, 2009
3D Integration

3D Si Integration

No sight in Volume Production in the next 10 years

The right way to go and compete with Moore’s law. The industry should strike to make this happened! Thin Wafers

W2W (SiO₂-SiO₂) bonding

3D IC Integration

Memory-chips Stacking

Cost issues and Competing technology

8@50μm thick 2Gb Chips (16Gb)

Active Interposers (Wide I/O DRAM, Wide I/O Memory)

Need Ecosystem, EDA, and Business models. 3D Wide I/Os

Passive Interposers (2.5D & 3D)

Will be used the most in the next 10 years

2.5D IC Integration with Passive Interposer

Micro Bump

TSV/RDL/IPD Passive Interposer

3D IC Integration with Passive Interposer

TSV/RDL/IPD Passive Interposer

After John Lau, Plenary keynote at 2011 IWLPC
Potential Applications of 3D IC Integration

Memory-Chip Stacking
- DRAM or NAND Flash stacking with TSVs on organic substrate
- Over molding the DRAMs or NAND Flash

Wide I/O Memory
- Wide bandwidth/low power memory on CPU/Logic with TSVs
- Logic on Logic with TSVs
- Underfill is needed between active chips

Wide I/O DRAM
- DRAM stacking with TSVs on Logic with TSVs
- Over molding the DRAMs

Wide I/O Interface
- Moore’s law chips on a passive interposer with TSVs
- Underfill is needed between chips and the interposer

Underfill is needed between the active/passive TSV interposer and the organic substrate

After John Lau, Plenary keynote at 2011 IWLPC
Intel’s TSV (Through Silicon Via) in 3D Interconnects

A four stack wire-bonded die package

Advantages:
- Smaller form-factor
- Low power
- Wider bandwidth
- Better performance

After John Lau, Reliability of 3D IC Interconnects, 2011
New Measurements in mD-IC Era

■ Moore’s Law
  - More transistors in a 2D die area
  - Monolithic Integration (MI) by using planar technologies in a single die
  - 2X in 12 to 24 months
  - 45-year progress will continue for another 2 decades

  (G. Moore, Electronics 1965 & ISSCC 2003 Plenary Talk)

■ 3D IC - Lu’s Metrics
  - More functions per unit volume in a smaller footprint
  - Heterogeneous Integration (HI) by using multi-dimensional stacked-die technologies
  - Multiple-X every year?*
  - Emerging as Application-driven, started in the 21st century and continuing

*Nicky Lu, ISSCC 2004 Plenary Talk

*Ho-Ming Tang (ASE) and Nicky Lu observed a linear increase in the number of devices divided by the cube root of total package dimensions on an exponential axis vs. time.

(Nicky Lu, ISSCC 2004 Plenary Talk)
Growth Barriers for the IC Industry - Return on Investment Issues

- Can a $300B Industry Sustain Building Future $10B Angstrom Fabs?
  - Annual announced Capex has exceeded $45B in 2011
  - How much is the Industry's profit required to cover continuous Capex investments?
  - It’s hard for most Fabless to share the risk that Foundries have committed to take

- How Many Times Can a Company Afford Each >$100M Design Failure?
  - A few bugs can scrap a design investment
  - A few field-application or reliability failures can cause >2X penalties
  - Unexpected customer changes can force design termination

- More Product Introductions have Suffered and Fallen off Cliffs
  - Clones, copycats, overcompetition, last-minute changes in customers/suppliers...
  - Speculative patent litigation without solid grounds hurts productivity
  - Products do not have high value nor stay long enough to achieve returns
Do ICs Need a Renaissance?

Where is the new da Vinci?

- A painter, sculptor, musician, scientist, mathematician, anatomist, geologist, writer, cartographer, botanist, engineer, inventor, but
- The Broadest and Deepest Architect and Designer!
New Technology Frontier: DNA Synthesis

- Moving From Cutting-and-Pasting DNA to Programming DNA
- Carlson’s Curve Shows Exponential Growth that Exceeds Moore’s Law
- Analogous to Computer Science and Electrical Engineering, Humans are Breaking New Ground in Programming DNA

Source: The Economist, 2006
Living Electronics are Possible: Biological Memory and Counters in Living Cells

- Single Invertase Memory Module Encodes Memory in DNA Orientation

- Single Invertase Memory Modules Enable Counter Circuits in Living Cells

After Professor Timothy Lu, MIT (Source: Science 2009)
Define mD-ICs Based on Vector Description III

For Example,

\[ mD = 8D = Y3 + Y6 + Y7 + Y8 \]

- **Vector Axis Contents**
  - Axis Y0: Transistor, diode, etc.
  - Axis Y1: IC die in silicon, GaAs, InP, etc.
  - Axis Y2: Silicon Carriers, Active/Passive Interposer, etc.
  - Axis Y3: A die-tower (Multiple Dies Stacked Vertically)
  - Axis Y4: Multiple die-towers (Laterally Positioned)
  - Axis Y5: Embedded active/passive in multi-layers substrates, superlattice, etc.
  - Axis Y6: Optical/magnetic component
  - Axis Y7: Bio sensor, life device, and electronics, etc.
  - Axis Y8: Energy storage device, battery, etc.
  - ...Axis Y100 ~ Axis Y

Substrates

- LED
- Optical function
- Solar cell/Battery function
- Bio function
A Low-cost High-power 3D LED and IC Integration SiP with TSV Interposer with Embedded Fluidic Channels

3D MEMS and IC Integration on PCB/Tape

MEMS Substrate with TSV
Cavity Package Cap
Sealing Ring
MEMS Device
Ordinary Solder Bumps
Tiny Solder Bumps
Through Silicon Via (TSV)
ASIC Chip

MEMS/ASIC Module Attached on the Substrate of a Package which is Assembled on PCB

or

MEMS/ASIC Module Flip-Chip Attached on PCB

Solder Balls
Underfill may be needed between the ASIC and substrate

New Paradigm for the Integrated Design Industry

- From Manufacturer to Designer to Heart-Touching Architect
- Today, IC Industry < Silicon Industry, but Tomorrow, Integrated Design & Architect (IDA) Industry Based on IC Industry > Silicon Industry
Industry Business Structures are Varied in the Experience Economy (I)

**Vertical Integration**
- IDM (Integrated Device Manufacturer)
  - Application & Subsystem Design
  - Chip Design
  - Wafer Fab
  - Packaging & Testing

**Horizontal Segmentation**
- Fabless & Foundry
  - Application & Subsystem Design
  - Chip Design
  - Design Foundry
  - Wafer Foundry
  - Packaging & Testing
  - IP/EDA

**Notes:**
- CVVI?!
Industry Business Structures are Varied in the Experience Economy (II)

- Clustered Virtual Vertical Integration (CVVI)
  - Co-Development by Companies
  - Integrated Knowledge Domains
  - Profit and Loss Sharing
  - Heart-Touching Experiences

- Versus Vertical & Horizontal Integration

After Nicky Lu, ISSCC 2004 Plenary Talk
New Business Mindset in the Experience Economy

Leadership (Top-Down)
Support Organizations & Infrastructures:
Process & object-oriented
New Business Mindset in the Experience Economy

Heart Touching (Bottom-Up)
Experience Delivery
Channel: Human-oriented

Leadership (Top-Down)
Support Organizations & Infrastructures:
Process & object-oriented
New Business Mindset in the Experience Economy

Life-Worth Experiences: Joy, Wealth, Love, Peace

Resource Flow: Synchronized to Support

Heart Touching (Bottom-Up)
Experience Delivery
Channel: Human-oriented

Leadership (Top-Down)
Support Organizations & Infrastructures:
Process & object-oriented

Value Flow: Prosper and Touch Hearts

“For where your treasure is, there will your heart be also.”
- Mathew 6:21
Etron Product Synergy is Aligned with Experience-Driven Mindsets

Buffer Memory (Brain)  3D WebCam (Eye)
USB3.0Host (Nerve)  USB3.0 Flash (Thumb)

Buffer DRAM & KGDM: Storing Experiences

Webcam Controllers: Capturing Experiences

Memory  Logic

USB3.0 & High Speed Serial Links: Connecting Experiences
USB3.0 Flash Drive Controller: Touching Experiences

Like!
Etron is Very Open to Collaboration via Either Vertical Integration or Horizontal Engagement

- In the Coming Heterogeneous Integration Era, Etron Welcomes Collaboration with Companies under the CVVI Model
Through Semiconductor

We Connect People to

Touch the Dream

www.etron.com