



WORLD

ISO/TS 16949 CERTIFICATION BY SEMICONDUCTOR COMPANIES

SEVEN GROWTH OPPORTUNITIES FOR THE CHIP INDUSTRY DURING THE MARKET UPTURN

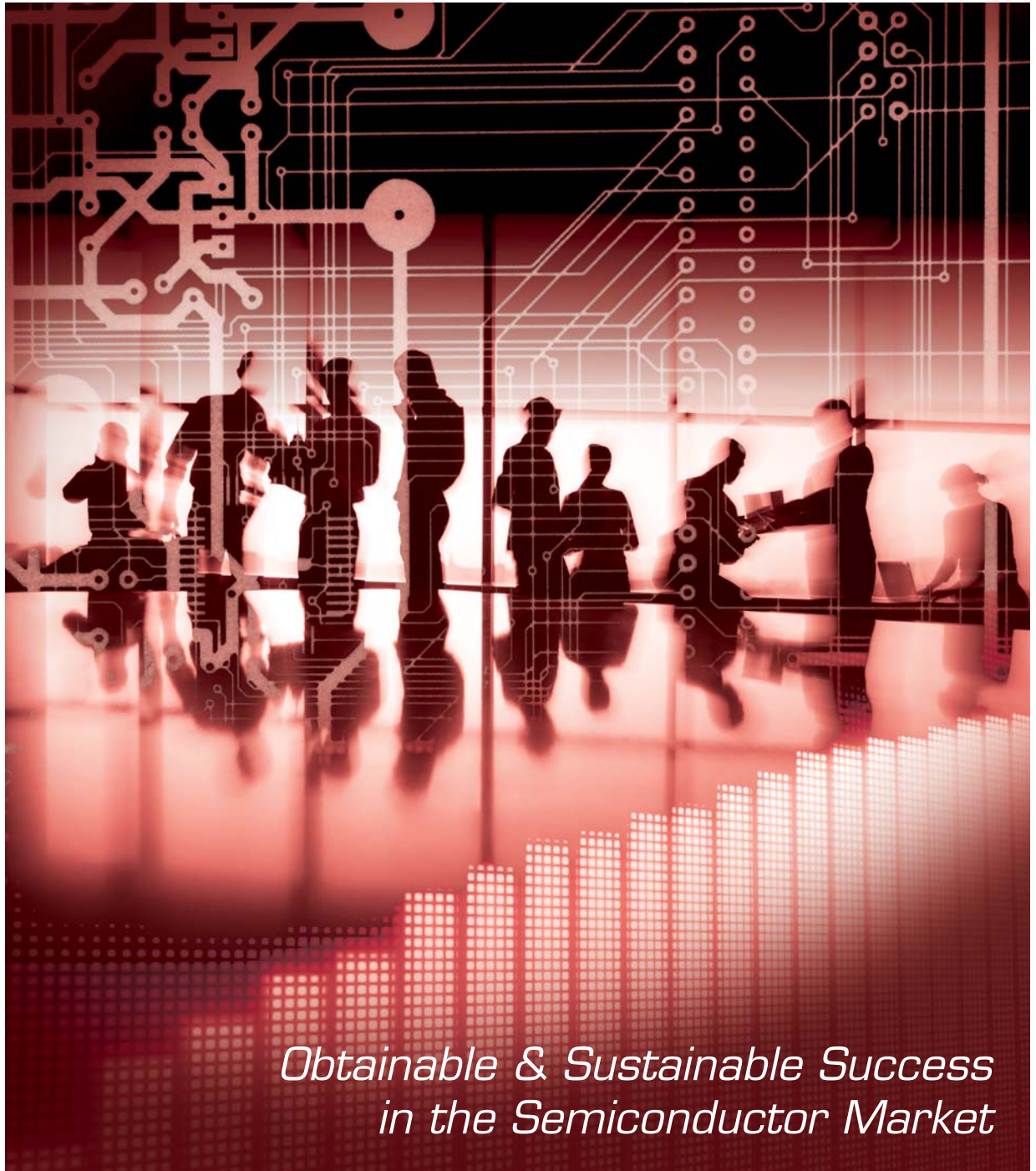
SERIAL COMMUNICATIONS IN SOC DESIGN: HOW TO SUCCESSFULLY INTEGRATE SERDES IP

MAXIMS: DATA, DECISIONS, REACTION RATES — HOW EACH DEFINES MARKET SHARE GAINS

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A TIERED MANUFACTURING STRATEGY: THE NATURAL SOLUTION FOR A HIGH-PERFORMANCE

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MISSION AND VISION STATEMENT

ISO/TS 16949 CERTIFICATION BY SEMICONDUCTOR COMPANIES

DOUG SCOTT, DIRECTOR, QUALITY AND PRODUCT ENGINEERING, FLIPCHIP INTERNATIONAL
JOHN BOSI, QUALITY MANAGER, FLIPCHIP INTERNATIONAL

A relatively recent catch phrase in the semiconductor industry regarding quality management system (QMS) certification is “TS certification.” TS is short hand for a comprehensive QMS standard called ISO/TS 16949. The goal of ISO/TS 16949 is to develop a “best-in-class” process-based QMS that provides for continual improvement, emphasizing defect prevention and the reduction of variation and waste in the supply chain. This QMS platform was originally developed and agreed upon by major automotive manufacturers in the United States and Europe to provide a common approach to quality system management. With the rapid integration of semiconductor devices into all aspects of automotive manufacturing, ISO/TS 16949 is gaining traction throughout the entire supply chain.

ISO/TS 16949 is based on all the currently mandated and industry-standard ISO 9001:2008 specifications with the addition of automotive industry-specific requirements. ISO/TS 16949 is more stringent in every aspect than any other QMS currently available. To meet these TS requirements, there is a need for increased management interaction, customer focus, employee competence, resource management, continual improvement and review of key performance indicators (KPIs). However, with top management’s commitment to quality, strategic planning and a process-based approach, ISO/TS 16949 certification is not out of reach by semiconductor companies committed to improving their current QMS and expanding their market base.

So how does a semiconductor company successfully pass the third-party audit process and become ISO/TS 16949 certified on the first attempt? From experience, seven key areas have been identified. If these areas are addressed properly in advance of the certification audit(s), the likelihood of obtaining ISO/TS 16949 certification is well within reach.

- Define a Clear Company “Quality Policy” – The force that dictates a unified quality focus throughout the QMS is a company’s quality policy. This quality policy should clearly address the goal to achieve customer satisfaction by exceeding requirements and expectations through continual improvement. Continual improvement, in particular, is a recurring theme of the ISO/TS 16949 standard. All employees should have a

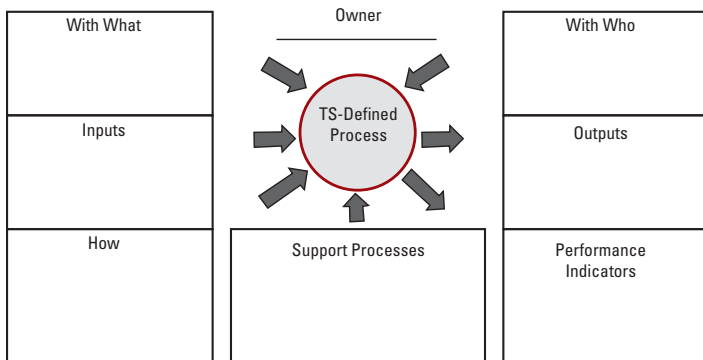
thorough understanding of the company’s quality policy. This policy shall be regularly reviewed. In addition, each employee should be empowered within this policy’s umbrella to identify and gate maverick material from reaching the supply chain. It is critically important that everyone, not only the quality department, take ownership of “quality” within an organization.

- Attain Full Management Buy-in and Support – ISO/TS 16949 certification cannot happen overnight, nor can the preparation for the certification audit. There is a significant amount of preparation activity that needs to take place within all departments of a company. These departments need to take individual responsibility to ensure that their areas are ISO/TS 16949-compliant. For this to happen, top management needs to completely embrace the TS certification process and direct the entire organizational structure to ensure full support of the QMS upgrade. Organization support includes being receptive to work with internal auditors and willing to address internal audit findings with permanent, corrective actions. While insight gained from external auditors is always helpful, the internal organization is in an excellent position to identify its key strengths and opportunities for improvement. Top management will also need to be involved in QMS reviews throughout the year. This review shall include documented meeting minutes identifying support for company-wide continuous improvement activities and objectives.
- Identify a QMS Representative to Lead the Preparation Process – With top management’s commitment in place, a management-level QMS representative will need to be identified with the responsibility and authority to manage the entire TS preparation and audit process. The third-party TS certification auditors will dig into every area of the company’s QMS, and having a confident, knowledgeable QMS representative overseeing these activities is paramount. This QMS representative shall manage implementation steps and timelines, ensure top management involvement and support, and set in motion the entire organization’s embracement of ISO/TS 16949 requirements through education and training. Additionally, this QMS representative should have a clear understanding of all ISO/

TS 16949 requirements and be able to focus extra preparation activities to areas that need more assistance. A well-organized approach is absolutely essential. Expect approximately six to nine months of necessary preparation time prior to the third-party certification audit.

- Achieve a Clear Understanding of a “Process-Based Approach” – The idea of a process-based approach is the heart of the ISO/TS 16949 standard. A process-based approach governs the mindset and actions in an organization and is oriented towards achieving a vision rather than targeting specific individual tasks. This kind of process-based approach differentiates ISO/TS 16949 from typical element-based QMS approaches. For example, under an element-based approach, performance indices such as tool up-time and on-time preventative maintenance (PM) performance would be individual items or elements of concern for the equipment engineering department. Under a process-based approach, the equipment engineering department under the vision of the company’s QMS would have responsibility for all equipment activities that would affect company-wide on-time delivery goals. Tool up-time and on-time PM performance would therefore be only two performance indicators within a larger scope of their QMS responsibilities. Each area of a company that has inputs, outputs and performance indicators are considered an individual process in a process-based approach system. Identified processes within the QMS could be sales, logistics, research and development, finance, purchasing, process engineering and management responsibility (depending on applicability).
- Create Turtle Diagrams – Turtle diagrams are an excellent way to detail all items that relate to processes within the QMS. All processes should have identified supporting processes, inputs, outputs and performance indicators in addition to required specifications (how), systems (with what) and persons involved (with who). A turtle diagram will present all of these items in a simple and organized way. Completed turtle diagrams will show third-party auditors that the company has a clear understanding of the TS-mandated process-based approach. These diagrams also make the audit process easier and as a result help the TS auditor(s) consider all aspects of the organization’s business process when determining conformance levels.

Figure 1. Turtle Diagram Example



- Ensure the Integrity of Defined Systems – With all of the above listed planning in place, any lack of identified and documented QMSs will lead to major non-conformances during the ISO/TS 16949 audit. The following systems should be in place with fully documented specifications, gate reviews, internal audit trails and all required output performance indicators: advanced product quality planning (APQP), process failure mode and effects analysis (PFMEA), measurement system analysis (MSA), production part approval process (PPAP) and statistical process control (SPC). The ISO/TS 16949 auditors will spend a significant amount of time ensuring these systems are instituted as they are explicitly required by the TS standard.
- Encourage Complete Employee Support and Involvement – The last, but equally important, key step to obtaining ISO/TS 16949 certification is full employee support and involvement during the preparation process. To aid in the visibility of TS, it is important to have activities identified that are not only beneficial to the QMS, but also remind employees of ISO/TS 16949 on a daily basis. An activity that falls into this category is having a 5S initiative. 5S is a workplace organization methodology in which the five S’s stand for sorting, setting, shining, standardizing and sustaining. Having such an initiative in place addresses two needs. First, 5S helps to meet the TS requirement for cleanliness of premises, and second, it empowers employees to take ownership of their particular area in respect to workplace organization. This employee ownership, in turn, permeates into all aspects of the ISO/TS 16949-defined QMS. Ultimately, the decision to become ISO/TS 16949 certified is not a simple one. In addition to ensuring all ISO/TS 16949 requirements are addressed during the preparation, there needs to be significant top management support, planning, QMS management and complete company-wide involvement. However, the benefits far outweigh the investment required to obtain this difficult certification. Companies that have successfully completed the TS certification process agree that their new QMS is more comprehensive and better defined than it was with other QMS certifications. The process of redefining a company’s QMS to meet TS standards leads to increased departmental ownership, product yields, supply chain management control and continual improvement activity. Regardless of a semiconductor company’s supplier tier level to automotive end applications, ISO/TS 16949 certification is absolutely obtainable and worth every effort to achieve this “best-in-class” QMS. ■

About the Authors

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By capitalizing on the hybrid TV market with a new, innovative approach, Fresco Microchip experienced record growth in only a few quarters—an accomplishment that is very difficult for a start-up to attain. In my interview with Lance Greggain, president, chief executive officer and co-founder of Fresco Microchip, we discussed the key enablers of the company's remarkable growth, where the analog-to-digital transition in various regions stands today and how the company confronts this issue, new opportunities and much more.

— Jodi Shelton, President, GSA



LANCE GREGGAIN

President, CEO and Co-founder, Fresco Microchip

Q: By targeting the hybrid TV market, Fresco Microchip transformed itself into one of the fastest growing fables companies of 2010. How does Fresco plan to continue this momentum? While there are few companies serving this market, how does Fresco ensure that it remains innovative and competitive?

A: One of the first strategic decisions Fresco Microchip made was to serve an existing market (which for us was hybrid TV), thereby reducing market risk. This has greatly contributed to our growth. The company's unwavering dedication to delivering value through innovation and providing performance improvements that reduce system costs will sustain our incredible growth. We have a multi-generation plan geared towards providing this value to the TV tuner industry and other consumer electronic (CE) companies.

To remain competitive, we structure the company around innovation. We have a fundamental understanding of system requirements and a continued objective of trying to improve the value proposition that we present with every product generation. In the past, I have witnessed start-ups developing innovative technology, riding that innovation without improving upon it, and as a result, competitors taking away their market share. A company must always innovate, be aware of their value proposition and continually update their proposition or else it will be taken from them.

Q: Can you give us an example of how Fresco Microchip has helped to drive technology? As a GSA member for over four years, how has the Alliance helped Fresco in this endeavor?

A: It was only two years ago that

analog demodulator chips with external SAW filters saturated the TV market. However, today, these chips are essentially disappearing within this market with the introduction of the hybrid model. As previously mentioned, Fresco has always had a thorough understanding of system requirements and how combining analog and digital signal processing (DSP) technology could create a paradigm shift in the market. Fresco has established a new benchmark for picture quality at the lowest system cost.

GSA is an invaluable source of industry information and networking. They say no man is an island, and no start-up is an island either. Without this industry support, I believe it is very tough, particularly when you are not in Silicon Valley, to be a successful start-up.

Q: As a small company, Fresco Microchip displayed remarkable performance in meeting the demand of original equipment manufacturers (OEMs) for hybrid TV receiver chips in a timely manner. What company strengths enabled Fresco Microchip to swiftly take the necessary actions (e.g., secure foundries, double work staff) to successfully deal with this urgency?

A: Fresco's strengths lie in our competent employees and the strong partnerships we have formed with suppliers. All Fresco's founders had previous experience with start-ups, so we knew the difficulty and complexity of serving the hybrid TV market in a start-up environment. As a small company, to execute our value proposition and provide the complete system solution to customers—chips, software and design support—our employees have had to wear multiple

hats and rotate responsibilities. Our solid design-for-test (DFT) and design-for-manufacturability (DFM) methodologies come from years of slugging it out and providing products to a very demanding customer base.

In addition, we have really good partners. We have had the support of Taiwan Semiconductor Manufacturing Company (TSMC) and our assembly and test provider Unisem. Unisem ramped flawlessly and executed very well on the operations side. In fact, Fresco shipped over 10 million parts before we had a single test escape return.

Q: Though digital broadcast is certainly taking off, each of the major regional markets is in a different phase of the analog-to-digital transition, creating difficulties for TV manufacturers that must meet the different regional specifications. How do Fresco Microchip's solutions allow its customers to support multiple regions?

A: Most analysts predict the analog to digital transition to take 5–10 years, which is a lot longer than expected. The transition is underway in North America, but over 300 million TVs are still connected to an analog cable plant. Nobody ships a TV to North America without an analog tuner and demodulator. Canada is likely to begin the transition sometime next year. However, a vast majority of Canadians own analog transmitters so it will be a tough switch. In the EU, it is still somewhat fractured. France is in the beginning stage, while Eastern Europe has not started at all. The transition in China is moving more slowly than anticipated, and Mexico has no set timetable.

The fundamental design of



Jasper Design Automation's formal verification solutions are proof that innovation in EDA is alive and well. In my interview with Kathryn Kranen, president and chief executive officer of Jasper Design Automation, we discussed the benefits of the company's verification solutions, how the acquisition of EDA start-ups can stunt innovation, issues the EDA sector is addressing through collaboration and much more.

— Jodi Shelton, President, GSA

KATHRYN KRANEN

President and CEO, Jasper Design Automation

Q: *As the complexity of today's electronic devices increases, chip design verification becomes more of a challenge. Please explain how Jasper Design Automation's formal verification solutions reduce risk and accelerate time-to-market for chip companies.*

A: The Jasper difference is in the way we apply and deploy advanced formal verification solutions to meet the particular needs of our customers. Our solutions address a spectrum of design-critical verification challenges such as getting the architecture unambiguously right, enhancing design reuse, verification including low-power optimization, protocol certification and post-silicon validation. Deploying formal technology, from design inception through intellectual property (IP) exploration and even post-silicon, can greatly accelerate time-to-market and deliver a high return on investment (ROI). We often hear from new customers that formal verification can quickly root out bugs in designs that had previously been in verification for months.

Q: *The verification obstacles encountered by system designers and chip designers are becoming increasingly similar, leading some to believe that the two groups will eventually merge. How does the use of formal verification benefit system designs?*

A: The early use of formal verification for model system architectures before register transfer level (RTL) can provide benefits through the entire development cycle, spanning both hardware and embedded software. Formalizing an executable spec accelerates the design and verification of a chip and individual design components. High-capacity formal

verification is also key for verifying hardware interaction with software, including the operation of software-configurable registers, register assignments, and other software-programmable hardware functions such as power control. Looking at the need for hardware/software co-design, and the marriage of hardware and software verification for systems, formal verification technology is critical. Formal verification, by its mathematical nature, is independent of complexity in a way simulation can never approach, and can verify complex interactions rapidly and comprehensively for hardware, software and systems.

Q: *In a market where EDA start-ups and venture capital are scarce, Jasper Design Automation has launched reputable products as well as gained recognition for its innovative efforts. Amid a tough environment, what are the keys to success that has allowed a small company such as Jasper Design Automation to prosper?*

A: Jasper thrives because we completely focus on delivering a flexible, broadly deployable solution, including support, which solves top customer problems directly. Jasper's architecture investment supremely lends itself to rapid innovations that we often develop in partnership with our customers. This is diametrically opposed to delivering a software package that ends up sitting on a shelf unused. Jasper also created a scalable business model to reflect its broad and demonstrable value. Thankfully, raising capital has never been a problem for Jasper due to the viability of our business model, our impressive customer traction, and making strategies and execution metrics transparent to our very

sophisticated investors and board.

Q: *As the current vice president of the Electronic Design Automation Consortium (EDAC), you have promoted the achievements of private EDA companies and showcased the significant return on investment (ROI) the EDA segment delivers to the semiconductor industry. Please describe EDAC's impact on the industry.*

A: EDAC focuses on issues that individual EDA suppliers cannot address themselves. We have government lobbyists to ensure encryption, and export control regulations don't place onerous restrictions on our member companies and customers. We have also developed an anti-piracy initiative to protect the interests of EDA customers and suppliers. The real victims of software piracy are the paying EDA customers who find themselves at a distinct disadvantage when they are selling against competitors who can produce parts more cheaply by using stolen software. As well, EDAC financially and strategically supports the annual Design Automation Conference (DAC), providing a high-quality global technical conference where the EDA community can share ideas, meet with customers and display the latest innovations in our field.

Q: *The EDA space saw quite a bit of M&A activity in 2010, with the larger companies acquiring the smaller players inside and outside the sector. Do you believe this is the best course of action (i.e., acquiring smaller players), or do you believe they should be partnering with other EDA companies or consolidating with other large players?*

A: Consolidation is a fact of life in

SEVEN GROWTH OPPORTUNITIES FOR THE CHIP INDUSTRY DURING THE MARKET UPTURN

SCOTT GRANT, MANAGING DIRECTOR, SEMICONDUCTOR BUSINESS, ACCENTURE

The semiconductor industry survived the recent rough recession. In fact, the industry finally learned from past mistakes by turning off the supply spigot faster and more aggressively than in previous downturns as demand plummeted. This is the good news. The bad news is that many companies in the industry continue to struggle with a wide range of issues, including an excessively narrow focus on engineering chips rather than deeply understanding end markets now and going forward, inefficient global operations and insufficient innovation.

To overcome these hurdles, capitalize on the market upturn and build momentum and growth, what should industry leaders do now? This article tackles this question head on. Drawing upon several industry research initiatives, associated analysis and insights, as well as deep industry experience meeting with executives throughout the industry constantly, this report recommends seven growth opportunities that will help semiconductor companies accelerate towards high performance.

Seven Growth Opportunities

One: Focus on End Markets

In traditional semiconductor end markets, growth depends on winning the “fight for sockets” and gaining a greater share of the silicon in specific end-market devices. Critical to winning this battle is having a much stronger understanding of customers’ reference designs including innovation channels, consumer behavior, and usability and form factor revolutionary modifications for future products. Chip firms need to use this understanding to provide chips that meet future needs. This, in turn, depends on having effective relationships with direct customers and distributors to gain better customer intelligence and a rich understanding of where innovation is headed in a three-to-five-year time frame.

In this pursuit, chip firms need to gather insights into the end market to understand the specific economics, the cyclical nature of demand and the unique nuances of the market. Two areas are critical. First is understanding end-market usage models via data analytics. This means grasping how the usage and movement of

technology, such as smartphones and e-tablets as a convergence of key forms and functions, is progressing within a specific market. Second is comprehending end-market value chains (i.e., what additional insights and expertise are required to succeed in developed and emerging end markets that result in added value to direct and indirect customers). The goal is for chip firms to become value-add design partners versus volume component chip manufacturers.

Two: Focus on Profitable Sales and Operational Planning

Sales and operations planning processes have historically focused on aligning supply and demand from only a unit and volume perspective. Thus, they have been narrower in scope and more conservative in their aims. Under this model, chip companies have typically considered capacity and inventory constraints along with price elasticity to determine optimal price points. Going forward, they need to focus on achieving profitable sales and operational planning. To do this, they need to balance their financial performance with their demand, supply and market realities.

Profitable sales and operations planning deliver probabilistic scenario modeling in profitability, pricing, product/channel mix and capacity allocation. The way to achieve this is by performing responsive supply analytics to improve visibility in forecasting by geography, market channel cost adjustment and inventory. Transitioning from traditional sales and operational planning to profitable sales and operational planning will allow chip firms to better leverage enhanced resource planning, customer relationship management and product lifecycle management investments with data integration and common planning processes.

Three: Focus on IP Design Chain Management

The chip industry continues to contend with intense pressures on product development costs and demands faster deliveries of such products to market. This situation has heightened the importance of chip intellectual property (IP) and design chain management stemming from the convergence of chip manufacturing and IP within early stages of research and development. To achieve growth during the upturn, chip firms need to drive several initiatives, including

integrating the management of IP and decisions about IP product portfolios. Such integration enables more effective collaborations on customer chip designs, lower chip development costs, faster validation of chip designs, reduced IP loss, increased IP reuse and licensing fees, and improved use of engineering capacity.

Four: Focus on Talent Management

With the market in recovery mode, more career opportunities are materializing for semiconductor professionals in various fields such as chip design, field application and technical sales engineering. Leading and retaining this talent is key for chip firms to seize growth. Many of these engineers have endured considerable hardship and excessive workloads during the recession as staffs have been trimmed. It's of paramount importance that semiconductor companies focus on how to retain knowledge, foster healthy organizations and positive corporate cultures, and care for a group of engineers who feel overworked and are looking for better, less stressful and more stable career opportunities.

To address these challenges, chip companies need to focus on succession planning and job ladder redesign. Firms with formal succession planning equip themselves to better weather market upturns by retaining key resources, especially people. Job ladders, which traditionally have been a system for tracking various leadership levels of the chip industry's organizational hierarchy, should be re-evaluated to provide these people with multiple and widely diverse growth tracks and career paths. Such diverse offerings will result in more competitive firms. Too often, chip companies become so focused on delivering a product to market on time that they don't spend enough time managing their talent effectively by helping their teams stay connected with strategic and personal objectives.

Five: Focus on Global Operations

Given the requirements of adapting to evolving markets, most semiconductor companies don't have the operational capabilities and rigor needed to be successful. Many have begun the process of transforming operations, but find it more challenging than they expected. In many cases, firms are transforming multiple areas of the business, yet the capabilities needed in each area are incomplete. Other companies have basic functions in place in areas such as customer relationship management (CRM), product lifecycle management (PLM), supply chain management (SCM) and enterprise resource planning (ERP). But they fall short in having the cross-functional collaboration, end-to-end visibility and process convergence needed to be truly responsive to end markets.

As serious as these problems are, they don't end there. New Accenture research has found that some key operational problems are global in scale. The research found that widespread deficiencies in talent recruitment and information technology have left the vast majority of electronics and high-tech firms poorly positioned for global expansion. Yet the research also found that virtually all survey respondents said they have sufficient capital to execute their global expansion plans. These shortcomings need to be addressed quickly as the battle for highly skilled talent and innovative IT intensifies worldwide.

These operations are changing fundamentally as the market turnaround continues. The research found that cost cutting is being superseded by the need to understand customers better and work more closely with them. Chip firms need to consider fine-tuning their global operations by reviewing their competitive essence—what makes them distinctive and differentiated. They may then use this

competitive essence as a compass to guide their operational decisions, win the next phase of competition and achieve high performance.

Six: Focus on Innovation

Innovation modeling is vital. This is the convergence of the firm's external consortiums, such as university research organizations, with the firm's internal research and development labs. The ability of chip firms to manage the early concept research phase across partners increases the likelihood that the concept will be converted to a marketable product. Leading chip firms need to effectively tie their points of innovation into key product portfolio decisions.

To ignite this innovation engine further, chip firms should develop clear innovation cycles, reward innovative ideas and acknowledge educated risk taking while investigating beyond the obvious and what has always been done. Traditional industry practices may not be growth drivers anymore. The industry has been stuck in many cases with the inability to see things in a different way, and this needs to change.

Additional research also revealed that approximately 60 percent of respondents said their organization has become more risk averse regarding new ideas. And 73 percent agree that their company tends to pursue product line extensions rather than new, groundbreaking products or services. Furthermore, 53 percent say their companies fail to learn from past mistakes.

A growth opportunity for chip firms is how they handle failure. The research found that the best innovators know how to reward failure as an opportunity for growth. Chip companies also need to improve the quality of ideas by breaking down organizational silos. The research discovered that too many companies are compartmentalized into discrete, insular groups that don't cooperate with each other. Too often, there is little if any cross-pollinating of ideas between different departments. As a result, the company as a whole doesn't benefit from all of the best ideas from all members of the company.

Seven: Focus on Embedded Software

Collaborating with various players in the semiconductor ecosystem is one of most important growth opportunities for this industry. Those include companies that develop software for use in the same devices that house semiconductors such as smartphones, media devices, set-top boxes and gaming consoles. The more chip firms collaborate with developers of embedded software to improve smartphone applications, for example, the more robust the opportunities will be to sell more semiconductor chips now and as the smartphone market continues to evolve. Differentiation in the smartphone market is more important and potentially lucrative in embedded software than chips. Chip companies need to get more knowledgeable of embedded software and more collaborative with embedded software providers. This growth opportunity is potentially huge. ■

About the Author

Mr. Scott Grant is currently a global managing director with Accenture's semiconductor practice and is based in Accenture's Phoenix office. He has supported product development, manufacturing, supply chain and customer service across the electronics and high-tech industry. His operational experience includes product development lifecycle, supply chain operations, product validation/test, supplier performance management, planning and operational excellence. Mr. Grant obtained a Bachelor of Science in business, Master of Science in systems engineering and business science, and a master's in international management. He can be reached at scott.grant@accenture.com.

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Thomas Chen, Steering Committee Chairman, e-Manufacturing & Design Collaboration Symposium

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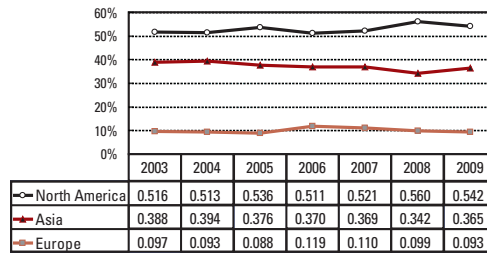
Keung Hui, Program Chair, e-Manufacturing & Design Collaboration and AEC/APC-Asia Joint Symposium

The following article contains highlights from e-Manufacturing & Design Collaboration Symposium 2010—a joint symposium with Advanced Equipment Control (AEC)/Advanced Process Control (APC)-Asia 2010.

For the past two decades, Taiwan has played an important role within the global semiconductor ecosystem. And its role will become even more prominent and crucial as device dimensions continue to shrink and investors take on more risk to manufacture state-of-the-art devices, subsequently necessitating the elevated services of its semiconductor foundries.

With over one-third of semiconductor revenues directly generated by Asian companies (Figure 1) and over 90 percent of fabless revenues indirectly facilitated by Asian foundries (Figure 2), Asia is having a substantial influence on value creation directly (via tangible amounts) and indirectly (via services).

Figure 1. Percentage of Worldwide Semiconductor Revenue by Region



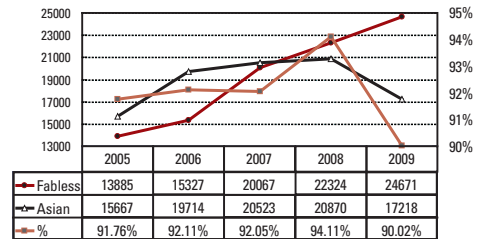
Asia accounts for over one-third of annual semiconductor revenues.

Source: GSA

The macro-economic impact by foundry service providers is best reflected in the increasing revenues reported by the top five fabless companies (Figure 2). Since 2007, these five companies have generated revenues

exceeding the combined revenue of all Asian foundries. In other words, the additional value facilitated by the foundry service far outweighs the cost of the service itself. This trend will be further magnified as the top five fabless companies' revenues continue to increase.

Figure 2. Revenue Generated by Asian Foundries and the Top Five Fabless Companies (Millions of US\$), Asian Foundries' % of Worldwide Foundry Revenues



Source: Wikipedia

The Taiwan Semiconductor Industry Association (TSIA), led by President Dr. T.Y. Wu and actively driven by Thomas Chen, former chairman of TSIA's 300 mm automation working group, launched the e-Manufacturing & Design Collaboration Symposium in 2007 to bring together all practitioners in the semiconductor industry to exchange the latest information about recent advancements, best practices, innovative ideas and exploratory visions. TSIA hopes that by forging a regional platform, every collaborator along the value chain, from design to manufacturing, testing and packaging, can

gather together under the banner of e-manufacturing and address common concerns:

- Supply chain and operational management.
- Logistics and inventory controls.
- Scheduling and production planning.
- Quality assurances through process and equipment controls.
- Design for manufacturability, test and yield.
- Integrated architectures of data exchange, from design files to process measurements and all the way down to the final testing results.

Observing this guiding principle, TSIA diligently collaborates with other institutions such as the Global Semiconductor Alliance (GSA) and Semiconductor Equipment Materials International (SEMI) to organize the e-Manufacturing & Design Collaboration Symposium (Table 1). Dr. Jeremy Wang, GSA's Asia-Pacific executive director and member of the Symposium's steering committee, stated, "GSA appreciates the opportunity to work with TSIA in organizing this annual event and truly hopes to bring more services and create more value for IC designers through such an exercise."

Table 1. e-Manufacturing & Design Collaboration Symposium

Date	Topic	Location
14 June, 2007	Design for Manufacturability	Howard Plaza Hotel, Taipei
27-28 November, 2008	In Conjunction with AEC/APC - Asia	Ambassador Hotel, HsinChu
2 October, 2009	Design Collaboration	International Convention Center, Taipei
3 September, 2010	In Conjunction with AEC/APC - Asia	Royal Hotel, HsinChu

President of SEMI Taiwan and Southeast Asia, and member of the steering committee, Terry Tsao commented, "SEMI has been a long-time partner of TSIA and shall continue to collaborate in endeavors on each and every occasion to bring device manufacturers and equipment suppliers together to create new values and

jointly explore the uncharted frontiers in semiconductor manufacturing."

Directed by the steering committee, the e-Manufacturing & Design Collaboration Symposium's organizing committee strives vehemently to knit together an all encompassing network, threading through various sectors of the semiconductor industry, from IC designers, intellectual property (IP) and electronic design automation (EDA) vendors, device manufacturers, equipment makers, suppliers and solutions providers, research institutions and academic organizations. This initiative is materially reflected in the event program.

For the joint symposium this year, the organizing committee again teamed up with the International SEMATECH Manufacturing Initiative (ISMI) and delivered a program of speakers and topics:

- GlobalFoundries – the future development of advanced process controls (APCs).
- Mentor Graphics – design tool innovations.
- PDF Solutions – advanced node cost reductions, from design through manufacturing.
- Verigy – the supply chain players involved in the final test of semiconductor devices.
- Selete – the consolidation of process and equipment data.

Dr. Brad Van Eck, mastermind and general chair of the past eight AEC/APC Symposiums in Asia and the past 22 AEC/APC Symposiums in the U.S., commented on the joint efforts, "TSIA is doing one superb job, and ISMI truly appreciates the collaboration with TSIA in helping bring the AEC/APC Symposium to Asia."

Although, geographically, Taiwan may be a small island, it considers itself one of the most advanced high-tech industrial bases in the world. Apart from semiconductor manufacturing, the flat panel display (FPD), light-emitting diode (LED) and photovoltaic (PV) cell industries have also grown rapidly in recent years. The geographical constraint has somehow miraculously transformed into a "clustering effect,"

meaning effective reverberating interchanges of capitals, technologies, talents, ideas, knowledge, skilled labor, materials and services in extreme intensities. This peculiar phenomenon is specific to Taiwan, as similar exchanges are diluted over vast geographical regions in other parts of the world. This is possibly one rationale behind the unique global techno-economic success of Taiwan seen over the past three decades.



The organizers of the e-Manufacturing & Design Collaboration Symposium: (left) Thomas Chen, chairman of the steering committee; (middle) Robert Chien, general chair of the Symposium; (right) Dr. Keung Hui, program chair of the joint symposium.

Source: Photograph by Power Chi of GSA

In addition to serving the semiconductor industry, the Symposium's organizing committee also aims to do the following so as to create more value within the supply chain in a cost-effective manner:

- Forge a cross-industry platform where management issues, such as the cascading complexities of supply chains, logistical and inventory difficulties, operational objectives of cost reductions and declining selling prices, IT infrastructures, IP protections and network securities and risk management, can be discussed.
- Integrate practicable solutions for inventory control, production planning and scheduling, quality assurance and yield management at a higher level of sophistication. This serves a higher purpose and transcends all artificial boundaries for the common good of sustainable development.

This year the joint symposium started to see preliminary success with cross-industry presentation of APC applications in the LED industry, where low yield is the paramount hurdle in this embryonic stage to a genuine lighting revolution.

SERIAL COMMUNICATIONS IN SoC DESIGN: HOW TO SUCCESSFULLY INTEGRATE SERDES IP

DAVID DEMARIA, VICE PRESIDENT, BUSINESS OPERATIONS, MoSys INC.

Moore's Law, as applied to computation and network processors, states that speed doubles every two years. However, packaging technology has lagged behind that rate considerably, scaling upward approximately once every eight to 10 years. This differential in growth rates limits the growth of physical connections. Therefore, if system-on-chip (SoC) designers are to achieve major gains in connection bandwidth, the advances must come in the electrical and protocol layers. After assessing the current trends in serial versus parallel interconnection, the design team will likely seek a high-speed serial solution as the only viable choice.

Once they have recognized the advantages of a serial solution, the design team probably will identify a reliable third-party vendor for their serializer/deserializer (SerDes) block of intellectual property (IP). The reason: SerDes IP requires specialized engineering talent and equipment to design and evaluate serial input/output (I/O) functionality. The team then faces two challenges: verifying block functionality and assuring that the block operates correctly when integrated with the rest of the chip's design elements. To assure a successful integration, the IP vendor must also provide post-silicon validation services that characterize the integrated SerDes block's performance.

The Brief Case for Serial: The Parallel Roadblock

Historically, serial communications have progressed from the macro world to the micro level. Most people rely on serial communications in computer networks on a daily basis, namely, the Ethernet protocol. More recent standards such as Peripheral Component Interconnect (PCI) Express, 10 Gigabit Attachment Unit Interface (XAUI), Serial ATA (SATA) and Universal Serial Bus (USB) 3.0 have expanded serial communications to backplanes. The resulting implementations exhibit cost-effective, low pin-count designs.

Further, these designs make no sacrifice in transmission speeds compared to single-ended parallel designs. Current SerDes I/Os exhibit data transmission rates of up to 10 Gbps with roadmaps to higher rates. SerDes IP is already validated in today's field-programmable gate array (FPGA), application-specific IC (ASIC) and network processor unit (NPU) designs. And differential serial designs require much lower power than single-ended parallel interconnects. Stated another way, serial designs transmit much more data for the same amount of power.

When comparing a parallel architecture to the same design in a serial architecture, the observer immediately notes the often dramatic reduction in real estate in the serial solution. Savings result because serial communication increases bandwidth density and reduces the number of interconnects since a serial connection only requires a matched differential pair. Once the design team realizes both the immediate and long-term advantages of shifting to serial I/O, they must then integrate the SerDes IP block into their SoC design.

Defining and Preventing Integration Problems

When chip designers integrate any IP block, regardless of function, they uniformly need to verify two things: that the block functions according to the provider's specifications and, of even more importance, that the block works in their own final design. The IP vendor provides functional evidence of performance specifications by demonstrating that the block works in existing silicon implementations.

Evidence of the block working in the customer's design can only be determined during bring-up and characterization following receipt of engineering samples. However, the IP block vendor facilitates this process by providing the design-for-testability (DFT) production test specification for the SerDes IP block to the design team.

For SerDes blocks, the I/O portion of the IP provides the interface between the chip and the outside world and is therefore mission-critical. Advanced SerDes IP providers take every action possible during the design process to assure successful integration. These steps are typically embodied in an IP integration checklist.

The IP Integration Checklist

A strong SerDes IP vendor provides the chip design team with a detailed checklist that details the technology specifications of the SerDes block. The checklist also includes:

- The targeted foundry's requirements and design file format specifications.
- Area in square millimeters for various lane options and the related power options and specifications.
- Protocol, physical coding sublayer (PCS) and configuration specifications, including reference clock frequency, data

encoding scheme, reference clock jitter and other technical requirements.

- Package and channel mode specification, including package type, interconnect types and number of connectors.
- Deliverables and formats, including documentation, data sheets, performance guides and application notes.

After the IP vendor and the design team have jointly completed the checklist and the customer has integrated the SerDes block into the design, the customer delivers the design files to the foundry for tape-out.

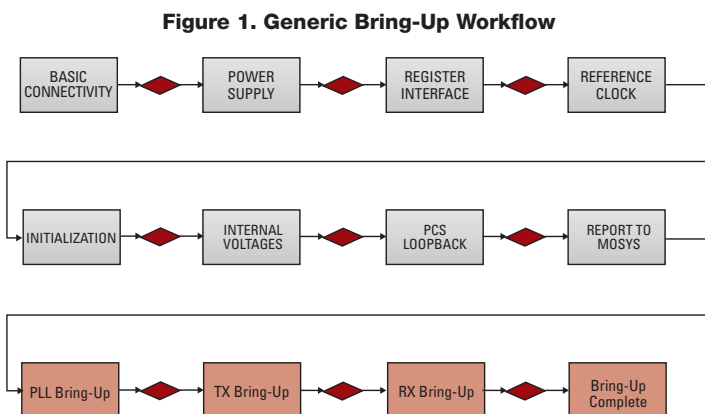
Receipt of Samples: Bring-up and Characterization

Following receipt of samples, the design, now embodied in silicon, must be tested to document the performance of the IP block. Testing verifies that the SerDes block functions with the other design elements. “Bring-up” verifies that the chip functions properly with the other design elements, while “characterization” captures all the necessary technical performance data. The industry usually refers to this process as “bring-up services.”

SerDes devices require specialized engineering talent and equipment to perform bring-up and characterization. Very few companies implementing a new chip design have the technical resources and capabilities to provide in-house bring-up services for SerDes blocks. As a result, the SerDes IP vendor typically provides bring-up services for their customers, including extensive documentation.

During bring-up, the specialized team enables customer sampling through internal loopback at targeted data rates and implements other production tests on the engineering samples. The bring-up plan also tests external loopback at targeted data rates and bit error rate (BER), and conducts a block-by-block functionality check. The team conducts bring-up in pseudo-random binary sequence (PRBS) test mode.

To fulfill complete functional and performance testing, the team characterizes the phase-locked loop (PLL), transmission (Tx) and reception (Rx) performance, power and reset for the SerDes IP block. Tx characterization includes jitter, amplitude, termination and equalization. Rx characterization includes Rx clock path (clock and data recovery (CDR), delay-locked loop (DLL), phase interpolator (PI)), jitter tolerance, equalization, termination and Rx sensitivity. The workflow chart in Figure 1 provides a generic model of the bring-up process.



Summary

Solid planning and preparation significantly improves the likelihood of success for the design team integrating a SerDes IP block. As a first step, the vendor must demonstrate functional evidence verifying that the IP block already functions in silicon. The second is to complete the IP integration checklist. When the design team receives foundry samples, they then verify that the block functions properly and characterize the technical performance data—bring-up services in industry parlance. The final test report delivers the detailed characterization and fully validates that the SerDes block works with the rest of the chip.

Conclusion

As SoC designers recognize the advantages of serial communications over parallel, they achieve increased data throughput without increasing power requirements. Because SerDes IP requires specialized engineering and capabilities, few design teams will have the resources to develop the IP in-house. By selecting a SerDes IP vendor with proven performance and capabilities, the team can expect a smooth integration.

Because SerDes I/O provides the interface between the chip and the outside world, validation of the IP block is critical. When a chip design team seeks to integrate a SerDes IP block into their design, they need multiple levels of validation that the block works as advertised. In the first level of validation, the IP vendor provides samples of the SerDes IP block that other customers have already embodied in silicon. At this stage, the vendor provides the design team with the bring-up and characterization reports for the designs that previously integrated the same IP block. This completes the first level of validation of the SerDes IP for the chip design team.

To assure successful integration, the design team reviews the vendor checklist in detail and jointly completes all necessary tasks. The team then completes the integration and delivers the design to the designated foundry. Following receipt of engineering samples, the design team almost always lacks the sophisticated and specialized equipment to conduct bring-up and characterization processes on the engineering samples. Leading SerDes IP providers offer value-added bring-up and characterization services. The resulting bring-up and characterization reports validate that the SerDes IP block works properly and performs to specification with the other design elements of the chip. ■

About the Author

David DeMaria is a successful executive with more than 25 years of experience in the electronics industry. Prior to joining MoSys, he was a senior vice president at Apache Design Solutions, a technology leader in electronic design automation (EDA). Previously, he was CEO of Optimal Corporation, an EDA company that he helped to grow and, ultimately, merge with Apache. Before that, he held a number of executive positions in leading EDA companies, including eight years at Cadence Design Systems, where he served as executive vice president of the systems business unit and senior vice president of worldwide marketing and strategy. Prior to Cadence, he was group vice president of the systems business at Viewlogic and managing director of Zuken-Redac. Mr. DeMaria attended Boston University for a B.S. degree in computer engineering. You can reach Mr. DeMaria at ddemaria@mosys.com.

GLOBAL MARKET TRENDS

ASIA

\$263.9 million – Revenue generated by the Asia-Pacific electronic design automation (EDA) industry in Q2 2010, a large 41.7% year-over-year (YoY) increase. – *EDA Consortium*

15 – Number of Asia-based companies ranked in Boston Consulting Group's report of the 50 most innovative companies, while 11 Europe-based companies placed. – *Boston Consulting Group*

\$74.7 billion – Amount of capital China plans to spend on the development of new energy industries from 2011 to 2020. – *China Securities Journal*

33.5 million – Expected number of liquid crystal display (LCD) TV sales in China this year. – *RedTech Advisors*

68 – Number of light-emitting diode (LED) wafer and chip fab companies in China. – *Semiconductor Equipment and Materials International (SEMI)*

\$102 billion – Amount expected to be generated from the convergence of the Internet, telecom networks and TV broadcasting networks in China, significantly boosting the region's economy. – *Digitimes Article*

33.8% – LED backlit models' estimated share of total LCD TV shipments in China in 2011, exceeding the share of cold cathode fluorescent lamp (CCFL) backlit sets in 2012. – *Digitimes Article*

\$64.8 billion – Estimated revenue generated by China's semiconductor distributors and suppliers in 2010, up from \$49.5 billion in 2009. – *iSuppli*

500 million – Current number of Internet users in China and

India. The two regions are forecasted to add 700 million more Internet users by 2015. – *McKinsey & Company*

\$213 million – Amount invested in the development of Taiwan's Worldwide Interoperability for Microwave Access (WiMAX) industry and its applications by the Taiwanese government during 2010 to 2013. – *Ministry of Economic Affairs (MOEA)*

84.5 million – Number of wireless local area network (WLAN) devices shipped by Taiwan-based manufacturers in Q3 2010, decreasing 12.2% quarter-over-quarter (QoQ) and increasing 19.4% YoY. – *Digitimes Article*

8% – Estimated compound annual growth rate (CAGR) of Taiwan's information security market during 2011 to 2013, reaching approximately \$760 million. – *RNCOS*

\$11.6 billion – Forecasted value of Indonesia's consumer electronics industry by 2014. This industry is expected to reach around \$7.3 billion this year. – *Research and Markets*

25 million – Estimated number of Internet users in Malaysia by 2015, which is close to 80% of the country's population. The increase in Internet users is driven by the Malaysian government's push to expand high-speed broadband. – *McKinsey & Company*

>40% – Share of worldwide satellite set-top box (STB) shipments that Brazil, China, India and Indonesia will account for in 2010. – *IMS Research*

INDIA

\$101.6 million – Predicted value of India's automotive engineering services market by 2015, growing at a CAGR of 7.9% from 2010. – *Frost & Sullivan*

84% – Current percentage of rural Indians who are unaware of the Internet. – *Internet and Mobile Association of India (IAMAI) and Indian Market Research Bureau (IMRB)*

50% – Forecasted percentage of Indian TV households that will use direct-to-home (DTH) STBs by the end of 2014. – *IMS Research*

10%–12% – Predicted growth of India's mobile devices market in 2010. – *Research and Markets*

8 – Number of venture capital (VC) firms that entered the Indian market this year. Overseas investors are showing interest in emerging markets such as India due to the growing demand for early-stage investment, increasing return and slow global VC recovery. – *SiliconIndia*

72 million – Projected number of mobile social network users in India by 2014, driven by the increasing number of citizens accessing social networking through their mobile phones. – *Analysys Mason*

76% – Percentage of Web users in India who have been victims of cybercrimes such as computer viruses, online credit card fraud and identity theft. – *Symantec*

EUROPE, THE MIDDLE EAST AND AFRICA (EMEA)

\$226.6 million – Revenue generated by the EDA industry in the EMEA region in Q2 2010, up 6.7% YoY. – *EDA Consortium*

47 million – Estimated number of European households with a connected TV in 2014, growing from less than four million in 2009. The number of households with a connected Blu-ray player will soar from five million in 2010 to approximately 66 million in 2014. – *Parks Associates*

\$14.7 million – Estimated revenue of the mobile services market in Western Europe by 2014. – *Parks Associates*

157.6% – Penetration of wireless subscriptions in Western Europe, where there are more subscriptions than citizens. Europeans typically have multiple subscriptions and phones. – *iSuppli*

20% – Predicted revenue growth of the closed-circuit TV and video surveillance equipment market in Russia during 2010 to 2011. – *IMS Research*

4.8 – Number of gigawatts of registered photovoltaic installations in Germany in the first three quarters of 2010, an increase of 327% from the same period in 2009. It is estimated that Germany accounted for 48% of global demand, driven by the intense speculation and debate over the country's feed-in tariffs (FiT) reductions and the subsequent three-step cuts in 2010. – *IMS Research*

50% – Penetration of wireless subscriptions in Africa and the Middle East. – *iSuppli*

THE AMERICAS

>30% – North America's estimated share of the global biometric market this year. – *RNCOS*

>10 million – Estimated number of 3-D TV shipments in North America by 2015. – *ABI Research*

1% – Expected growth of LCD TV shipments in North America in 2010, while another established market Western Europe will see an 8.9% increase. – *iSuppli*

274 million – Estimated number of smartphone users in North America by 2015. – *Parks Associates*

208 – Number of funding deals in Silicon Valley in Q3 2010, a decrease from 288 deals QoQ and 223 deals YoY. – *National Venture Capital Association (NVCA)*

\$3.5 billion – Expected revenue generated from mobile content, which is defined as music, games and video, in the U.S. this year due to the proliferation of smartphones. This market reached \$1.2 billion last year. – *eMarketer*

15%–20% – Percentage of U.S. consumers who are willing to pay a \$5 to \$10 monthly subscription fee for a service that promises savings of 10% on their energy bill. The earliest adopters will be smartphone users and security system owners. – *Parks Associates*

\$175 billion – Expected sales of U.S. consumer electronics in 2010, up 3% from a year ago. Sales are projected to reach \$182 billion in 2011. – *Consumer Electronics Association (CEA)*

61% – Percentage of global media tablet sales that North America will account for in 2010. As these devices become available in more markets, its share will drop to 43% in 2014. – *Gartner*

\$516.8 million – Value of EDA products and services purchased by the Americas in Q2 2010, representing an increase of 1.5% compared to Q2 2009. – *EDA Consortium*

>17.6 million – Number of PC shipments sold in the U.S. in Q3 2010, a 2.2% increase from Q3 2009. – *Gartner*

10% – Forecasted growth of TV services in Latin America through 2014. This expansion is fueled by growth in the region, technological innovations and changes in TV service regulations. – *Parks Associates*

55.1% – Projected growth of LCD-TV shipments in Latin America in 2010, led by Brazil. – *iSuppli* ■

MAXIMS: DATA, DECISIONS, REACTION RATES — HOW EACH DEFINES MARKET SHARE GAINS IN AN UPTURN

G. DAN HUTCHESON, CEO AND CHAIRMAN, VLSI RESEARCH INC.
DOUGLAS G. ANDREY, DIRECTOR, SEMICONDUCTOR MARKETS, VLSI RESEARCH INC.

While the semiconductor industry has been at the core of a profound transformation in technology and the economy, an enduring—but not endearing—part of the industry has been the market cycles that have characterized the business.

A fundamental principle of high-tech leadership is that downturns are used to build platforms for future market share gains. During a downturn, a company should focus on product development. Then, once the bottom has passed, the most important decision a company can make is when to expand. One can only hit a home run by swinging when the ball passes over the plate. Once the ball has flown into the catcher's mitt, it is too late. It takes time to get suppliers aligned with their customers' needs. Hit the ball and a customer's suppliers will be there to serve them. Fail to swing and they will see somebody else while the customer waits for the next pitch.

Major factors that drive the semiconductor industry's cyclical nature are end user demand, capacity, supply chain inventory and latency in data and decision making that accompanies each tier. Just-in-time and pull manufacturing have eliminated the information gaps on the supply side.

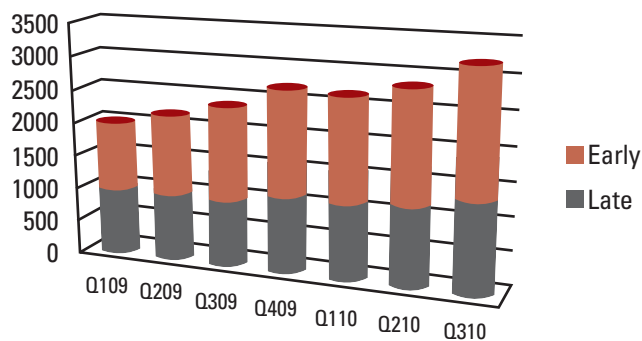
However, huge information gaps remain on the demand side—even to the degree that the actual market picture typically does not emerge for months or even a quarter. In the digital age of manufacturing, the demand side's picture taking resembles the imaging process in the old film processing days where one would have to wait for a picture to develop.

Understanding where the company is in the cycle and what actions to take are fundamental to the success of any semiconductor company. So what is the best way to know when the cycle has indeed turned upward? More importantly, when is the appropriate time to make the hard decision of ending a cost control regime and unleashing the organization for growth? Let's start by looking at the latest cycle.

In 2009, as the upturn came, there was a six-month difference between the earliest and the latest decision makers. The difference

was critical to their performance. To avoid pointing fingers, say two competitors were equally at a \$1 billion quarterly run rate in Q2 2009. One decides to ramp in the second quarter and the other waits until the third quarter. As a result, the early bird gets an 8 percent market share boost and, more importantly, they hit the sweet spot of a turnaround's early high-growth quarters. By Q3 2010, using only the market growth rate, the early bird achieves revenues of \$1.9 billion while the late bird achieves \$1.4 billion. The cumulative difference over the entire period is \$2.4 billion or 30 percent of the late bird's cumulative revenues over the period. So even if the early bird does not develop a spectacular product and only grows with the market, they will still get the biggest share.

Figure 1. The Early Bird Decision Opportunity

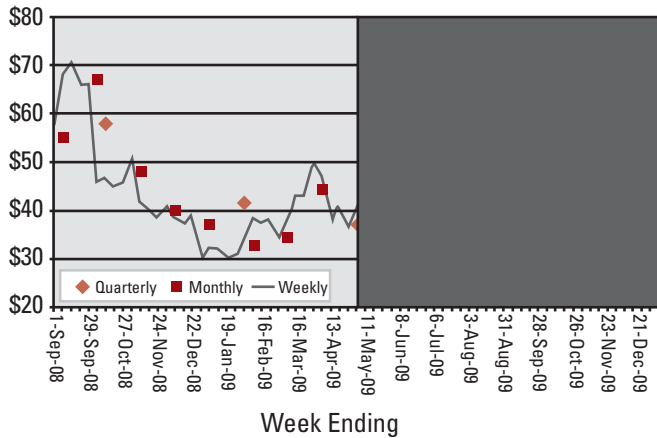


Source: VLSI Research Inc., 2010

While the math is easy, making the decision to pull the trigger on transforming the business into a high-growth company is not. Jump too early and it can be costlier than jumping late. A company can easily be the first mouse to the trap, and the second one will get the cheese. This is a gut-wrenching decision for even the most seasoned semiconductor executive. The only way to calm the emotional content of this decision is with better data. Better data leads to better decisions and, ultimately, better results.

A company gets three strikes when it comes to data: quarterly, monthly and weekly. To understand why this is important, let's go back to late April of 2009. It was on September 15, 2008 that Lehman Brothers filed for Chapter 11 bankruptcy protection, quickly after which IC sales began a steep decline. By late April, there was two, maybe three, quarterly data points to look at, all of which showed a steady decline.

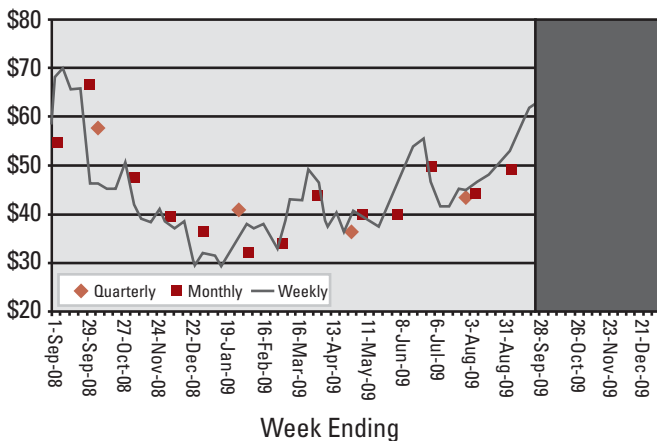
Figure 2. The Data Picture: Quarterly, Monthly & Weekly (IC Sales, Quarterly Run Rates, \$B, By Time of Data Availability)



Source: VLSI Research Inc., 2010

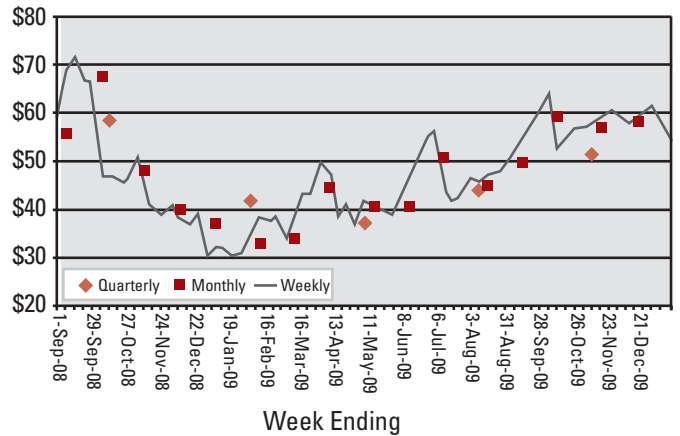
When looking at monthly data, there still was only two positive data points. But when looking at weekly data, there was a clear bottom 13 weeks before. Fast forward to late September when the late birds first recognized that there was an upturn, and the quarterly results still only showed a single positive period. But by then, it was clear from the monthly data that an upturn had occurred. The problem is that the big growth was over as Figure 4 shows. Worse, a semiconductor company's ability to run at market rates of growth was severely hampered. This is because they lost more of the early original equipment manufacturers' (OEM) design wins since they were not responding aggressively. If a semiconductor company's manufacturing was outsourced and they were not in the foundry order line, they simply could not get the wafers needed to respond. If they were a foundry and were not in the semiconductor equipment order line, they simply could not get the advanced node tools needed to respond.

Figure 3. The Data Picture: Quarterly, Monthly & Weekly (IC Sales, Quarterly Run Rates, \$B, By Time of Data Availability)



Source: VLSI Research Inc., 2010

Figure 4. The Data Picture: Quarterly, Monthly & Weekly (IC Sales, Quarterly Run Rates, \$B, By Time of Data Availability)



Source: VLSI Research Inc., 2010

Companies could have, and should have, been looking at their internal weekly data. If the executive of a company believes they are still in a downturn, the organization will believe it too and will not respond. The company's internal weekly data will mostly just confirm their opinion that the upturn has not arrived. They need an external reference point to know they are falling behind. More importantly, the source of the external reference point must provide weekly data with less than a week of latency. That is why VLSI Research has put so much effort into providing weekly data. ■

About the Authors

Dan is CEO and chairman of VLSI Research Inc. as well as the director of several Website businesses, including weSRCH.com. His career spans more than thirty years, in which he has become a well-known visionary for helping companies make businesses out of technology. This includes hundreds of successful programs involving product development, positioning and launch. Dan is a recognized authority on the economics of innovation and has a proven track record of accurately predicting trends using the economic models he develops. He has authored numerous publications on the strategic and tactical aspects of how to succeed in the business of technology. He has also been the keynote or invited speaker at dozens of conferences. Dan is arguably best known for his forecasting of strategic infrastructure shifts and his early-eighties development of the first factory cost-of-ownership models, which are now the basis for most large-scale capital decision-making.

Doug Andrey, director of semiconductor markets, focuses on the research and analysis of semiconductor markets and the market dynamics affecting semiconductor suppliers. He is responsible for supervising the research, analysis and reporting of semiconductor key performance indicators. This includes trend evaluation, statistical analysis, analyzing collected data and semiconductor market forecasting. Mr. Andrey also participates in client advisory activities. Prior to his current position at VLSI Research, Mr. Andrey held various positions focusing on market statistics and research. Most recently, Mr. Andrey was a market research manager at SanDisk Corporation, where he was responsible for key market research programs identifying opportunities for market share gains. He was also in charge of SanDisk's data acquisition programs and market analyst relations. He joined SanDisk from the Semiconductor Industry Association (SIA), where he was responsible for the World Semiconductor Trade Statistics (WSTS) program and internal market research to member companies. Mr. Andrey is a graduate of the University of Santa Clara, where he obtained a B.S. in information science and a MBA in marketing.

DisplayLink specializes in chips and software that enable easy virtual graphics connectivity between computers and displays over standard interfaces such as Universal Serial Bus (USB), wireless USB and Ethernet. With more than three million global users, DisplayLink's semiconductor and software technology is used in dozens of Tier-1 branded PC accessories found in most major channel outlets, including monitors, docking stations, display adapters, projectors and zero client systems that enable the expansion of the desktop visual workspace at significantly lower cost and energy than traditional solutions.

DisplayLink technology combined with major industry advancements, such as USB 3.0, will unleash a new level of interactivity and has the potential to enable any device to share media freely with any display using standard networks.

Recently announced, the new DisplayLink single-chip family, DL-3000 and DL-1000 series, will include integrated display and networking connectivity, high-performance audio and high-definition (HD) video support, as well as third-generation DisplayLink adaptive real-time compression technology that dynamically manages bandwidth and takes full advantage of bi-

directional throughput of SuperSpeed USB. This means multiple full HD videos, high-resolution graphics and networking data can be processed simultaneously while also substantially increasing today's HighSpeed USB (USB 2.0) graphics performance and enabling graphics delivery over gigabit Ethernet.

With more than 120 employees in Silicon Valley, the United Kingdom, Taiwan and Poland, DisplayLink technologies and successes have garnered numerous industry awards including the number two spot in the Deloitte Technology Fast 50 2010. ■

"DisplayLink is keenly aware of the importance that associations play in developing standards and best practices for major technology ecosystems. Our GSA membership is extremely valuable, as our company's success is predicated on leveraging accepted industry standards to develop products that ultimately meet the needs of end consumers."



– Dennis Crespo, Executive Vice President, Marketing & Business Development, DisplayLink

Craig Ensley, CEO
 Scott Tandy, Chief Strategy Officer & Executive VP
 Guy Gibson, CFO
 Dennis Crespo, Executive VP, Marketing & Business Development
 Tim Glauert, Co-founder & Chief Technologist, Software
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THIS SECTION IS DESIGNED TO ACQUAINT READERS
private showing
 WITH GSA'S PRIVATE SEMICONDUCTOR MEMBERS

Quantenna's latest third-generation Full-11n 4x4 multiple-input multiple-output (MIMO) Wi-Fi chipsets offer industry-leading reliability and whole-home coverage for delivering carrier services over wireless networks. The company's 802.11n chipsets are in trials with more than 12 carriers worldwide for broadband digital video services that require robust performance anywhere in the home.

4x4 MIMO delivers more than double the throughput of earlier 3x3 MIMO technology with better reliability. Quantenna's Full-11n chipsets offer carrier-grade industry-standard 802.11n features as well as dynamic digital beamforming, mesh networking and channel optimization. These features are essential for delivering up to four high-definition (HD) video streams at more than 100 Mbps data rates, over 100 feet, at full, 1080p resolution with near-zero packet error rate (PER) data transfers, despite a home's signal impairments and dead zones. Quantenna's chipsets enable Wi-Fi home networks to deliver the same quality as wired Ethernet plus compatibility with existing and future Institute of Electrical and Electronics Engineers (IEEE) 802.11n-compliant products.

Products and services using Quantenna's Full-11n chipset are available at retail stores and through carriers, and enable carriers to deploy triple-play, Internet protocol television (IPTV) and full HD video programming services while reducing support requirements and minimizing truck rolls and deployment costs. They also enable carriers to support new service models such as centralized, multi-channel digital video recorders (DVRs), remote DVR/set-top box (STB) maintenance, digital rights management, and content/privacy security.

Quantenna recently closed a \$21 million Series E financing round led by new investor DAG Ventures with participation from existing investors Sequoia Capital, Sigma Partners, Southern Cross Venture Partners and Venrock Associates. The funding is being used to accelerate product deployment through carriers and retail channels worldwide. Quantenna has now raised more than \$80 million to date. ■



"Quantenna is proud to have joined the world's premier semiconductor industry organization, and as a former board member, I'm personally pleased to be re-connecting with GSA and its many fine members. We are committed to playing a very active role in helping GSA continue its mission to foster start-ups into established semiconductor companies."

– David French, Chief Executive Officer, Quantenna

David French, CEO
 Behrooz Rezvani, Founder, President & Chairman
 Lionel Bonnot, VP, Sales
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A TIERED MANUFACTURING STRATEGY: THE NATURAL SOLUTION FOR A HIGH-PERFORMANCE MIXED-SIGNAL COMPANY

CHRIS BELDEN, EXECUTIVE VICE PRESIDENT AND GENERAL MANAGER, OPERATIONS, NXP SEMICONDUCTORS

Many major industries regularly experience the sort of cyclical change that requires all players to consider their own operational approaches and competitive strategies. The semiconductor industry is undergoing such continuous change. In the past decade, the face of the industry has dramatically altered. Vertically integrated semiconductor companies have been increasingly outsourcing substantial parts of their needs, fabless start-ups have grown into multi-billion dollar industry leaders, and the move to deep-submicron CMOS with multi-billion dollar wafer fabs has led to the consolidation of deep-submicron manufacturing into a small set of players, which include some of the leading independent foundries.

Many viewed this as inevitable, with a raft of predictions that consolidation would occur even amongst some of the largest, most established industry titans. However, in reality, there has been more de-consolidation than consolidation. Many diversified companies have chosen to increase their focus on their “core” and have deprioritized activities where there is no other path to leadership positions. A number of integrated device manufacturers (IDMs) have spun-off their memory businesses, a discrete semiconductor business

has been set-up as a separate entity and numerous players have chosen a more targeted approach in forming specialized companies.

During the depths of the recent financial crisis, the primary question concerning the industry was whether the economic challenges would trigger the further acceleration of these semiconductor trends and lead to a massive shakeout across a number of technology markets. This did not happen, but companies are realigning their product market focus and resetting the course towards market segments which offer greater revenue streams, market share growth and potential for differentiation. The incredible proliferation of semiconductors in almost every single application, device and service in society has led to a more diversified market with a huge number of multi-billion dollar market segments. The diversification of semiconductor applications is driving changes in the strategies of suppliers that are much more complex than textbook theories on consolidation, and in the mono-cultures of fabless companies and foundries.

These market opportunities and challenges have led the entire industry to consider whether their traditional manufacturing

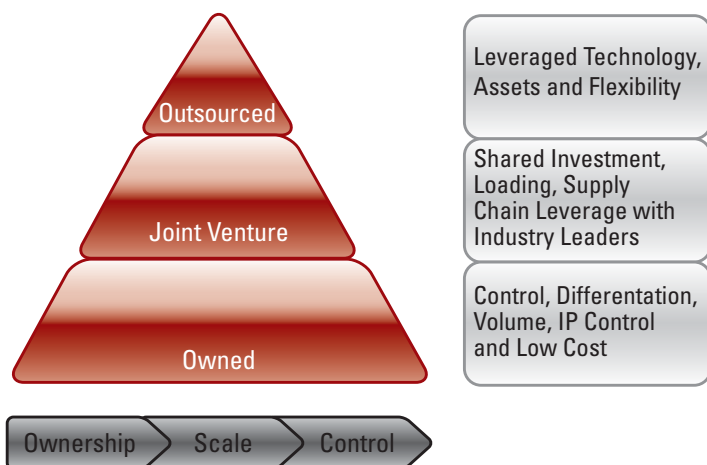
strategies are future-proofed, and have resulted in some firms embracing either an in-house or fully outsourced manufacturing path, with others adopting a hybrid approach.

Mapping Business and Manufacturing Strategies: Introducing the Tiered Manufacturing Strategy Model

A focused manufacturing strategy needs to support a focused business strategy—one that addresses real market demands. Today’s engineers are not focused on pushing the Moore speed envelope, but want to be able to combine analog and digital circuitry to optimize designs and achieve the greatest precision, highest bandwidth or lowest power consumption. They are demanding integration, enrichment and a complementary—not limiting—development route. The area to meet this need and that focuses on bringing the best of both analog and digital capabilities to the customer via the engineering community can be defined as high-performance mixed-signal.

For a high-performance mixed-signal company, it is vital to both secure the availability of optimized process and packaging technologies, and to have a flexible and competitive supply chain to fulfil customer demand. While value can be achieved from an outsourced approach for standard technology platforms, in application-focused markets where engineers are demanding more than speed alone, it is proprietary specialty processes that provide real differentiation and platforms for long-term technology leadership. With the combination of staying in control of proprietary specialty processes and a strong network of joint ventures and partners to create a “tiered manufacturing strategy,” benefits can really flow through to the entire community of engineers, customers and end users.

Figure 1. A Tiered Manufacturing Strategy: Balanced Control, Scale and Leverage



The Tiered Manufacturing Model in Practice

There is great value that can be created through teaming with key partners and realigning a tiered manufacturing model to meet an overall strategic direction and, most importantly, to support the needs of customers. To show how a tiered manufacturing process can accomplish this, the practices of a leading IDM in today’s industry will be examined.

Example

The IDM supplies about 60 billion products per year, based on about two million (8-inch equivalent) wafers, with a quality level of less than 0.50 ppm for complex products. The vast majority of these

products (85–90 percent) are manufactured in-house, with 10–15 percent outsourced to leading wafer foundries and assembly and test providers.

In recent years, the IDM has developed a leading-edge portfolio of specialty manufacturing processes, ranging from advanced embedded Flash technologies through LDMOS and RF-BiCMOS technologies up to SOI-based high-voltage and power processes. Many of these technologies are applied across multiple business segments (e.g., Flash for identification, microcontroller units (MCUs), and SOI for automotive applications and power and lighting solutions).

The segmentation of specialty technologies and general-purpose technologies cannot be mapped one-on-one to the segments of the IDM’s manufacturing sources: Specialty processes are run within in-house fabs, in joint ventures and in pure outsourcing mode where the IDM sometimes develops proprietary options on a commercially available platform. So although the IDM does not own any 300 mm fabs, the label “fabless” would be too simple for its activities in the 300 mm space, as it continues to drive the technology portfolio to meet the specific high-performance mixed-signal customer requirements.

Joint ventures with leading external manufacturing companies have been and will continue to represent one of the pillars of the IDM’s manufacturing strategy going forward.

Alongside the joint ventures, the IDM works with many foundries and subcontractors in a pure outsourcing model to benefit from the capabilities and competencies of partners such as TSMC, ASMC, GlobalFoundries, ASE and Amkor.

This provides the basis of a tiered manufacturing model which the IDM will further expand to support its growth in years to come: It will continue to manufacture in-house, but will also grow the network of joint ventures and outsourcing partners. Furthermore, it will continue to optimize its technology portfolio across the manufacturing network to meet engineers’ high-performance mixed-signal needs.

Driving Change

As mentioned previously, many major industries experience the sort of cyclical change that requires all players to rethink their own operational approaches and competitive strategies. The semiconductor industry is undergoing such continuous change. In this dynamic industry, the IDM examined has worked continuously over the last couple of years to develop a tailored and refined manufacturing strategy that will enable it to focus on and grow its high-performance mixed-signal business, while driving innovation in this area. This requires the right and, necessary, blend of in-house manufacturing with dedicated proprietary technologies, complemented by selective and strategic outsourcing partnerships establishing this “tiered” manufacturing strategy. ■

About the Author

Chris Belden is executive vice president, general manager of operations and member of the NXP management team. He joined NXP as senior vice president of global manufacturing in March 2008. Previously, Mr. Belden worked for Applied Materials Inc. where he was responsible for global operations. Before that, he spent the majority of his career at Motorola Inc. and Freescale Semiconductor Inc., where he was responsible for Freescale’s global manufacturing operations.

An inside look at innovative semiconductor start-ups

In 2010, remarkably few semiconductor start-ups received early-stage venture financing. Semiconductor investing has simply fallen out of vogue compared to the onslaught of investment in green tech and cloud computing. So it's reasonable to surmise that the few deals that have received funding this year must be special, or at least indicative of some significant trend.

EnVerv and **Calxeda (formerly Smooth-Stone)** both received Series A funding in 2010. That makes them part of a rarified crowd. There may be one or two others, but not many. Why did they receive funding versus so many others that tried? We won't know the full story, as both companies are early-stage "stealth" deals. But we can make a few observations.

EnVerv was founded to develop power line communication (PLC) systems-on-chip (SoCs) for smart grid applications. In Q2'10, the company raised \$6 million in initial funding from New Enterprise Associates and Walden International. The smart grid market is hot and represents a rapidly growing market opportunity. The electricity meter opportunity is a 130–150 million unit market. Twenty percent of this is forecasted to be accounted for by advanced metering infrastructure (AMI). It is estimated that by 2016, the electricity meter market will reach 220–245 million meters per year, with over 90 percent of them AMI. EnVerv is also focused on the intelligent lighting market, which the company believes will be a far larger opportunity.

EnVerv is squarely focused on the wide area network (WAN) market, not the home area network (HAN) market. EnVerv's premise is that today's PLC devices are not robust enough to support grid-scale WAN requirements. Unlike existing devices, EnVerv's PLC chips are based on real-world communications theory and signal processing expertise. The company argues that it will be the first vendor to introduce truly robust devices based on its signal processing edge; expertise in very high bit-rate digital subscriber line (VDSL), cable modem, Multimedia over Coax Alliance (MOCA) and 4G Worldwide Interoperability for Microwave Access (WiMAX) signal processing; test and measurement/calibration expertise; and communications/integration expertise. EnVerv is currently engaged with tier-one customers worldwide.

Calxeda, the second company mentioned, was founded in January 2008 "to bring ultra low-power mobile phone technology to the datacenter." In August 2010, Calxeda raised \$48 million from a syndicate comprising ARM, Advanced Technology Investment Company (ATIC), Battery Ventures, Flybridge Capital Partners, Highland Capital Partners and Texas Instruments. ATIC, also the primary investor in GlobalFoundries, is a technology investment company wholly owned by the Government of Abu Dhabi. That's a

huge funding round. And there's a few interesting investors in the syndicate—notably ARM, TI and ATIC.

Today's data centers rely on the age-old x86 architecture, which may not be optimal for cloud computing workloads. Calxeda argues that there is pent-up demand for data center platforms that offer significant improvements in performance from both the energy and density perspectives. Calxeda's technology, combined with ARM's architecture and tools, will provide significant improvements.

Calxeda will bring the low-power virtues of mobile phone technology to servers and data centers. The new capital will be applied to the final development and market delivery of high-performance, low-power chips "that will change the server market and the makeup of data centers."

Now you can see why ARM invested—it gets its fingers into the server market. And ATIC/GlobalFoundries needs to fill up its foundries. TI's OMAP processor is based on ARM, and we can certainly understand TI having keen interest in the server arena. No matter how you look at it, data centers and cloud computing are exploding, and any technology that provides significant benefits has obvious appeal. ■

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CHIP DESIGN: A OUTSOURCE DECISION

SANJAY KRISHNAN, BUSINESS MANAGER, HIGH-PERFORMANCE ANALOG DIVISION, MAXIM INTEGRATED PRODUCTS

Outsourced semiconductor manufacturing is well established, as witnessed by the thriving fabless business model. Pure-play silicon foundries such as Taiwan Semiconductor Manufacturing Company (TSMC) generated about \$25 billion in revenues in 2009, and are expected to grow faster than the overall semiconductor industry.

The rapid growth of standardized CMOS manufacturing since TSMC was established in 1987 has allowed chip companies to focus on creating value through circuit design. As these design techniques and blocks have become standardized, semiconductor executives have wondered if chip design might itself become outsource-able.

In this article, these factors will be explored in depth, and other important issues such as quality control, intellectual property (IP) and alternative business models such as revenue sharing and joint ventures for outsourced chip design will also be looked at.

Chip Design Outsourcing

According to a Gartner survey of 35 IC design services vendors, the total number of chip design starts fell by 15 percent in 2009. However, the share of outsourced design starts grew, and design services revenue associated with those starts grew by 18 percent over the previous year. In a year that was affected by a global economic recession, this indicates a strong economic value provided by IC design services firms. If the quality of the work they perform meets expectations, it is likely that the share of outsourced chip design will continue to grow, even when the economy picks up.

Decision Parameters

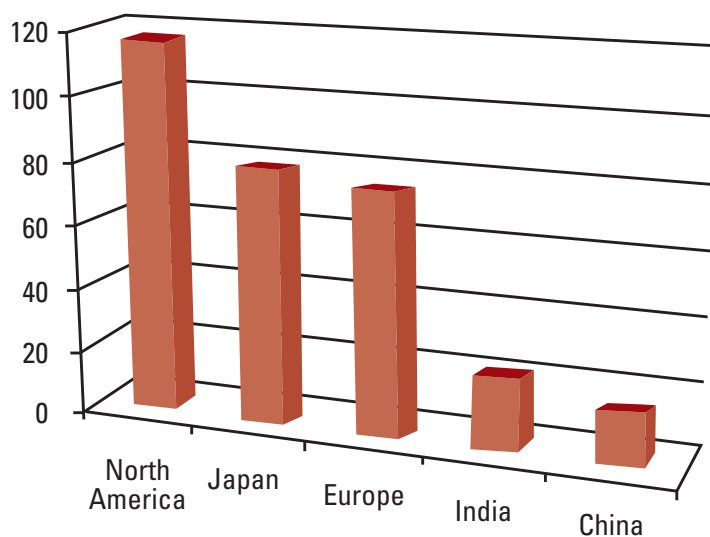
The three often stated and analyzed parameters that inform the IC design outsource decision are:

- Cost: measured in research and development (R&D) dollars spent on chip development.
- Time-to-Market: measured in months, from chip definition to sample.
- Expertise: measured in chip performance and number of redesigns (“passes”) required.

Cost

Semiconductor R&D budgets typically range from 20 percent to 40 percent of gross revenues, higher than most industries. The major component of this budget is engineering salaries. This fact has motivated chip design companies to seek out talented engineering teams in lower cost countries—India and China being the main contributors.

Figure 1. Engineer Salaries (US\$ Per Year)



Source: EE Times, November 30, 2009

The cost advantage of salaries does not take into account the level of experience of the engineers in the survey, which for the U.S. and EU are more than twice the number of years as the engineers from India and China, and likely to be much higher. Adjusting for years of experience, the ratio of 5:1 salary (Figure 1) between developed and emerging economy electrical engineers is likely to be closer to 2:1.

The cost advantage has become less significant over time. India- and China-based design teams have been designing larger and more complex chips and architecting software that goes with the system. Core competencies have been built in these countries for customizing intellectual property (IP)—software or hardware—to enable low-cost, rapid and reliable chip development.

Time-to-Market

A familiar problem for semiconductor companies serving fast-changing consumer electronics markets is the hyper-aggressive tape-out schedule to meet a customer's market window. In such situations, complementing internal design engineering with external partners is an easy and good decision to make. Unfortunately, for design services firms, such engagements are stop-gap measures and often restricted to physical design activities which are often considered non-core functions by IC design houses.

Silicon-proven IP can speed up time-to-market, and design services vendors often provide such IP blocks on a fee-based (non-recurring engineering (NRE)) or royalty basis. Customizing IP for specific applications tends to be faster than developing from scratch, which translates to a time-to-market advantage.

The need for faster time-to-market is often seen as a breakdown in the product planning process within a semiconductor company. This results in the need for higher management approval for outsourcing chip design. Lastly, even a successful delivery of results by a design services partner does not always result in repeat projects.

Expertise

The least encountered reason for outsourcing chip design has been the lack of internal expertise. This has traditionally been due to chip design companies seeing their core expertise in circuit design rather than chip definition. However, chip design has become a multi-layered and complex problem requiring expertise from the architectural level to transistor level. Many smaller chip companies and virtually all start-ups benefit from an ecosystem of vendors who provide services in areas where they themselves lack expertise. A typical digital chip design can be expected to contain memory, input/output (I/O) structures, phase-locked loops (PLLs) for clocking and standard cells, all of which are routinely developed by companies that specialize in such IP. Design services firms may additionally design custom circuits for a particular chip.

Other areas of chip design expertise include testability, design for manufacturability (DFM), test vector design, yield improvement and circuit redesign for smaller geometries (optical or functional shrink). For companies that are too small or further removed from the chip design itself, the design services firm provides a turnkey solution that includes foundry selection and packaging and test services: The final delivery is a working chip.

Turnkey solutions in chip design are the most valuable type of engagement from the expertise angle, and most likely to generate trust and repeat business. But once again, the outsource decision needs executive approval and a strategic reason that is more powerful than the reasons seen so far. Unless outsourcing is part of the business model of the chip company, questions regarding IP protection, control, quality assurance and long-term maintenance of the IP will be difficult to overcome.

R&D as a Variable Cost

Large semiconductor design firms implicitly consider another important factor, the flexibility of R&D budgets. Revenue fluctuations due to economic volatility or market mistiming can cause cash flow volatility, which can be reduced by more flexible R&D budgets. This is an incentive to outsource part of the R&D budget, which allows for faster reaction times than the traditional method for laying off and re-hiring engineers. From an industry point of view, this merely shifts the volatility between firms; however,

design services firms are better equipped to handle this as they work with multiple customers across multiple end markets and can benefit from the diversification this allows.

The Future of the Outsourced Chip Design

Market reports have shown increased chip design outsourcing trends in tough economic times. As the industry discovers effective partners for outsourcing, these partnerships will remain and grow in strength even in good economic times.

However, the greatest threat to this trend comes from the design services companies themselves: some provide design services with a long-term aim of manufacturing the branded chip themselves. Many hungry chip design start-ups are willing to perform design services to feed the product development that they see as the ultimate profit generator.

In response to this threat, chip design outsourcing will be a more sustainable industry trend if:

- Design services firms can assure their customers that they will not compete or aid their customer's direct competitors. This has been possible in the case of India-based outsource partners who have established a credible business modeled on the software outsourcing industry. Design automation firms are also possible candidates for such partners, although previous attempts in this area have had limited success.
- Contracts can be structured where profits are shared with the design services firms. By sharing risk and reward, this creates better long-term incentives for both partners in the outsource value chain. A joint venture is an example of such a contract, where the scope of the agreement can be easily defined and the outputs measured.
- Chip design outsourcing is motivated by a strategic evaluation of a chip company's core competencies, and not as a solution to a problem of cost, time-to-market, lack of expertise or budget crunch. Few engineering-led semiconductor design companies today are ready to give up their core strength in designing chips in the immediate future. Due to this, IP sub-block design services will have a hard time emerging in the way the automobile industry spawned an ecosystem of parts suppliers around major car manufacturers.

With the growing architectural complexity of a system-on-chip (SoC), the trend towards buying blocks of IP rather than designing from scratch will increase. Chip design outsourcing today makes more sense, from the perspective of separating system and circuit expertise rather than from the perspective of cost alone, another trend that will strengthen. The beneficiaries are IP vendors who will strengthen their silicon-proven offerings, SoC design services firms that can integrate and customize such IP, and the users of IP who will gain a valuable time-to-market advantage. These trends could, in fact, be accelerated by emerging companies in China and India. ■

About the Author

Sanjay Krishnan is the U.S. chair of GSA's Analog/Mixed-Signal Working Group. He is a business manager in the high-performance analog group at Maxim Integrated Products (NASDAQ: MXIM). Since 1998, he has worked at semiconductor and design automation companies in engineering and business roles and has advised technology start-ups. He can be reached at sanjay_krishnan@mba.berkeley.edu or 858-344-1340.

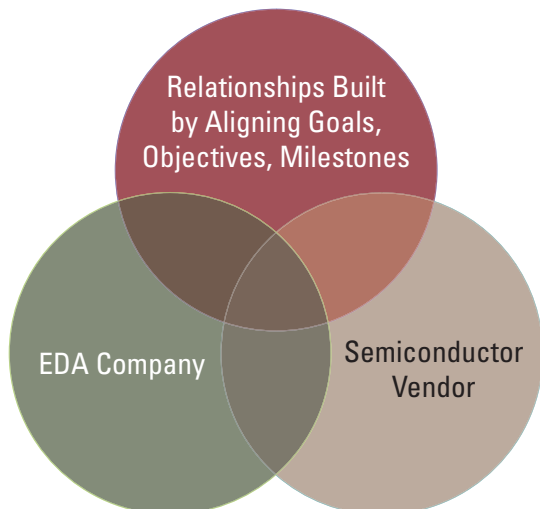
EDA AND THE GLOBAL FABLESS VENTURE: SHARED DESTINY

RON BURNS, VICE PRESIDENT, SALES, EVE

Over the last 10 years, electronic design automation (EDA) companies have tried various methods to partner with new ventures, but not without re-occurring fundamental challenges. New ventures, by their nature, are exciting and cutting-edge, but limited in tool volume and revenue. A variety of approaches have been taken, including investments and lower venture pricing (perhaps also with reduced support). Remember the pre-telecom days? But at the end of the day, EDA companies are not venture capitalists, and after a few failed attempts, the sector has returned to square one.

Fabless and, often, small semiconductor companies need EDA's support and technology access. As EDA moves slowly out of the latest catastrophic meltdown, it's more important than ever to consider that fabless semiconductor ventures and EDA companies have a shared destiny and must find new ways to partner.

Figure 1. A Shared Destiny



Semiconductor ventures need the support and technology access from EDA vendors. The two have a shared destiny and need to find new ways to partner.

After “The Great Idea”: Challenges for Today’s Young Venture

The key to success for today’s young venture is innovative technology.

In the quest for funding, new ventures are finding that investors are making fewer bets and demanding more progress at every milestone. The “great idea” must now be on a fast track to scalable revenue.

And with the globalized distribution of markets and talent, new ventures are scrambling to make critical decisions quickly. What is the company’s core capability, including intellectual property (IP), and what is it enabling? How is the company attracting early adopters or first customers?

One of the most difficult and critical core technology decisions a fabless company must make is whether to develop or source IP. Many large EDA companies are building IP portfolios that new ventures may find useful, but these ventures may not have the resources available to buy the IP. Alternatively, some companies will license IP for the duration of the project, while other more creative firms will allow a start-up to mix in and out certain pieces of IP over the project’s lifetime under the same license.

Another difficult task is building a world-class development team that is increasingly globalized. Multi-core system-on-chip (SoC) design and its complexity drive fabless ventures to quickly scale software and hardware teams. External development partners can play a role, particularly in enabling technology. Software frequently falls into this category.

As a result, it’s common to see design teams spread over three or more continents. There are numerous examples of a vice president of engineering in one location, such as Silicon Valley, with hardware development split between Silicon Valley and another Asian, European or North American location. Software engineers can be anywhere—India, South Africa, Australia, etc.

Because investors are making fewer bets, access to design teams is critical and accelerated. Many times, they are courted when developing the first concept; and once aware, perhaps alone or

with other investors, they are involved in tracking and evaluating a venture's progress. If successful, the semiconductor SoC may be the key competitive lever needed to swing a market.

What the EDA Sector Really Wants

Often, an EDA vendor can relate to these challenges and, with some creativity, help a fabless start-up address them. Many EDA players have spent time with fabless start-ups and have enjoyed working with them. But most secretly hope that these companies will either become big fast or merge with a large customer, carrying praises of their EDA supplier's technology with them. And it is hoped that special business models, if provided, will be balanced by lower support costs.

As new fabless ventures look at EDA and EDA looks at new fabless ventures, there may be other synergies identified that both are missing, and values both can gain in the short term and long term by working together.

EDA + Venture 3.0: Where to Now?

It helps to consider the fabless venture as a partner and align the project to the start-up's specific goals, objectives and milestones. EDA and new ventures have a number of interesting relationships that can develop:

EDA Access Models

The EDA industry has adopted time-based licenses, even where sophisticated systems operate in server mode for global projects. There is also more interest in remote access models, particularly in the case of technologies involving hardware-like acceleration and emulation, but also if the EDA vendor is involved in the design itself.

Design Services

Design services have been offered to fabless companies in the past, but with varying degrees of success. While new ventures have traditionally been more open to design services, the cost of sourcing models from local geographies, particularly in the U.S. and Europe, has been too high.

In a Generation 2 (Gen 2) model, ventures went directly offshore or contracted design services from companies like Wipro, Mindtree and others specializing in design implementation. There were numerous success stories, but, clearly, going global was complicated and required processes and commitment. The industry is in a Generation 3 (Gen 3) model now, where the ecosystem of EDA companies, fabless companies, silicon providers and IP providers are all global at some level. The reality is that on any given project critical talent is available both locally and globally if the right management and communication channels are in place. A key value that an EDA company can offer in the Gen 3 model is the ability to require a much smaller scale of business than a larger offshore design partner, provided tools and IP are part of the relationship.

Some firms have begun offering their EDA core competency as either software or hardware and tool methodology services, and working with an external design services firm. This trend can be modeled as a partnership between the EDA company and the design services firm, or the start-up will employ both companies separately and expect them to work cooperatively.

Co-marketing

The opportunity for co-marketing is often overlooked when building a strategy for working with a new venture, but should be factored into the EDA company's objectives during project planning. Public

marketing with joint demos; participating at events for shared lead development, news releases, datasheets and other marketing collateral; and sharing mailing lists is obvious. This, of course, comes once the venture wants to be visible and has launched its product.

Many EDA companies know from experience the value of featuring clients at major trade shows such as the Design Automation Conference (DAC) and GSA's Emerging Opportunities Expo & Conference. Furthermore, there is an opportunity to invest in creating a true information bridge that spans from the semiconductor venture to the EDA provider and original equipment manufacturer (OEM). While EDA companies have traditionally focused on DAC-like events, perhaps more important are events that connect the entire ecosystem. An example is the Mobile World Congress held each year in Barcelona, Spain that attracts the entire telecommunications value chain, from service providers through telecom OEMs and the semiconductor industry that supports them.

When the venture is in stealth mode, EDA can support these companies in less visible ways:

- Introductions can be made to third parties or potential investors.
- Partners can support each other's development efforts under a non-disclosure agreement (NDA). When working with a partner who's testing a new technology, both the start-up's engineering team and the EDA company's support group can offer insight and feedback on the technology, leapfrogging the company ahead of the competition on a feature set it may not have.

When a stealth mode start-up and an entrepreneurial EDA company have forged a tight, solid working relationship, the goal is to develop a bond and level of trust. While the start-up is unwilling to talk publicly about the relationship and how it's employing the EDA tools, it may talk privately to its development partners. Once the start-up launches its products, that relationship will likely evolve into a more visible endorsement.

Co-development

Co-development is another area worth exploring. While it is difficult on a core flow, it is possible for enabling IP, models and technology. An example is verification IP. The component that comes standard with the system is modeled where the start-up has the ability to create its own, based on the original IP.

Many IP companies have done cross-licensing deals for internal semiconductor IP. The potential to collaborate with companies to co-create and drive new IP in real time for emerging standards is great.

The Road Ahead

The effect of globalization beyond shifting markets and teams offers a chance for EDA to collaborate with new ventures in new ways. EDA and fabless companies can co-create products, and EDA companies can bring these enabling products to market. This helps lower development tool costs for new ventures as technology is pushed further. EDA and these new global fabless ventures are not only interconnected, but also, in some respects, bound by the same destiny. ■

About the Author

Ron Burns is vice president of sales at EVE. He has a distinguished career with more than a 20-year proven record of success in executive management, sales and marketing. Prior to EVE, Burns served as general manager of Wipro Technologies' semiconductor and system solutions business unit. Burns holds a MBA from Santa Clara University in Santa Clara, California and a Bachelor of Science degree in electrical engineering from the University of South Florida in Tampa, Florida. You can reach Ron Burns at rburns@eve-usa.com.

Fresco's solution has the unique flexibility to service all standards and non-standards, which is a big deal in China. Fresco's technology can completely reconstruct any bandwidth signal and reject adjacent channels perfectly. Our design's flexibility enables our customers to seamlessly serve various regions that are in different transition stages. Although Fresco's initial target was the EU, customers have successfully shipped our products to every area in the world. We have hybrid chips in televisions in Europe, North America, Brazil and the Asia Pacific.

Q: *An analyst recently lowered its Q4 2010 revenue estimates for three large analog/mixed-signal semiconductor companies, indicating that the analog industry may be slowing down. Is Fresco also seeing this trend? If so, what do you attribute this slowdown to?*

A: While we have seen some dramatic shifts in market share in the TV space, the softness of the analog industry is primarily an outcome of inventory correction (as a result of overbooking) which always occurs during allocation periods. This is a cyclical problem that the industry will probably see again and again.

Q: *NXP's CEO recently stated that mixed-signal semiconductor technology will be critical in solving future energy efficiency, healthcare, mobility and security challenges that impact society. With this increased need, does Fresco Microchip plan to implement its mixed-signal technology in other markets?*

A: The TV tuner space is a very large market, so we are going to be focused on it for awhile. However, having said that, the world is going to remain analog, and low-cost processing is going to remain digital. Our corporate DNA is about innovating at points where DSP can enhance analog processing. We continue to see these opportunities expand in a number of areas, and we are dedicated to bringing our expertise to those points of leverage to provide new value propositions. So, yes, in the future we will implement our mixed-signal technology in many different markets.

Q: *The landscape of the global TV market is rapidly changing due to the arrival of mobile TV, 3-D TV, etc. How is the company's commitment to providing enhanced picture quality impacted by the new ways of viewing content?*

A: As the number of TV tuners and other wireless applications explode due to the growing world of TV delivery, Fresco sees expanding opportunities for its radio frequency (RF) solutions. These opportunities include digital video recorders (DVRs), a brand new device in the living room which often have as many as six TV tuners; 3-D broadcast which requires two channels; white space communications; and more. The requirements for changing TV signals are also growing. The good news for Fresco is that our innovative technology can be applied to virtually every arena whether it is TV, FM, Wi-Fi, 60-gig, etc.

Q: *New research shows that the economic recession stirred an entrepreneurial spirit worldwide, resulting in the vast formation of start-ups. With the experience of five start-ups under your belt, what advice would you impart to start-up executives in terms of achieving market growth and gaining capital?*

A: To be successful in today's industry, I believe there are three qualities a start-up executive must possess. First, to get a start-up off the ground, they must exhibit perspicacity, which is the ability to see the opportunity and know how to take advantage of it. An effective executive will be able to define and communicate their value proposition. The second quality is alacrity. They must move quickly because no matter what the opportunity is and how significant their advantage is, it doesn't last forever. The ability to seize that opportunity with the funding raised is always time-limited. Tenacity is the third quality. They have to be relentless and never stop moving, slow down or become complacent. Getting the first customers over the finish line is the hardest thing to do until you have to get the next set of customers over the finish line. ■

Going forward, TSIA is committed to promoting the exchange of technological innovations across industries in Taiwan for the sustainable creation of value and wealth, not only locally but also globally. As expressed by Dr. T.Y. Wu, "TSIA is fully conscious of its charter and roles in serving the needs of its member companies and is dedicated to collaborate with every organization or institution whoever has a stake in creating new values for the global community as a whole." ■

About the Authors

Thomas Chen, director of Taiwan Semiconductor Manufacturing Company's (TSMC) technology system integration division, where he has served for over 20 years, holds an M.S. from National Tsing-Hua University, Taiwan and an executive MBA from National Taiwan University. Founding chair of TSIA's 300 mm automation working group, he was co-chair of the Institute of Electrical and Electronics Engineers (IEEE) Robotics and Automation Society Technical Committee on Semiconductor Manufacturing Automation, and served as a board member of the Society of Manufacturing Engineering, Taipei Chapter. Recipient of the Taiwan National Management Excellence Award, he has won numerous recognitions for his innovations and services. He can be reached at wychen@tsmc.com.

Robert Chien, deputy director at TSMC, holds an MBA from the School of Management, State University of New York at Buffalo. He was one of the key initiators of APC and fault detection (FDC) in TSMC. He concurrently supervises three computer integrated manufacturing (CIM) teams in one 200 mm fab and two 300 mm fabs: Fab6 and Fab14 in Tainan Science Park and Fab15 in Taichung Science Park, Taiwan. Prior to joining TSMC in 2000, he served for over 15 years at IBM as a sales manager of system integration service in the semiconductor and liquid crystal display (LCD) industries. He can be reached at robert_chien@tsmc.com.

Keung Hui joined TSMC in 2000 and is a technical manager in developing the core engine of control systems for APC. He received his Ph.D. in control engineering from the University of Hong Kong and has served the semiconductor public since 2003 with the IEEE International Conference on Robotics and Automation (ICRA) Workshop on 300 mm automation in Taipei. He is the program chair of the e-Manufacturing and AEC/APC-Asia Symposium in Taiwan. With over 30 publications, his interests are in modeling and the control of dynamic systems. A seasoned hand in facilities engineering and a chartered engineer in the U.K., he earned his Hong Kong Institution of Engineers corporate membership and other professional memberships after extended exposure in the building services industry. He can be reached at chsuo@tsmc.com.

EDA as it is in the entire semiconductor industry. However, I do not believe the acquisition of premature start-ups is the best strategy for the EDA sector's growth. Many EDA start-ups are positioned for an acquisition by a larger player before they have delivered sustainable value to the market and significant adoption of their technology has occurred. In these cases, when the prevailing exit strategy is solely to gain enough traction to be acquired, there may be a few winners, but there will be a lot more fire sales. Early exits often lead to infant mortality of critical innovations.

Jasper and my previous companies have had the staying power to drive substantial adoption of missionary solutions, making sure they have real world applicability and sustainable ROI. Once technology, customer adoption and scalability risks are eliminated, then only can a business with real value to investors, customers, employees and potential M&A candidates be built. This raises a company's valuation regardless of a choice of exit strategies.

Q: Many industry professionals have voiced the need for cooperation within the EDA industry to create an open ecosystem for the design community. With an increased group effort, what area do you feel the industry should be focusing on?

A: Jasper is very enthusiastic about unified standards, and we are active in organizations such as Accellera that promote standards for EDA, semiconductor and IP vendors. It's much more valuable for EDA suppliers to focus on tool innovation rather than support fragmented "same but different" standards, and our customers who want to use best-in-class tools from multiple vendors suffer too if interoperability is not ensured.

Q: Jasper Design Automation has openly advocated for the EDA

industry to leverage the advantages of parallel computing, an issue that has been highly debated by the community due to technical challenges. Explain the value parallel computing provides the industry.

A: By leveraging the advantages of parallel computing, expensive calendar time and engineering labor is exchanged for relatively inexpensive computer time, maximizing throughput. With a new-generation EDA platform, Jasper has a huge advantage and is leading in this area because our architecture is designed for scalability and parallelization. We view parallelization as a way to shrink schedules and user efforts, delivering inherent ROI for customers. For example, think of how much engineering productivity is unleashed when a verification run is slashed from 10 hours to just one hour!

Q: As a verification expert, what questions or complaints are you hearing from chip companies relating to IP reuse, and what issues are resulting? How can companies overcome these challenges and increase the value of their IP?

A: According to Ron Collett, president and CEO of Numerics, adding 10 percent of new circuitry to each block in a large design may actually double the total design effort. That's the main dilemma posed by IP reuse, and one that presents a tremendous opportunity for Jasper. We are delivering enabling technology to address IP comprehension, reuse, modification and collaborative coding as we believe the industry has focused a great amount of energy on packaging IP, but very little on solving basic challenges. It is naïve to think of IP as plug-and-play. It's not enough to verify protocols. The block must achieve true interoperability with the rest of the chip's logic. We're empowering designers with the knowledge they need to actually comprehend and integrate IP safely so the reuse paradigm can be leveraged to its maximum potential. ■

GSA 2011 EVENTS CALENDAR

Suppliers Forum & Networking Series

March 9, 2011 ■ London, UK

GSA Memory Conference

March 31, 2011 ■ San Jose, CA

ITAC & GSA Conference

April 13-14, 2011 ■ Montreal, Quebec

Silicon Series Luncheon

April 28, 2011 ■ Santa Clara, CA

Israel Executive Forum

May 3, 2011 ■ Tel Aviv, Israel

GSA & IET International Semiconductor Forum

May 11-12, 2011 ■ Munich, Germany

GSA Semiconductor Ecosystem Summit

October 6, 2011 ■ Santa Clara, CA

Silicon Series Luncheon

October 20, 2011 ■ Boston, MA

Silicon Series Luncheon

October 27, 2011 ■ Austin, TX

Awards Dinner Celebration

December 8, 2011 ■ Santa Clara, CA

