JP001 Questionnaire Results Summary

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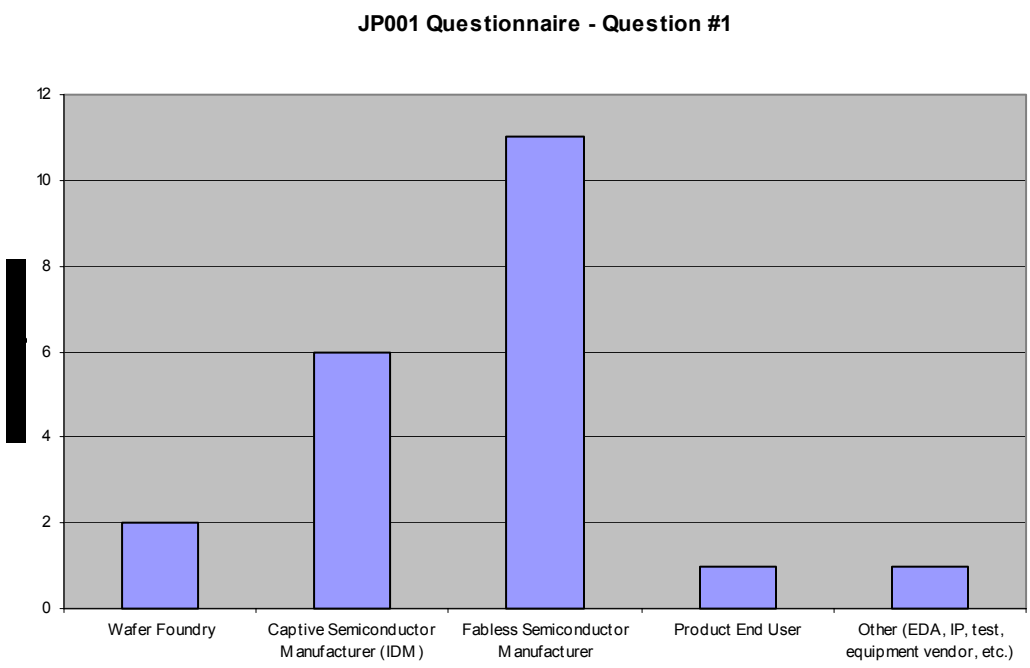
JP001 is a joint JEDEC/FSA document released in 2002 as a guideline on foundry process qualification. A questionnaire soliciting feedback on JP001 was sent out in June 2004 to members of the FSA and simultaneously to JEDEC JC-14 members. A total of 18 responses were received. Fourteen were from FSA members and four were from JC14 members. While a greater number had been hoped for, the sample provides meaningful statistical information. A summary of the response to questions #1-5 is given in Table #1.

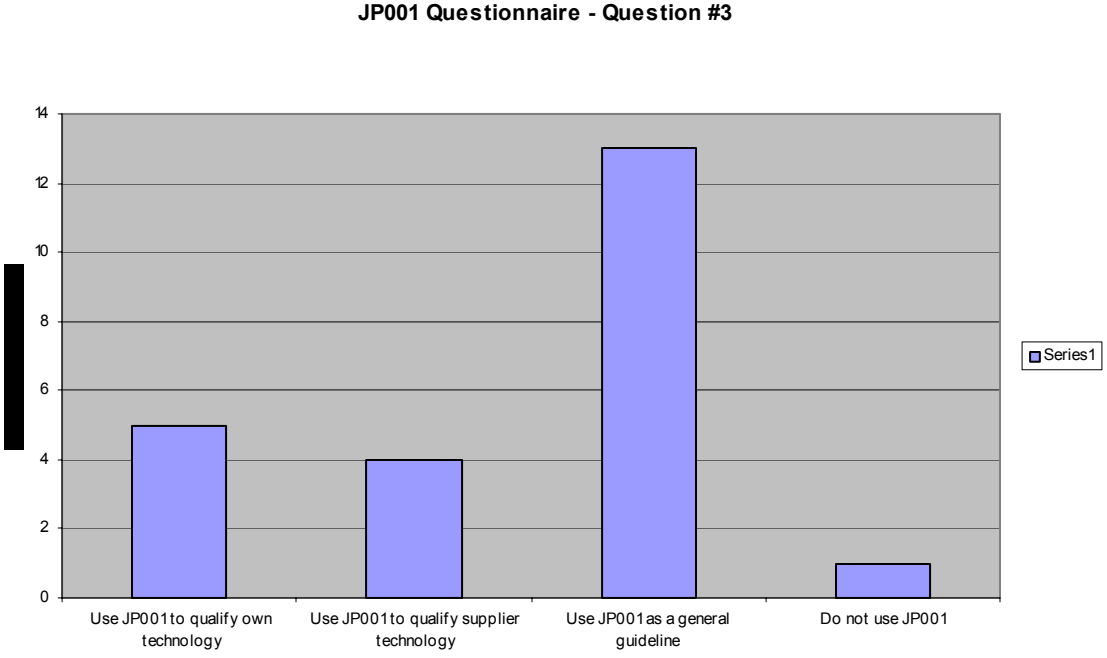
Table #1 – Summary of Responses

Question	Total number of respondents	18
1a	Wafer Foundry	2
1b	Captive Semiconductor Manufacturer (IDM)	6
1c	Fabless Semiconductor Manufacturer	11
1d	Product End User	1
1e	Other (EDA, IP, test, equipment vendor, etc.)	1
2a	Familiar with JP001	17
2b	Not familiar with JP002	1
3a	Use JP001 to qualify own technology	5
3b	Use JP001 to qualify supplier technology	4
3c	Use JP001 as a general guideline	13
3d	Do not use JP001	1
4a	JP001 covers 90-100% of our requirements	8
4b	JP001 covers 70-90% of our requirements	7
4c	JP001 covers less than 70% of our requirements	1
5a	JP001 overlaps 90-100% of our qualification spec	6
5b	JP001 overlaps 70-90% of our qualification spec	5
5c	JP001 overlaps less than 70% of our qualification spec	2
5d (N/A)	We do not have our own foundry qualification spec	3

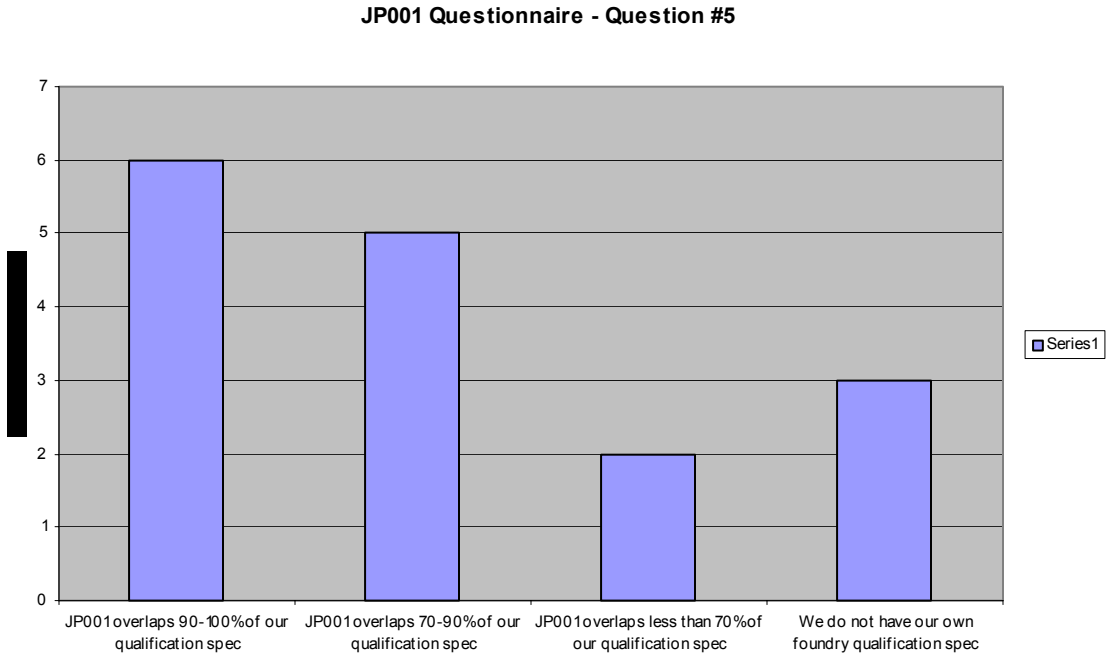
As seen in the chart for Question #1, the largest group of respondents was fabless semiconductor manufacturers (11). The number of foundry respondents (2) was disappointing, but understandable given their historic reluctance to disclose information outside of their customer base. The respondent from one major foundry (Chartered) was an active participant throughout the evolution of JP001.



The chart for question #3 shows that the majority (13) use JP001 as a general guideline. Of the 18 respondents, five also use it to qualify their own technology, and four use it to qualify supplier technology. This issue was a major point of contention during the approval process for JP001, as many were opposed to its adoption as a JEDEC standard, and preferred the less restrictive "JEDEC publication". The survey, as well as many anecdotal observations, demonstrates that the guideline enjoys wide use.



The chart for question #5 shows that JP001 covers most user requirements. Gaps are highlighted by several respondents, as will be seen in the responses to Question #6. This was anticipated, as rapid changes in technology and qualification methodology invariably outpaced the slow approval process for JP001, which is arrived at by consensus.



Responses to Question #6

What the respondents lacked in numbers, they made up for with input. A total of 42 separate suggestions were made. Of these, 17 were suggested additions, 12 were suggested modifications, 2 were corrections and 11 were general comments. Several inputs were related to characterization of the Cu/Low-k metallization and interlayer dielectric, as well MIM and POP capacitors for mixed signal and RF. Specific recommendations included TDDB for the ILD, extensive stress migration testing and leakage and maximum voltage limits. Areas not yet covered by JEDEC standards were noted, including P2ID. Several respondents called for a better tie-in of technology qualification tests to product yield and reliability, through enhanced PCM data and expanded evaluation of the TQV (technology qualification vehicle). There was a call for addition of qualification tests specific to mixed signal, RF, power and flash technologies. Finally, there was a call to rectify the obvious lack of pass/fail criteria in JP001. This was another issue that was the subject of much debate during the approval process for JP001. The complete list of suggestions is attached.

What Next

The results of this questionnaire provide some assurance that the approach adopted in putting together JP001 is on the right track. Obviously, much needs to be done to keep JP001 current and relevant to the needs of JEDEC and FSA members. The document will

need to be expanded to cover more adequately mixed signal, RF, memory and power technologies. Some of the work will need to be shouldered by JC-14.2 Other JC-14 subcommittees will undoubtedly need to contribute. Given that the primary response to the questionnaire came through FSA, it will be imperative to maintain and strengthen the SFPQ committee, although the scope of its work may need to redefined. A significant thrust of SFPQ effort has to be directed at foundries. In the end, the payoff is in their response to the concerns of FSA members highlighted by this questionnaire.

Responses to Question #6

Suggested additions

1) Best practices/ expectations for Cu/Low-K BEOL including chip-package interactions
2) It would be nice to draft documents generated (sic) for those documents that do not have JEDEC references in place yet such as P2ID
3) Section 12.2, Early life test (pp29-31). Since a constant failure rate is not a very good assumption for the early life period, I would suggest adding the calculation methodology using the Weibull distribution, which can provide a more accurate measure of early life failure rate (assuming the Weibull beta is known). JESD 74 does not treat using the Weibull in much detail, and an explanation of the correct way to use this calculation method would be useful.
4) PCM and reliability data for interlayer caps (MIM, POP, …) used in RF & mixed signal design should include: Maximum voltage ratings and leakage characteristics. - Copper stress voids (stress migration) and low-k dielectric breakdown voltage
5) Generally, reporting requirements should include appropriate signoff, archiving, and revision control of final qualification report and supporting documents as performed by the company for meeting other corporate documentation requirements, I.e. QS9000, ISO900X, etc.
6) Best practices/ expectations for ultra-thin gate dielectric
7) I would suggest addition of a section for TDDB testing of interlayer dielectric when low-k dielectric is used. Although this may be burdensome on foundries, I believe it is very important to have an estimate of the voltage acceleration parameter, gamma, for ILD which can be used in determining the voltage acceleration factor (AFV) for HTOL testing.
8) PCM and reliability data on poly and thin film resistors used in RF & mixed signal design should include: Maximum current ratings including self-heating and aging effects.
9) Product Hot Carrier (I.e. degradation of Fmax of a microprocessor)
10) 10.3.2 P2ID- Addition for guideline of design rule for antenna ratios relative to ratio resulting in 0.1% failures. Guidelines for appropriate range of structures would be beneficial.
11) MOS and biploar transistor operating life tests should include dynamic supply effects. In RF & mixed signal design transistors are sometimes put under stress where voltage dynamically exceeds Vcc. One example being power amplifier design with inductive loads. Aging and breakdown characteristics are not tested under these conditions.

12) Add requirements specific to mixed signal, RF and fllash qualifications. Emphasize adequate test structures, test methodology, lifetime model.
13) Recommend addition of TDDB for deposited MIM dielectrics (I.e. Si34 is commonly used for linear MIM capacitors). Requirement for defect density and lifetime extraction [i.e. exp(-E)] T0.1%.
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17) Section 12 has proven to be insufficient to demonstrate expected yields. There is no requirement to identify edge related yield fallout, or specify edge exclusion in analysis. Wafer level probe should be utilized early in the qualification process with the TQV to work out and prove manufacturability. Packaging and characterization of edge die is crucial to prove performance to specified edge exclusion zone.

Suggested modifications

1) Page ii, acronyms: Suggest list be alphabetized, and add: FA (failure analysis), TC (temperature cycling)
2) It would be helpful to have a table showing the statistical meaning of the results obtained as a result of the sample size criteria outlined in section 4
3) Page 2, section 5: Suggest use TC instead of TCT to remain consistent throughout
4) Revise temperature-bias instability with potential addition of NBTI
5) Page 3-4: Suggest update standards, for example JEDEC JEP1122 is 122B, and JESD47 is now 47B
6) 8.1 Electromigration
7) 8.2 Stress Migration
8) Page 12 section 8.4 Inter/intra-metal dielectric reliability
9) Section 10.2 TDDB
10) Section 10.3 Plasma damage
11) Page 25-26 Section 11.3 NBTI
12) Page 27 section 12.1.1

Suggested corrections

1) 6.1.5 Endurance Tests: Document # is JEDEC JESD50 (not 51)
2) Section 12.4.1, THB/HAST test requirements, page 33. Under "Test Conditions" the temperature for HAST is listed as 131C. JESD22-A110 lists this temperature as 130C. I believe this should be changed so as to be consistent with the JEDEC spec.

Comments

1) An outlook of TQV best practices for 65nm and 45nm nodes would be useful - SRAM size and cell count - and options for other vehicles
2) We have discovered that meeting the guidelines set forth in JP001 does not necessarily ensure reliable operation of our product and IP blocks. This is even true when moving between fabs within the same company. Adding process qual quidelines for NVM and in particular logic NVM would be particularly useful.
3) Very good document and we hope that foundries follow these guidelines
4) I believe that the spec is good in that it summarizes the test methods and requirements from a number of different JEDEC and other documents. Perhaps as the specification gets more widespread acceptance, we will start seeing in the foundry qualification reports more of the information specified here.
3) JP001 outlines reliability tests that should be made, suggests sample sizes to be used and provides instructions on how the tests are to be run. It does not, however, provide any suggested specifications as to what the results should be for each of the tests. So a silicon vendor could complete all of the specified tests using the specified techniques and declare the process "qualified" regardless of the results! Any plans to "suggest" what the results should be by technology node?
4) This is a very thorough set of guidelines. We haven't had the opportunity yet to use the detail in this document as a guide in qualifying a new fab.
5) We have our own internal qualification policy which has a flvor of JEDEC specs but not fully compatible
6) Alphamosaic use JP001 as a guideline to assess 3rd party foundry process qualification. We are not process experts and as such rely on standards and the expertise of our foundry partners. We are not really qualified to comment on the content and quality of standards like JP001.
7) (very important) Site location information relarive to edge exclusion needs to be specified for all tests listed in this document. PCM data with 35mm edge exclusion with product picked at 3mm edge exclusion leaves a large unknown gap. It should be considered by JC14.2 on how to fill this gap.
8) In general, we find JP001 to be a useful benchmark for a core set of qualification activities, and would like to see it extended to cover the areas soecifically excluded in the forward of the first edition - ultra thin oxide and Cu/Low-K
9) One section of the spec where I don't see as much data from foundries as the spec suggests is section 8.2-stress migration. Five temperatures may be considered too burdensome by foundries. However, testing to at least 2000 hours is important. The literatire suggests that such testing is necessary in order to determine if the silicon technology is free of the failure mechanism for the useful life of the product
10) Generally, foundries are using much of that specified in JP001. A querry of Tier-1 foundry indicated that they conform with JP001. More detailed requirements as listed in above requests for additions would have eliminated complications due to new process introductions.
11) Another area which does not seem to get as much attention as it probably should is P2ID testing (section 10.3)

List of Respondents

AMD –Mike Van Hoy
Agilent – Dennis Eaton
Agere Systems – Carl Peridier
Aeroflex - Steven Netherton
Alphamosaic - Keith Walker
Chartered Semiconductor - Andrew Yap
EMC Corporation - Michael Sosnowski
IBM Microelectronics - Thomas Sandwick
Impinj - Ron Paulsen
Intersil - Mike Dion
Macronix - Albert Kuo
Magnolia Broadband - William Reinisch
Mellanox - Shmuel Maharshak
Mentor Graphics - Bruce Brunken
Polar Fab - Walter Jopke
Skyworks - Richard Burton
Spirea AB - Peter Olofsson
T-RAM – Frank Ruttenberg