UNDERSTANDING THE SEMICONDUCTOR INTELLECTUAL PROPERTY (SIP) BUSINESS PROCESS

Finding, Evaluating and Licensing Commercial SIP

Vin Ratford, Nick Popper, Dan Caldwell and Tom Katsioulas
Industry Baseline Working Group (IBWG)
June 2003

SIP INDUSTRY OVERVIEW

- Semiconductor Intellectual Property is essential for IC design
- SIP value will continue to grow with increasing complexity
- SIP product market is projected to grow to $1.5B by 2007*
- However, the SIP business infrastructure is still maturing
- The FSA IP Committee is focusing on a variety of SIP issues
- The IBWG promotes a consistent baseline for the SIP business

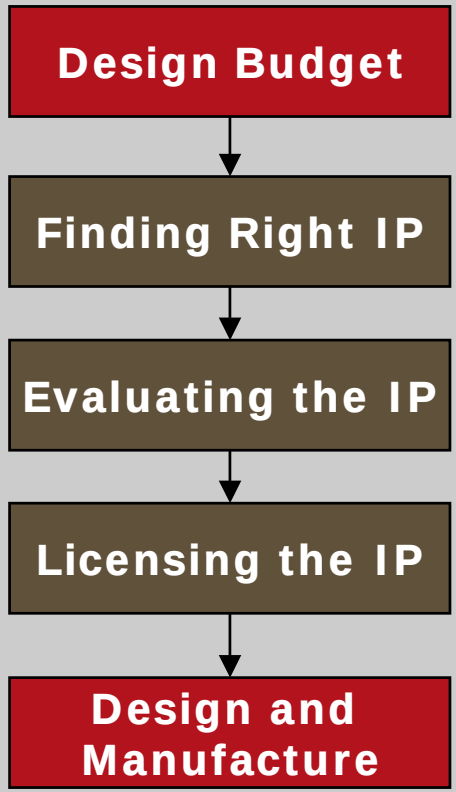
Source: In-Stat/MDR, April 2003

SIP BUSINESS ENVIRONMENT

- The SIP business is more complex than EDA and IC business
  - Business practices include elements of IC, EDA, and services
  - Several parties are involved in the SIP supply chain to build ICs
  - SIP Buyers purchase multiple SIP types from several sources
- One key barrier to standardizing the SIP business is SIP variability
  - SIP Value: Functionality, reusability, availability, spec, form, type
  - SIP Form: Soft versus Hard IP cost/performance characteristics
  - SIP Type: Library, Memory, Processor, Analog, and Connectivity
- Distribution channel diversity also contributes to complexity
  - SIP providers: Web downloads, direct sales, NRE, and services
  - Foundries: Direct or indirect distribution and 3rd party support
  - EDA Vendors: Proprietary or foundry SIP, and design services

SOURCING SIP PRODUCTS

- Criteria: decision to “make vs. buy” SIP
- Factors: Availability, Spec, Type and Cost
- Sources: SIP Providers, EDA, Foundries, etc.
- Business models: value, cost, risk, payments
- Quality: maintenance relative to specification
- Mobility: portability and second sourcing
- Licensing: scope, terms and conditions



BASELINE TERMINOLOGY

- SIP Product
  - Set of design files, models, test benches, that make up the offering
  - A “Virtual Good” licensed by a SIP Provider to one or more SIP Buyers
  - Commercial SIP has a functional spec and well defined characteristics

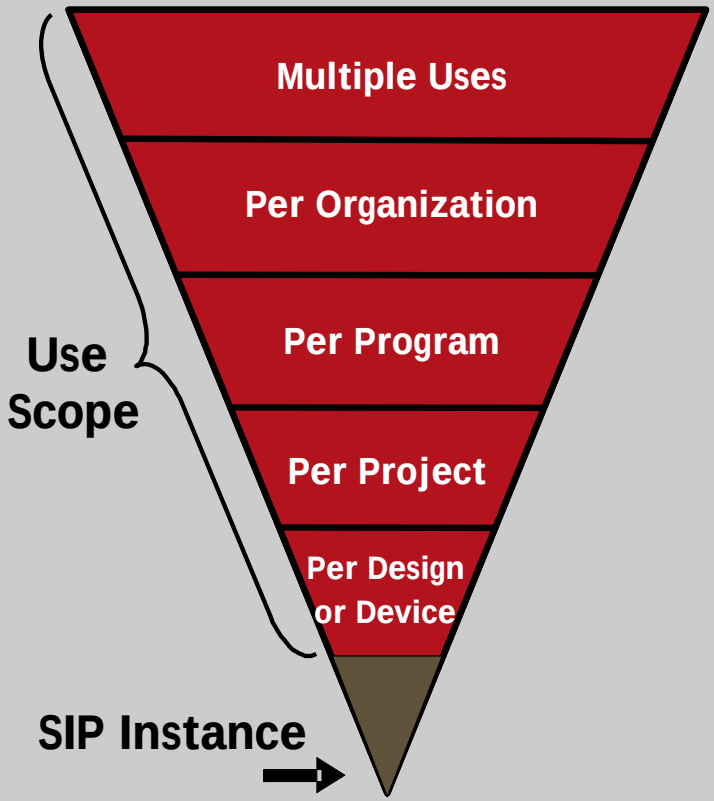
- SIP Purchase
  - Transfer of limited IPR* in an SIP from a Provider to a Buyer
  - There is normally no wholesale transfer of ownership of SIP rights
  - Unlike “Real Goods” the Provider maintains ownership of the SIP

- SIP License Agreement
  - A contract that defines the terms of the SIP Purchase
  - Typically includes right to manufacture products using SIP
  - It may also limit the use of SIP to a pre defined field

Intellectual Property Rights

BASELINE TERMINOLOGY (CONT'D)

- SIP Rights
  - Scope of permissible SIP uses which may vary based on several business parameters
  - Use, Copy, Modify, Distribute, Sub-license
- SIP Instance
  - A specific configuration of the SIP used one or more times based on Use Scope
- SIP Use Scope
  - A defined field of use with a set of restrictions based on business model
- SIP Tracking
  - Measures used by SIP Providers to identify and monitor usage of their products



BASELINE TERMINOLOGY (CONT'D)

SIP Use Scope

Per Design	An IC intended to be manufactured and distributed commercially
Per Project	One or multiple chip designs for a single application segment
Per Program	One or multiple projects for a variety of application segments
Per Organization	One or more geographies (incl. corporate-wide) and/or programs
Multiple Uses	Many uses over a period of time for given process technologies

FINDING SIP AND RELATED PRODUCTS

- FSA Listing: https://www.fsa.org/directories/suppliers/index.htm

- Direct Sources (see Appendix)
  - SIP and infrastructure Providers
  - Semiconductor foundries
  - EDA Tool and Service Providers
  - Broad line IC suppliers

- Internet Catalog Listings
  - Virtual Component Exchange (VCX) www.thevcx.com
  - Design and Reuse (DNR) www.design-reuse.com
  - Open Cores (open source IP) www.opencores.org

- Industry Consortia
  - Virtual Socket Interface Alliance (VSIA) www.vsi.org
  - Silicon Integration Initiative (Si2) www.Si2.org
  - Rosetta Net Consortium http://www.rosettanet.org/
  - FSA IP sub-committees initiatives www.fsa.org/committees/ip

EVALUATING SIP BUSINESS MODELS

- Business Issues
  - SIP Buyers cope with multiple Providers and business models
  - SIP business infrastructure is viewed as confusing and inconsistent
  - It takes significant effort to determine the economic value of SIP
- IBWG Goal
  - Develop a baseline for objectively comparing business models
- Objectives
  - Define business models and enabling components for SIP
  - Establish a taxonomy to facilitate SIP purchasing transactions
  - Provide examples on SIP commercial products by type

TYPICAL SIP BUSINESS MODELS

Typical SIP Business Models

	Per Use	Time Based	Royalty Based	Access
Purpose	Fee for each SIP on defined use scope	Multiple uses of SIP over a period of time	Amortize cost of SIP Share Risk-Reward	Fee for SIP portfolio over a period of time
Payments	Event Based	Time Based	Value Based	Subscription Based
Structure	One time fee for a design (first or subsequent)	Fee for all designs within a given time	Some or all fees spread across units	Up Front Fee plus discounted use fee
Scope	Per Design Per Device	Multiple Uses Per Device	% of Unit Value Per Device	Multiple SIPs Per Organization

Sources: SIP Business Overview - Dan Caldwell - Virage Logic; SIP Market – Gartner Inc.; Selected SIP vendors

TYPICAL SIP ENABLING COMPONENTS

Typical SIP Enablers

	Maintenance	Support	NRE	Contract Service
Purpose	SIP updates, bug fixes, and revisions	Address specific customer needs	Enable SIP use	Enable IC design
Payments	% List Price License Fee	Scope Based	Milestone Based	Hourly Based
Structure	Part of Initial License Agreement (May be included)	Basic Package or, Separate Contract	Initial Fee % Milestones	Initial Fee (SOW) % Milestones
Scope	Changes in spec, process tech, etc.	Web, Email, Tel, On-Site, Geography	Modifications, re-spins, porting, etc.	Tool runs, IC Integ, EDA Views, etc.

Sources: SIP Business Overview - Dan Caldwell - Virage Logic; SIP Market – Gartner Inc.; Selected SIP vendors

PER USE MODEL

- Definition/Purpose
  - Fee paid for each SIP licensed within a defined scope of use
  - Usually applicable for a specific SIP and/or SIP configuration

- Payments: Event Based
  - Initial fee for 1st use paid upon execution of the license agreement
    - Portion of license fee may be paid on event basis (i.e. tape-out)
  - Reuse fee paid for a new scope (optional, subsequent to initial use)
  - Other fees may be paid for derived uses (optional, may also be NRE)
    - Re-spins, Derivatives, Variations, New Configurations

- Scope of Use
  - Typically Per Design, Per Project and Per Device

TIME BASED MODEL

- Definition/Purpose
  - Fee paid for a SIP and/or SIP configuration over a period of time
  - Unlike EDA user licenses the right to manufacture with the SIP

- Payments: Time Based
  - Initial fee paid upon execution of the license (may be perpetual)
  - Renewal fee paid when the explicit or implicit* time period expires
  - May include an EDA Time-Based License for companion software
    - Generator Software: Memory and PLL Compilers, Programmable Cores
    - Embedded Software: Application Layers, Device Drivers, Stacks, RTOS

- Scope of Use
  - Multiple uses for specific process technology (Per Device)

*End of life of the specific process technology

ROYALTY BASED MODEL

- Definition/Purpose
  - Fee paid for a SIP amortized over the life time of the end-product
  - SIP Provider and SIP Buyer share the risk-reward of failure-success
- Payments: Value Based
  - Initial fee paid upon execution of the license (may be small, or waived)
  - Subsequent fees per unit (royalties) are based on measurable criteria
  - SIP Providers ask for audit provisions to conform with SEC regulation
- Scope of Use
  - Per IC unit (% of cost, or % of ASP, or Fixed Fee)
  - Per Wafer (% of cost, or % of ASP, or % of used die area)
  - Value Based (% improvement in die size, performance, or yield)

ACCESS MODEL

- Definition/Purpose
  - Fee paid to access a SIP portfolio over a period of time
  - SIP Buyer may use any of the SIP without specifying up front
- Payments: Subscription Based
  - Access (or subscription) fee enables to design with any of the SIP
    - May be a one-time flat fee which includes any specific SIP use
  - Optional discounted fee for each specific SIP use paid upon event
    - Tape-out, Wafer In, Production, etc.
- Scope of Use
  - Typically multiple uses of multiple SIPs per organization

MAINTENANCE

- Definition/Purpose
  - Fees paid to cover the cost of updates, bug fixes, revisions, etc.
  - SIP Provider defines what is covered (or not) based on SIP spec

- Payments: Vary by Business Model
  - Typically 12-18% of the license fee paid over a period of time
  - Usually not discounted and accounted separately from the license
  - Time period may be different than the term of the SIP license

- Scope/Examples
  - Changes in the Spec: which updates covered; corner cases; test bench
  - Process Technology: which and how many updates; foundry mobility
  - Connectivity Standards: which revision; which future changes supported
  - EDA Tools & Formats: which tools models; how often they get updated
  - End Product Integration: SIP performance in the IC; services offered

SUPPORT

- Definition/Purpose
  - Fees paid for technical support relative to SIP Buyer's needs
  - Parties define what is covered (or not) as part of support package
    - Often structured as a separate agreement based on scope of use
- Payments: Scope Based
  - Pre-defined fees for basic support package of a specific scope
  - Some SIP Providers may be include it as part of maintenance
  - Custom programs extend support based on needs and resources
- Scope/Examples
  - Basic Support: Email, Web, Telephone, occasional on-site AE
  - Resources needed: # of engineers, concurrent projects, geographies
  - Expertise needed: Training, R&D, modifications, end-application

NRE CHARGES

- Definition/Purpose
  - Fees paid to enable the use of the SIP (work is central to the SIP)
  - Providers seek the right to own the SIP and typically recover fees
  - The SIP developed may result into some sort of shared rights

- Payment: Milestone Based
  - Initial fee paid upon execution of the agreement based on SOW*
  - Subsequent fees paid on a milestone and/or event basis

- Scope/Examples
  - SIP modifications, custom configurations, re-spins
  - Porting SIP to new foundry for the same process node
  - SIP development for a new process node, or revision of a standard
  - Integration of multiple SIPs into a new SIP configuration

*SOW: Statement of Work outlining nature of work, cost, and timeframe of delivery

CONTRACT SERVICES

- Definition/Purpose
  - Fees paid to enable an IC design using SIP (work is peripheral to SIP)
  - Fees are for engineering hire; usually customer owns deliverables
    - Shared rights may occur but are not typical (work is not central to SIP)

- Payment: Milestone or Hourly Based
  - Initial fee paid upon acceptance of the statement of work (SOW)
  - Subsequent fees paid based on completion upon invoice

- Scope/Examples
  - EDA design flow services (Synthesis, Analysis, Place+Route, etc.)
  - Custom design views (Timing Models, Physical Models, etc.)
  - IC integration services (Assembly, Full Chip Verification, etc.)

EXAMPLES: DIGITAL SIP

Digital SIP	Per Use	Time Based	Royalty Based
IP & Deliverables	Soft Silicon Proven DSP Netlist, Test Bench, etc.	Firm Silicon Proven PCI EDA Views + Test Bench	Protocol Processor EDA, GDSII, Firmware
Initial Fee - Scope	Fee for first IC in 0.18u TSMC, UMC, or CSM	Up-front fee for 3-years Multiple use in UMC L130	Fee due on GDSII delivery Any IC in TSMC 0.13u
Event Fees	Fee due on execution of SIP License Agreement	Fee due on execution of SIP License Agreement	Quarterly payments made after first shipment
(Re) Use Fees	% Reuse Fee up to 3 ICs	Renewal upon expiration	Royalty per chip (% ASP) based on performance
Maintenance	15% covers bug fixes and minor spec updates	15% covers bug fixes and updates for Rev 2.1 only	15% covers firmware and up to 2 process updates
Support	Incl: Email, Tel, on site AE	Incl: Email, Tel, on site AE Separate On-site R&D	Separate custom package
NRE	Functional Modifications	Revisions beyond 2.1	Port to a New Foundry
Contract Services	System Level Verification	Back-end implementation	Full Chip Verification

EXAMPLES: MEMORY SIP

Memory SIP	Per Use (Instance)	Time Based	Royalty Based
IP & Deliverables	Dual-port SRAM 2Kx16 Col Mux 4 EDA Views, BitCell*	SRAM Compiler, EDA Views, and BitCell GDSII*	Custom High Speed SRAM EDA Views, BitCell GDSII
Intial Fee - Scope	Fee upon delivery Multi-uses in TSMC* 0.18u	Up-front fee for multiple uses in CSM* 0.18u	% Fee upon SOW Per Design UMC L130
Event Fees		Annual TBL for Compiler	% Fee upon tape-out
(Re) Use Fees	% of License Fee to reuse on another foundry	Renewal upon expiration or for a new foundry port	% of chip Cost based on acceptance criteria
Maintenance	Optional - 15% per annum	15% covers compiler, EDA, bitcell, process updates	12% covers bug fixes and up to 3 process updates
Support	Incl: Email, Phone AE	Incl: up to three chips	Custom Package
NRE	Characterizations and Modifications if needed	Re-Characterization	Custom Development
Contract Services		Custom EDA Views	IC integration + Testing

* Foundry provided bitcell in GDSII

EXAMPLES: MEMORY SIP (CONT'D)

Memory SIP	Per Use - (Project)	Royalty Based	Access
IP & Deliverables	All SRAMs needed for a particular mask set	Self Testable, Repairable, SRAM Platform System	All Memory Compilers and complete Bitcell portfolio
Initial Fee - Scope	License fee upon delivery for a specific mask set	Up front License Fee plus Royalties Per Unit	Up-front fee for 3 years in TSMC and CSM 0.18u
Event Fees			% Fee Per Design due upon tape-out
(Re) Use Fees	% of License Fee to reuse on another mask set	% per unit sold, or per die based on savings (repair)	Renewal upon expiration
Maintenance	Optional 15% per annum	15% covers bug fixes and process updates	Included
Support	Incl: Email, Tel, on site AE	Incl: Email, Tel, on site AE	Incl: Email, Tel, on site AE
NRE	Characterizations and Modifications if needed	Characterizations and Modifications if needed	Re-characterization
Contract Services		Test + Repair Integration Yield Enhancement	Custom Fit Sizes

* Foundry provided bit cell (implicit time base)

EXAMPLES: LIBRARY SIP

Library SIP	Per Use	Royalty (3rd Party)	Access (+Per Use)
IP & Deliverables	High speed Std Cell Lib and I/O package	Std Cell Lib, I/O*, Bitcell*, & RAM compiler package	Complete Cell, I/O, SRAM Compiler, and bitcell* pack
Initial Fee - Scope	First chip in L130	Free for TSMC 0.18u (Paid by Foundry)	Annual Access Fee for use in UMC L180, L130
Event Fees	Tape-out Fee (Paid by End-User)		Per Design Tape-out Fee (Paid by Fabless ASIC Co)
(Re) Use Fees	% of Initial fee for each new chip up to 3 uses	Royalty per Wafer (Paid by foundry; Audit Right)	
Maintenance	12% covers up to 2 process updates	Free; Covers up to 4 process updates	Included; Covers process updates beyond time
Support	Paid Separately	Applications support package paid separately	Custom Premium Package
NRE Charges	Custom I/O Cells	New Custom Cells	I/O Modifications
Contract Services		Special Characterization	

* Foundry specific Foundation SIP

EXAMPLES: ANALOG SIP

Analog SIP	Per Use	Time Based	Royalty Based
IP & Deliverables*	50-250 MHz PLLs (Multiple SIPs Per Config)	Dual 6-bit and 10-bit Low voltage DACs	Custom 10-bit 400Mhz DAC Optimized for Video
Initial Fee - Scope	First chip for CSM 0.18u	Perpetual for multiple uses in UMC L180	% upon execution Any chip in UMC L130
Event Fees	% upon Tape-out		% upon SIP acceptance % upon tape-out
(Re) Use Fees	New chip in CSM 0.18u (Alternate SIP Config)	Renewal upon expiration	Fixed Fee per chip within 30 days of quarter sold
Maintenance	Included for first year 2 process changes max	15% paid annually covers only bug fixes	18% covers process changes beyond term
Support	Incl: Email, Tel, On-site AE	Incl: Email, Tel, On-site AE	Separate for on-site Eng
NRE Charges	Port to new foundry (New SIP License)	Re-characterization	% upon GDSII delivery
Contract Services		Custom size modifications	Platform Integration

*All deliverables are in GDSII

LICENSING SIP PRODUCTS

- Business Issues
  - Multiple SIP sources with a wide variety of licensing agreements
  - Inconsistent policies, licensing scope, provisions, terms, conditions
  - It usually take a significant effort to negotiate key business issues

- IBWG Goal
  - Develop a terminology and taxonomy to facilitate SIP licensing

- Objectives
  - Establish a baseline of typical provisions found in SIP agreements
  - Provide a taxonomy of contract provisions, and related options
  - Examine and analyze SIP Provider and SIP Buyer perspectives

SIP LICENSING PROVISIONS

Contract Provision	Description	Where	Req/Opt - Effort
Definitions	Type of agreement; Parties involved; SIP specifics; Llicense grant rights	MLA	R
Scope of License	Where and how the SIP can be used *Use, Copy, Modify, Distribute, Sub-license*	MLA App	R
Restrictions-Rights	"Forbidden uses" of the SIP Product; Disclaimer on third party Licenses	MLA	O
Deliverables	Items are delivered; Media of delivery; Terms an conditions	MLA App	R
Acceptance	Conditions under which a non Silicon Proven SIP Product is accepted	App	O
Payments	Fee structure; Payment terms; Method; Currency & taxes;Rights/Terms of audit	App	R
Special Conditions	Requests related to SOW, SIP Mobility, SIP Performance, Sales & Marketing	App	O

Sources: VCX Model agreement; Keith Witek - AMD; Carl Hoxeng - Virage; SIP provider agreements

Legend: R: Required; O:Optional; MLA: Usually in Master License Agreement; App: Usually in Appendix

SIP LICENSING PROVISIONS (CONT'D)

Contract Provision	Description	Where	Req / Opt - Effort
Warranty	How long is the coverage; What to do if SIP does not work; What voids warranty	MLA	R
Indemnification	IPR covered; Remedies and obligations if a third party alleges SIP infringement	MLA	O
Limitation of Liability	What happens if use of an SIP causes harm to the Buyer; Formula for limitation	MLA	O
Maintenance	What is covered or not; Which process-tool updates; What if the spec changes	MLA	R
Support	What is included or not; Other contract for support based on Buyer's needs	Other	O
Term and Termination	How long the agreement lasts; What are the conditions for early termination	MLA	R
Confidentiality	What is confidential; How it's being treated; How to keep it that way	MLA	O
General Provisions	Governing law, assignment, export requirements, integration/modification	MLA	R

Sources: VCX Model agreement; Keith Witek - AMD; Carl Hoxeng - Virage; SIP provider agreements

Legend: R: Required; O:Optional; MLA: Usually in Master License Agreement; App: Usually in Appendix

SIP LICENSING PROVISIONS

- Definitions
  - Type of agreement being formed and effective dates
  - Parties involved: Licensor, Licensee, and 3rd parties
  - SIP specifics: Product, Technology, Data, Views, etc.

- Scope of License
  - Permitted uses of the SIP
    - Use (i.e. Multiple Uses, Geography, Program, Project, Design, Device)
    - Copy and Restrictions (i.e. how many copies allowed and restrictions)
    - Modify (i.e. no netlist changes allowed in Soft SIP except cell resizing)
    - Distribute (i.e. Fabless ASIC vendor may have a right to distribute)
    - Sublicense (i.e. OEM and reseller or distribution agreements)

SIP LICENSING PROVISIONS

- Modification rights and ownership
  - Does the Buyer have the rights to modify?
  - If so who has the ownership of modifications?
- Sublicense rights
  - Allocation of ownership on jointly created SIP Products
  - May be needed if SIP Product is formed by multiple SIPs
- Restrictions on Scope
  - “Forbidden uses” of SIP Product (i.e. no special layer change)
  - Disclaimer of implied licenses (i.e. all rights under the agreement)
  - Third party licenses (i.e. I^2C from Philips requires another license)

SIP LICENSING PROVISIONS

- Deliverables
  - Items to be delivered, media of delivery, terms, and conditions
- Acceptance
  - Conditions that constitute acceptance for non silicon proven SIP
  - For silicon proven SIP acceptance occurs upon “delivery” of items
- Payments
  - Fee Structure (as defined in business models)
  - Currency; Exchange risk and permits
  - Payment Terms and Method of payment
  - Taxes (withholding on foreign countries)
  - Royalties; Under/Overpayment; Rights and Terms of Audit;
  - Other fees (brokerage, joint SIP owners, etc.)

SIP LICENSING PROVISIONS

- Special Conditions (Examples)
  - SOW Related: progress updates, intermediate milestones, etc.
  - Special SIP Requirements: corner cases, silicon performance, etc.
  - Sales & Marketing: Provider asks for reference or marketing P.R.
  - SIP Mobility: Buyer asks for alternatives during limited fab capacity

- Warranty
  - Basis of warranty (typically a spec provided by SIP Provider)
  - Warranty period (how long does it last; how long to notify licensor)
  - Notification of non-compliance (licensee identifies issues with IP)
  - Licensor's obligations on non-compliance (i.e. fix, or replace)
  - Actions and inactions that void warranty (i.e. modifications)
  - International warranty (may be mandatory in certain jurisdictions)

SIP LICENSING PROVISIONS

- Indemnification
  - IPRs* covered (copyrights, trade secrets, patents, etc.)
  - Applicable geography (Typically only industrialized countries)
  - Provider's obligations (modify, replace, compromise, settle, etc.)
  - Buyer's obligations (notice, cooperate, don't settle, etc.)
  - Conduct that renders indemnity null and void

- Limitation of Liability
  - Formula for calculating limitation (license fee multiple with a floor)
  - Exclusions (conduct that renders Limitation of Liability null and void)
  - "Reverse Indemnities" (conduct that may result liability to 3rd party)

- Indemnity Gap
  - Gap between what SIP Providers offer and what Buyers expect

*Intellectual Property Rights

SIP LICENSING PROVISIONS

- Maintenance and Support
  - Maintenance coverage level with special language for accounting
  - Separate support contract usually referenced in the agreement
- Term and Termination
  - How long agreement lasts; conditions for early termination
  - What happens after the agreement ends (post termination rights)
- Confidentiality
- General Provisions
  - Governing law and jurisdiction (local compliance requirements)
  - Assignment (protecting SIP from time of creation and beyond)
  - Export requirements: (Commerce, State/DOD, Treasury)
  - Entire Agreement clause for integration and written modification

PROVIDER AND BUYER PERSPECTIVES

	Provider Perspective	Buyer Perspective
License Grant	Narrow Scope of Use	Broad + Flexible Scope
Restrictions	Limit Geographies, Copies, etc.	Few or No Restrictions
Deliverables	Set of Items; Accept on Delivery Narrow Maintenance Coverage	More Items; Accept On Criteria; Broad Maintenance Coverage
Warranty	As Is; Applies to SIP only Above and beyond is NRE	No Limitation; Applies to SIP and IC
Remedy - Cure	Fix, Replace - Weeks	Fix, Replace, Refund - Days
Period - Parties	30-90 days Licensee Only	3-5 years Licensee + Related Parties

PROVIDER AND BUYER PERSPECTIVES

	Provider Perspective	Buyer Perspective
Indemnity	Copyrights + Trade Secrets Indemnify Only	No Limitation on Any SIP Defend, Indemnify, Hold Harmless
Geography	Limited the US, EC, and Asia	Worldwide Without Restriction
Remedies	License to Use, Design Around, Refund, Termination	No Restrictions, Some Remedies
Liability	Based on Transaction Value	Based on Business Risk
Damages	Limited to license price, or Multiple With a Cap	No Caps or Restrictions
Exclusions	Improper Use; Modifications	Flexibility Trade-offs

ACKNOWLEDGEMENTS

IBWG: SIP Providers, Foundries, EDA Vendors and SIP Customers

- Vin Ratford, Xilinx — vincent.ratford@xilinx.com
- Nick Popper, Consultant, Software & IP Licensing — nick.popper@gmail.com
- Dan Caldwell, Semiconductor IP Business Consulting — dan_caldwell@yahoo.com
- Keith Witek, AMD — keith.witek@amd.com
- Steve Kompolt, Real Intelligence — steve@realintelligence.com
- Tom Katsioulas, 3Plus1 Technology — tomkat@sprintmail.com
- Jim Ensell, Virage Logic — jim.ensell@viragelogic.com
- John Ford
- Carl Hoxeng

Feedback, comments and suggestions to: ipeducation@fsa.org

Current List of Participating FSA Members

SIP Products and Infrastructure	
ARM	http://www.arm.com
Artisan Components	http://www.artisan.com
Synchronicity Inc.	http://www.synchronicity.com
Virage Logic	http://www.viragelogic.com
Virtual Component Exchange	http://www.thevcx.com
Virtual Silicon Technology	http://www.virtual-silicon.com

Semiconductor Foundries	
1st Silicon	http://www.1stsilicon.com
Chartered Semiconductor	http://www.charteredsemi.com
Hynix Semiconductor	http://www.hynix.com
Tower Semiconductor	http://www.towersemi.com
TSMC	http://www.tsmc.com
UMC	http://www.umc.com

APPENDIX (CONT'D)

List of Participating FSA Members

EDA Tools and Services	
Barcelona Design Inc.	http://www.barcelonadesign.com
Cadence Design Systems	http://www.cadence.com
Mentor Graphics Corporation	http://www.mentor.com
Monterey Design Systems	http://www.montereydesign.com
Reshape	http://www.reshape.com
Sagantec Corporation	http://www.sagantec.com
Sequence Design Inc.	http://www.sequencedesign.com
Synopsys, Inc.	http://www.synopsys.com

Broadline Semiconductor Suppliers	
Fujitsu Microelectronics	http://www.fujitsumicro.com
IBM Microelectronics	http://www.ibm.com/chips/
LSI Logic	http://www.lsilogic.com
Motorola Inc.	http://e-www.motorola.com
NEC Electronics	http://www.necel.com
Philips Semiconductor	http://www.semiconductors.philips.com
Samsung Electronics	http://www.samsung.com/semiconductor
ST Microelectronics	http://us.st.com