

JEDEC/FSA JOINT PUBLICATION

FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION
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Foreword

This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BiCMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The process technology owner will be required to document the details of specific testing unique to the process being qualified.

The guideline attempts to reflect common best practices in the semiconductor industry. Given the rapid rate of technology progress in the semiconductor industry, it should be updated periodically in order to ensure that it is aligned with current best practices.

Introduction

This publication, entitled 'Foundry Process Qualification Guidelines', is co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

Originally introduced as a standard, it has been approved as a publication. By its nature, this guideline encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of requirements in one place has a practical value that outweighs the case for simplicity.

Although the various tests and procedures contained in this guideline are described as "requirements", it is ultimately the marketplace of foundries and their customers that determine what constitutes an acceptable technology qualification process. It is expected that the continuing input of users of this guideline will help to keep it a relevant and useful document.

Acronyms

The following acronyms have been used in this document.

WLR:	wafer level reliability	NBTI:	negative bias temperature instability
EM:	electromigration	HTOL:	high temperature operating life
SM:	stress migration/voiding	EFR:	early failure rate
IMD:	inter/intra-metal dielectric	FIT:	Failures in time
HCI:	hot carrier integrity	THB:	temperature-humidity bias
GOI:	gate oxide integrity	HAST:	highly-accelerated stress test
VRDB:	voltage ramp dielectric breakdown	ESD:	electrostatic discharge
TDDB:	time-dependent dielectric breakdown	HBM:	human body model
QBD:	Charge to breakdown	MM:	machine model
P2ID:	plasma-process induced damage	CDM:	charged device model
BTS:	bias temperature stress	TQV:	technology qualification vehicle
TVS:	triangular voltage sweep	PCM:	process control monitor

FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

(From JEDEC Board Ballot JCB-02-86, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability, and the Fabless Semiconductor Association's Committee on Standard Foundry Process Qualification (SFPQ))

1 Scope

This document describes test and data methods for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC or other widely accepted standards.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wearout mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process via the testing of a relevant functional technology qualification vehicle (TQV), including life test. The level 2 tests are described in Section 12. Other Reporting requirements (e.g. PCM data) are also included.

2 Quality system

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request.

3 Responsibilities

The foundry whose process is being qualified has the responsibility to perform the requisite qualification tests on one or more test vehicles containing all the requisite test structures. The relevant test structures used in qualification of the process shall adhere to standard requirements and specifications as defined in this document or as referenced herein.

3.1 Level 1 qualification

The foundry is responsible for the design and implementation of the level 1 test vehicle (i.e. TESTCHIP). For the special case of a foundry customer driving process development, development of the level 1 test vehicle may be shouldered in whole or in part by the customer. The foundry shall fabricate the qualification silicon, execute the described level 1 tests and create the qualification report. The tests and qualification report may be done by the foundry or third party test vendor. The qualification requirements may be reduced for a derivative process, where the parent process has already been fully qualified at the same location.

The level 1 qualification report shall include: (1) qualification plan, (2) description of the test vehicle including relevant test structure features and dimensions, (3) summary of test methods used, (4) pass/fail criteria and (5) test results, analysis and model parameters as described in this document.

3 Responsibilities (cont'd)

3.2 Level 2 qualification

In general, the foundry is responsible for the design and implementation of the Level 2 test vehicle (e.g. SRAM or pilot product). For the special case of a foundry customer driving process development, or where the customer requires TQV data before such a vehicle becomes available, development of the level 2 test vehicle may be shouldered in whole or in part by the customer. The foundry, customer or third party test vendor may execute the Level 2 (TQV) tests and requisite failure analysis. The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results. The qualification report shall adhere to the minimum reporting requirements and format described in this document.

The level 2 qualification report shall include: (1) qualification plan, (2) description of the technology qualification vehicle (TQV), (3) test description & specification, (4) pass/fail criteria (5) test results & analysis including failure rates and (6) FA results.

While it is expected that a particular foundry methodology may differ from the methods outlined in this document, the wafer foundry should demonstrate to the customer that it has satisfactorily addressed all issues of interest. The wafer foundry should therefore provide a documented procedure and supporting data that provide an assessment of potential failure and wearout mechanisms.

4 Sample size

In general, data should come from 3 non-consecutive wafer lots, although the use of more lots is not precluded. A wafer lot is a group of wafers processed as a batch through the same or similar equipment in the same processing interval, using the same or similar conditions, materials, and methods. Typical sample sizes per lot are given in the individual test descriptions. Where applicable, confidence limits for each test population should be calculated. A conservative estimate of 40 die per wafer was made in determining sample size for tests that required the usage of all dies on the wafer.

5 Use of packages

Plastic packages with a wire-bonded die are generally used for testing of the technology qualification vehicle (TQV) or pilot product. For plastic packages, the maximum package temperature is less than the plastic glass transition temperature or 155 °C, whichever is lower. A qualification report for the standard wire-bonding process should be included. Advanced packaging (e.g. BGA, flip-chip or chip-scale) may be substituted where applicable. This, in combination with TCT and THB tests will demonstrate the assembly capability of this wafer fab process.

Side brazed ceramic packages are generally required for process wear-out tests performed at package-level at Temperatures greater than 155 °C. Consequently, wafer level testing is recommended wherever possible.

All references to temperature in the following sections imply junction temperature unless otherwise specified.

6 Reference documents

6.1 Industry standard documents

The following reference documents contain provisions that, through reference in this text, constitute provisions of this document. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based in this publication are encouraged to investigate the possibility of applying the most recent editions of the reference documents indicated below. For undated references, the latest editions of the reference document referred to applies. Check the JEDEC website at <http://www.jedec.org>.

6.1.1 Reliability assessment methodology

JEDEC JEP70-B, *Quality and Reliability Standards and Publications*.

JEDEC JEP132, *Process Characterization Guidelines*.

JEDEC JEP143, *Solid State Reliability Assessment and Qualification Methodologies*.

JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*.

JEDEC JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JEDEC JESD34, *Failure-Mechanism-Driven Reliability Qualification of Silicon Devices*.

JEDEC JESD659, *Failure-Mechanism-Driven Reliability Monitoring*.

JEDEC JEP131, *Process Failure Mode and Effects Analysis (FMEA)*.

6.1.2 Electromigration and stress migration

ASTM F1260M-96, *Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallization*.

JEDEC JESD33-A, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line*.

JEDEC JESD37, *Standard Lognormal Analysis of Uncensored Data, and of Singly Right-censored Data Utilizing the Persson and Rootzen Method*.

JEDEC JESD61, *Isothermal Electromigration Test Procedure*.

JEDEC JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature*.

JEDEC JESD87, *Standard Test Structures for Reliability Assessment of AlCu Metallization with Barrier Materials*.

JEDEC JEP139, *Guide for Isothermal Aging Method to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding*.

6.1.3 Hot carrier integrity

JEDEC JESD28, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress*. See also EIA/JEDEC JESD28-1 (addendum on data analysis).

JEDEC JESD60, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress*. See also JEDEC JESD60-1 (Addendum on data analysis).

6.1.4 Gate oxide integrity

JEDEC JESD35A, *Procedure for Wafer-Level-Testing of Thin Dielectrics*. See also addendum's JESD35-1 (test structures) and JESD35-2 (test criteria).

6.1 Industry standard documents (cont'd)

6.1.5 Endurance tests

IPC/JEDEC J-STD-020, *Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.*

JEDEC JESD22-A101, *Steady State Temperature Humidity Bias.*

JEDEC JESD22-A104, *Temperature Cycling.*

JEDEC JESD22-A108, *Temperature, Bias and Operating Life.*

JEDEC JESD22-A110, *Highly Accelerated Stress Test (HAST).*

JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices prior to Reliability Testing.*

JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits.*

JEDEC JESD51, *Special Requirements for Maverick Product Elimination.*

JEDEC JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*

JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

6.1.6 Electrostatic discharge tests

JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).*

JESD22-A115, *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM).*

JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components.*

ESD STM5.1, *Electrostatic Discharge Sensitivity Testing – Human Body Model.*

ANSI ESD STM5.2, *Electrostatic Discharge Sensitivity Testing – Machine Model.*

ANSI ESD STM5.3.1, *Charged Device Model (CDM) – Component Level.*

6.1.7 Latchup test

JEDEC JESD78, *IC Latch-Up Test.*

6.1.8 E-Test Parameters

ASTM F616-86, *Standard Test Method for Measuring MOSFET Drain Leakage Current.*

ASTM F617-86, *Standard Test Method for Measuring MOSFET Linear Threshold Voltage.*

ASTM F1096-87, *Standard Test Method for Measuring MOSFET Saturated Threshold Voltage.*

6.1.9 Quality standards

EIA-557, *Statistical Process Control Systems.*

EIA-670, *Quality System Assessment.*

ISO 9001:2000, *Quality Management Systems – Requirements.*

JESD671, *Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems).*

6 Reference documents (cont'd)

6.2 Selected references

Meeker, Q.A. and L.A. Escobar, *Statistical Methods for Reliability Data*, John Wiley, 1998.

Tobias, P.A. and D.C. Trindade, *Applied Reliability*, 2nd Ed., CRC Press, 1995.

Nelson, Wayne, "Accelerated Testing: Statistical Models, Test Plans, and Data Analyses", in *Wiley Series in Probability and Mathematical Statistics-Applied Probability*, John Wiley, 1990.

Amerasekera, E.A. and F.N. Najm, *Failure Mechanisms in Semiconductor Devices*, 2nd Ed., John Wiley, 1997.

Ohring, Milton, *Reliability and Failure of Electronic Materials and Devices*, Academic Press, 1998.

Yue, John, "Reliability", in C.Y. Chang and S.M. Sze (eds.), *ULSI Technology*, McGraw-Hill, 1996, Chapter 12.

Takeda, E. et al, *Hot-Carrier Effects in MOS Device*, Academic Press, 1995.

Amerasekera, E.A. and Charvaka Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley, 1996.

IRPS Conference Proceedings and Tutorials are an excellent source of information on current test methodologies and reliability models. (Web site www.irps.org)

Microelectronics Reliability, Pergamon Press. This journal publishes the proceedings of ESREF, the European equivalent of IRPS, along with frequent review papers.

7 Qualification test summary table

Section	Procedure	JEDEC Reference Standard(s)	Other Standards	Qual or Eng
8.1	Electromigration	JESD61, JESD87, JESD33A, JESD37, JESD63	ASTM: F1260-96 EIAJ-986	Q
8.2	Stress Migration (Stress-Induced Voiding)	JEP139, JESD87		Q
8.3	Thermal Cycling (Copper Interconnect)	JESD22-A104		Q or E
8.4	Inter/Intra Metal-Dielectric Reliability	None		Q or E
9.1	DC Hot Carrier Injection	JESD28, JESD60	EIAJ-987	Q
10.1	Voltage Ramp Dielectric Breakdown (VRDB) / Charge to Breakdown (QBD)	JESD35		Q
10.2	Time-Dependent Dielectric Breakdown (TDDB)	None	EIAJ-988	Q
10.3	Plasma Process Induced Damage (P2ID)	None		Q or E
11.1	Ionic Contamination/ Bias Temperature Stress (BTS)	None		Q or E
11.2	Ionic Contamination/ Triangular Voltage Sweep (TVS)	None		Q or E
11.3	Negative Bias Temperature Instability (NBTI)	None		Q
12.1	Long Term Life Test (HTOL)	JESD22-A108, JESD47, JESD74, JESD85, JEP122		Q
12.2	Early Life Test	JESD22-A108, JESD47, JESD74, JESD85, JEP122		Q
12.3	Temperature Cycling (TC)	JESD22-A113, JESD22-A104		Q
12.4	Temperature Humidity Bias (THB) / Highly Accelerated Stress Test (HAST)	JESD22-A113, JESD22-A101, JESD22-A110		Q
12.5	Yield Data & Defect Density Calculation	None		Q
12.6	ESD Characterization	JESD22-A114, JESD22-A115, JESD22-C101	ANSI/ESD: STM5.1, STM5.2 & STM5.3	Q
12.7	Latchup Characterization	JESD78		Q
13.1	Process Control Monitor (PCM) Characterization	JEP132	ASTM: F616-86, F617-86 & F1096-87	Q
14.1	Construction Analysis	None		Q

8 Interconnect reliability

8.1 Electromigration

Testing should be done on each via level and metal layer with any differences in design rules or process parameters, including the metal process and the inter/intra level dielectric. For instance, if metal layers and vias 2-4 have the same design rules and undergo similar processing, testing of metal 2 and connecting vias (lowest similar metal level) will suffice. Worst case stacked via structure (if known) or each permutation of stacked vias should be tested separately. Via tests should exercise electron flow both up and down in the via, thus stressing the via-to-metal interfaces.

The method described in this section may have limitations when applied to certain new technologies (e.g., Cu/Low K). In such instance, the applicability of the method should be assessed on a case by case basis.

8.1.1 Electromigration test requirements

Reference procedure	<p>ASTM F1260-96, <i>Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallization</i>.</p> <p>JEDEC JESD33-A, <i>Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line</i>.</p> <p>JEDEC JESD37, <i>Standard Lognormal Analysis of Uncensored Data, and of Singly Right-censored Data Utilizing the Persson and Rootzen Method</i>.</p> <p>JEDEC JESD61, <i>Isothermal Electromigration Test Procedure</i>.</p> <p>JEDEC JESD63, <i>Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature</i>.</p> <p>JEDEC JESD87, <i>Standard Test Structures For Reliability Assessment of Al-Cu Metallization With Barrier Materials</i>.</p>
Test parameters	<p>a) Failure criteria are defined by a percent resistance change or a short circuit detected to an extrusion monitor. The appropriate failure limit (e.g., 2%, 5% or 20% resistance change) depends on the functionality specification for the technology.</p> <p>b) Relative resistance change is defined as: $[(R_{INITIAL}-R_{FINAL})/R_{INITIAL}]$, where $R_{INITIAL}$ is initial resistance and R_{FINAL} is final resistance, as measured at the stress temperature.</p>
Test structures	<p>Test structures shall be designed for each combination of line and via/contact per JEDEC JESD87, <i>Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials</i>.</p>
Vehicle	<p>Test structures may be stressed at package or wafer level. For package level tests, ceramic packages should be used.</p>
Method	<p>a) Constant Current stressing at 150 °C – 250 °C or isothermal stressing at 150 °C – 350 °C. Performing the test at higher temperatures may be suitable in certain cases (e.g., for Cu metallization). For package tests, current densities should be chosen to minimize joule-heating.</p> <p>b) The test plan should allow for extraction of activation energy and current density exponent for Black's equation model, consistent with JESD63.</p> <p>c) Consistent with ASTM F1260-96, resistance increase of the test structure and an indication of a short circuit by the extrusion monitor shall be measured within periods that are much shorter than the anticipated time of the test. Continue each experiment in the test plan at least until the number of failures reaches the larger of the following conditions:</p> <ol style="list-style-type: none"> 1) at least 50% of the samples have failed, or 2) at least 12 samples have failed when the experiment sample size is ≤ 24. <p>d) Failure analysis of representative failure samples is recommended. (If No Failure analysis is done, data analysis based on % cumulative failure may be misleading, when different fail mechanisms are present)</p>
Cautionary Note	<p>The methodology outlined above allows for the derivation of an EM model for the metallization being tested. If the suggested sample requirements and/or the minimum number of allowed failures are not followed, it may not be possible to derive such a model. However, it may be possible to establish a lower bound on lifetime for a given set of stated conditions, and demonstrate that qualification goals are met.</p>

8.1 Electromigration (cont'd)

8.1.1 Electromigration test requirements (cont'd)

Model to be used	<p>Black's Model</p> $t_{50} = A_j^{-N} \exp\left(\frac{E_A}{kT}\right)$ <p>a) Plot failure times on a logarithm scale versus a Normal probability scale of cumulative percent failed and obtain estimates of t_{50} (hours) and s, for each experimental condition, as per JESD 37 or equivalent.</p> <p>b) Calculate 90% confidence intervals for t_{50} and s. For uncensored data, use JESD37 or equivalent for confidence intervals. For censored data, document the method used to determine confidence intervals.</p> <p>c) Determine current density exponent (N) and activation energy (E_A) from the data, as per JESD63.</p> <p>d) Bimodal distributions, where encountered. The weaker distribution should be modeled independent of the main population where feasible, considering the number of failures.</p>
Sample size and stress conditions	<p>a) Samples from a minimum three lots are to be tested at one current density/temperature combination, for all test structures referenced under "Test Structures" above.</p> <p>b) Samples from one lot are to be used for determination of Black's equation parameters. Three current densities ($J_1 > J_2 > J_3$) and three temperatures ($T_1 > T_2 > T_3$) are recommended. Current density and temperature values should be within the limits outlined under "Method" above.</p> <ul style="list-style-type: none"> - For determining activation energy, stress three groups at J_1/T_1, J_1/T_2, and J_1/T_3. - For determination of current density exponent, stress three groups at J_1/T_1, J_2/T_1, and J_3/T_1. <p>c) Sample Size Considerations</p> <ul style="list-style-type: none"> i) A minimum starting sample size of 15 per experiment (for each test structure for each unique set of test conditions) is required to provide accurate estimation of t_{50} & sigma; a minimum sample size of 20 is recommended. ii) A minimum of 12 valid time-to-fail data points is required (for each test structure for each unique set of test conditions) for determination of t_{50} and sigma. If there are less than 12 valid time-to-fail data points for an individual experiment, that experiment must be run again. iii) No more than 50% of the sample data can be censored, i.e. at least 50% of the samples must be taken to failure. iv) In a multi-cell test, the 50% failure requirement may be waived for the cell with the lowest acceleration.
Merit number	<p>a) Calculate time for < 0.1% Failure ($t_{0.1}$) at maximum design rule current density at the maximum operating junction temperature for the technology (Based on formula: $t_{0.1} = t_{50} \exp[-3.09 s]$, where s and t_{50} are nominal values from the measurements, not upper or lower confidence bounds).</p> <p>b) Calculate maximum current density (J_{MAX}) using the following conditions: 0.1% failure; maximum operating junction temperature (T_{USE}); 100,000 hours lifetime; J_{STRESS} and T_{STRESS}, and associated nominal values of s and t_{50}, from stress condition J_1/T_1; and nominal values of E_A and n.</p> <p>NOTE Both T_{USE} and T_{STRESS} must include applicable joule heating (per JESD33A) and are in kelvin.</p> $J_{MAX} = J_{STRESS} \cdot \left\{ \frac{\left[t_{50} \cdot \exp\left(3.09_{(for\ 0.1\%)} \cdot s + \frac{E_A}{8.617 \times 10^{-5}} \left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}} \right) \right) \right]}{100,000 \text{ hrs}} \right\}^{\left(\frac{1}{n}\right)}$
Other data required	<p>a) Line width, thickness, sheet resistance and composition of metal lines, via dimensions and measurements of alignment of via/contact layers to their respective metal layers.</p> <p>b) In the event that failure distributions are bi-modal, or if early failures occur, failure analysis should be provided to compare the failures of the different distributions.</p>

8.1 Electromigration (cont'd)

8.1.2 Reporting requirements

- 1) Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
- 2) Back end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric.
- 3) Relevant design rules: minimum widths, minimum spacing, contact and via sizes, minimum overlaps of metal to contact and via, maximum current densities.
- 4) Brief description of test structures (metal level, line width & length, number and placement of contacts or vias, etc).
- 5) For each experiment in the experimental plan:
 - a) Test conditions (Nominal T_{STRESS} , Actual T_{STRESS} , J_{STRESS})
 - b) Starting Sample size, lognormal plot of failure time data, percent valid fails at end of test.
 - c) Sample estimates (nominal values) of t_{50} and sigma with their 90% confidence limits, and the method used to determine sample estimates and confidence intervals.
- 6) Extracted Black's equation parameters: activation energy (E_A), current density exponent (N) consistent with JESD63, and pre-exponential factor (A) using Black's model.
- 7) Projected sample estimated lifetime for 0.1% failure @ maximum current density at the maximum operating temperature, using nominal t_{50} and sigma.
- 8) Maximum current density for 0.1% failure at the maximum operating temperature for the technology being evaluated, for 100,000 hours.
- 9) Construct a 90% confidence interval about the best fit projected lifetime at the maximum operating temperature and maximum current density. Compare this confidence interval to the qualification pass criteria, (the pass criteria is not specified in this document), to judge the risk that repeating the qual will result in a fail outcome.

8.2 Stress migration (stress-induced voiding)

This test is required for Aluminum interconnects. Testing should be done on all metal layers which differ from previous technologies in dimensions, passivation or metallization and interconnections (vias, studs, etc.). For technologies which use the same processes for multiple layers, the focus should be the layers with the smallest groundrules and the thickest total passivation layer (typically M1).

NOTE The methodology outlined below allows for the modeling of stress voiding for the metallization process. If the methodology is not adhered to, or if it was not possible to collect adequate failure statistics, it may not be possible to extract a degradation model.

8.2 Stress migration (stress-induced voiding) (cont'd)

8.2.1 Stress migration/ stress-induced voiding requirements

Reference procedure	JEP139, <i>Guide for Isothermal Aging Method to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding</i> . JEDEC JESD37, <i>Standard Lognormal Analysis of Uncensored Data, and of Singly Right-censored Data Utilizing the Persson and Rootzen Method</i> . JEDEC JESD87, <i>Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials</i> .
Test parameters	Relative resistance change per JEP139.
Test structures	1) Metal lines: Kelvin-connected serpentines & mazes with min line width, and lengths $\geq 5,000\mu\text{m}$ 2) Via chains: Short-line and long-line chains of which the metal lines should be $\geq 5,000\mu\text{m}$
Vehicle	Wafer Level or package level
Method	Per JEP139, For a completely new metallization: 1) Select 10 wafers from each of 3 wafer lots (total 30 wafers) 2) Measure sheet resistances and line resistances of relevant structures 3) Separate wafers into five groups: 2 wafers per lot in each group 4) Age the five wafer groups at 5 different temperatures (e.g. 175, 200, 225, 250 & 275 °C) 5) Take readouts of resistance measurements at selected intervals (e.g. 24, 48, 100, 250, 500, 750, 1000 & 2000 hours) 6) Per JEP139, failure criterion is a percent increase in resistance, dependent on the functionality requirements of the technology. 7) Plot the failure times on a lognormal probability plot (per JESD37) to determine sample estimates of t_{50} and sigma and to check log-normality of the data. 8) Determine effective activation energy, Δh (per JEP139) 9) Determine acceleration factor, AF (JEP139 equation 3) NOTE An abbreviated version of this procedure is acceptable for well-understood processes, and would permit using just one wafer per lot and three temperatures, which would embrace the temperature of peak voiding. OPTIONAL To further understand the impact of stress-induced voids on the metal interconnects, a wafer level or package level electromigration test can be performed on the aged samples, as well as unstressed samples from the same lot.
Model to be used	Per JEP139: $t_{\text{FAIL}} = A \cdot (1/\Delta T^2) \cdot \exp(\Delta h/kT)$, where t_{FAIL} = time to failure (failure defined as a % increase in resistance) ΔT = Difference between test temperature and passivation deposition temperature Δh = Effective activation energy for stress migration
Sample size	120 (20 Die * 2 Wafers * 3 Lots) per temperature, per metal level, or as appropriate to obtain a statistically valid sample and provide spatial information.
Merit number	1) Acceleration Factor, AF 2) Calculate time for 0.1% Failure at the maximum operating temperature (Based on formula: $t_{0.1} = t_{50} \cdot \exp[-3.09 \sigma]$, where σ is determined from the measurements.) 3) Maximum operating temperature for 0.1% failure at 100,000 hours. Alternate merit numbers may be provided by the foundry, supported by the appropriate model.
Other data required	Test structure characteristics: width, height, length, resistance, and relative alignment of metal to via.

8.2 Stress migration (stress-induced voiding) (cont'd)

8.2.2 Report requirements

- 1) Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
- 2) Back end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric, passivation deposition temperature.
- 3) Relevant design rules: minimum widths, minimum spaces, contact and via sizes.
- 4) Brief description of test structures and test conditions (T_{STRESS})
- 5) Sample size, lognormal plot of failure time data, percent fails at end of test, lognormal t_{50} and sigma.
- 6) Extracted parameters for stress migration model: activation energy, pre-exponent.
- 7) Projected lifetime for 0.1% failure @ the maximum operating temperature.

8.3 Thermal cycling (copper interconnects)

This test May be done during qualification, or as part of an engineering study. A thermal cycling measurement is required during qualification to assure the robustness of Cu/SiO₂ and/or Cu/low-k stacks in terms of voiding or delamination of the copper interconnects. For all other combinations with aluminium interconnects thermal cycling is not required. Testing should be done on all metal layers and via/contact level and various combinations of those.

8.3.1 Thermal cycling test requirements

Reference procedure	No JEDEC standard available. However, stress conditions should be equivalent to those applied to the pilot product (TQV) at package level, per JESD22-A104. <i>JESD87, Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials.</i>
Test parameters	The resistance shift of the interconnect structure is recorded during thermal cycling.
Test structures	The same test structures as for stress migration measurements can be used: <ol style="list-style-type: none"> a) Metal layer x and metal layer x+1 with a single via/contact (or a sea of vias). Using the design rules, the geometry of one metal layer is a wide line, e.g., large area of metal, while the geometry for the other is min (narrow line). All permutations should be covered, especially when metal layer material (from Cu to Al) or IMD changes (e.g., from low -k to SiO₂) from one metal level to the next. b) Stacked via/contact structures of all permutations should be tested especially with maximum and minimum geometries allowed by the design rules. c) Via/contact chains with minimum via/contact geometries and minimum spacing between vias/contacts and minimum line widths. Lines can form any type of serpentes or mazes.
Vehicle	Wafer level stress in oven, or self-heated.
Method	Do one of the following: <ol style="list-style-type: none"> a) 500 cycles from -65 °C - +150 °C, or b) 1000 cycles from -55 °C to +125 °C, or c) An equivalent temperature range may be used with different upper and lower temperature limits but the same ΔT (e.g. +30 °C to +210 °C). d) Alternative cycling scheme and range with technical justification. <p>NOTE 1 For cases (a) or (b) above, the temperature ramp rate and soak conditions are as specified in 22-A104. NOTE 2 Alternate scheme may include the use of a heated wafer chuck, or possibly a self-heated structure.</p>
Model to be used	None available. In the absence of a proven model, only field product evaluations would prove conclusively the reliability of the process.
Sample size	Minimum: 120 (all die on the wafer * 1 wafer * 3 lots) per temperature for all permutations of the test structures or as appropriate to obtain statistically valid samples and provide spatial information. The measured devices should be uniformly spaced across the wafer for wafer mapping purposes.
Merit number	A significant resistance increase (e.g., > 20%) indicates severe stress voiding.
Other data required	Lot identification; wafer number; die location; details of interconnect and via/contact geometry: width, height, length, resistance before stress, relative alignment of via/contact to metal line.

8.3 Thermal cycling (copper interconnects) (cont'd)

8.3.2 Report requirements

1. Fab name and location; process name, lot number, wafer number and date code, and certification that material tested represents wafers of current process qualification.
2. Back end scheme: thickness & composition of each layer and via/contact type (tungsten etc.), inter-level dielectric, passivation deposition temperature.
3. Relevant design rules: min. widths, min. spaces, min. via/contact sizes.
4. Brief description of test conditions.
5. Sample size per lot for each measurement, plot of resistance change, percentage of fails at the end of the stress, lognormal t50% and sigma.
6. When problems occurs deliver relevant failure analysis investigations on all affected wafers for the clear identification of the root cause.

8.4 Inter/intra-metal dielectric integrity

This test May be done during qualification, or as part of an engineering study. The insulation characteristic of an inter-metal dielectric layer (IMD) is required for the case that the IMD is not SiO₂. The dielectric between metal lines of one metal layer should be stressed. The inter-metal dielectric reliability between the metal layers can be tested optionally. Testing should be performed on all IMD layers especially when the metal layer scheme changes.

8.4.1 IMD test requirements

Reference procedure	No JEDEC standard available.
Test parameters	<ol style="list-style-type: none"> a) Leakage current through the IMD at maximum operating voltage (V_{DDMAX}) before the reliability stress. b) For the ramped voltage stress test: <ul style="list-style-type: none"> ▪ Weibull distribution of the voltage to failure (V_{FAIL}). ▪ Record the complete extrinsic and intrinsic branches of the distribution. c) For the constant voltage stress: <ul style="list-style-type: none"> ▪ Weibull distribution of the time to failure (t_{FAIL}). ▪ Normal distribution of the leakage current @ V_{DDMAX} before and after stress.
Failure criteria	<ol style="list-style-type: none"> a) For the ramped voltage stress test: <ul style="list-style-type: none"> ▪ Failure is defined by the leakage current exceeding a specified value at the stress temperature, e.g., equal to the IMD leakage current specification. b) For the constant voltage stress: <ul style="list-style-type: none"> ▪ Failure is defined by the leakage current exceeding a specified value at the stress voltage and temperature. This value may be calibrated relative to the IMD leakage current specification @ V_{DDMAX}.
Test structures	<ol style="list-style-type: none"> a) Three different sizes (oxide area/capacitance between metal lines) should be tested. b) Two types of test structures are recommended for testing: <ul style="list-style-type: none"> ▪ A metal serpentine with two metal combs inserted from each side to cover both edges of the serpentine or ▪ Two metal combs inserted in each other (no serpentine).
Vehicle	Wafer level measurements.
Method	<p>Stress to be done at +125 °C or greater:</p> <ol style="list-style-type: none"> 1. Ramped voltage stress to failure, or 2. Constant voltage stress at 2 V_{DDMAX} or greater. Stress should continue until 50% or more of the samples exceed the failure criterion.

8.4 Inter/intra-metal dielectric integrity (cont'd)

8.4.1 IMD test requirements (cont'd)

Model to be used	No model established so far. Acceleration model of constant voltage gate oxide stressing can be adapted for the constant IMD stress.
Sample size	a) For the largest structure size and for all various constellations of IMD layers: Minimum 120 (20 Die · 2 wafers · 3 lots). b) For the other two structure sizes: A minimum of 40 (20 Die · 2 wafers · 1 lot) is required for all various combinations of IMD layers. The measured devices should be uniformly spaced across the wafer for wafer mapping purposes.
Merit number	1. The leakage current at operating voltage (V_{DDMAX}) before stress. 2. For the ramped voltage test: <ul style="list-style-type: none"> ▪ Defect density at $2V_{DDMAX}$, defined as: $D = (-1/A_{IMD}) \cdot \ln(1-F)$ Where F is the cumulative distribution function (CDF) for V_{FAIL} @ $2V_{DDMAX}$ and A_{IMD} is the dielectric area between the metal lines in cm^2. ▪ It is recommended to assess the area scaling of the V_{FAIL} results between the three differently sized test structures against the Poisson Model 3. For the constant voltage stress: <ul style="list-style-type: none"> ▪ No merit number is defined. However, it is possible to derive a lifetime model following a methodology analogous to that outlined in section 10.2 on TDDDB testing.
Other data required	Lot identification; wafer number; die location; thickness of IMD; details of serpentine/comb geometry: width, height, length, spacing.

8.4.2 Report requirements

1. Fab name and location; process name, lot number, wafer number and date code, and certification that material tested represents wafers of current process qualification.
2. Back end scheme: thickness & composition of each inter-level dielectric and metal layer and passivation deposition temperature.
3. Detailed description of test conditions: stress time, step time, stress bias, voltage increment, breakdown criteria, and min/start and max/stop voltage.
4. Sample size per lot for each measurement; representative plots of leakage current; percentage of initial leakage fails; Weibull distribution of V_{FAIL} data; Defect density at intersection extrinsic/intrinsic branches and V_{FAIL} at 63.2%.

9 Conducting channel hot carrier injection (HCI)

9.1 DC conducting channel hot carrier (HCI)

1. Testing should be done on the minimum geometry device for each transistor type (NMOS, PMOS, native or low V_T device, etc.). Additional device lengths may be tested for modeling purposes.
2. The degradation should be evaluated at the worst case bias conditions (refer to JEDEC procedures).
3. Lifetime extrapolation should include Burn In (if applicable) in addition to use conditions. In this case worst case stresses at Burn In should be included.
4. The failure criteria for the monitored parameters will depend on the specific requirements of the technology.
5. The lifetime calculated from this stress reflects operation at worst case dc bias. Use conditions may be ac. Product lifetime will depend on use of device in circuit, and ac stress testing and/or simulation is highly recommended.

9.1 DC conducting channel hot carrier (HCI) (cont'd)

9.1.1 DC HCI test requirements

Reference procedures	<ul style="list-style-type: none"> - JESD60, <i>A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress.</i> - JESD28, <i>A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress,</i>
Test parameters & failure criteria	<ul style="list-style-type: none"> a) A DUT is considered to fail when a chosen device parameter changes by more than the specified failure criterion at worst use condition (typically $V_{DDMAX} = 1.1V_{DD}$) at a specified end of life. Example of a typical failure criterion is 10% change in forward I_{DSAT}. b) Selection of device parameter depends on the impact of the shift in its value on circuit operation. c) Other Device parameters such as G_M, I_{DLIN}, V_{TLIN}, can be used to monitor HC degradation depending on the circuit application.
Test structures	BOTH NMOSFET / PMOSFET: Minimum and nominal channel length L (W if required) as allowed by the circuit design rules. All Voltage Supply Device options offered must be evaluated. See JESD28/JESD60 for requirements.
Vehicle	Wafer Level or Packaged Level
Method	<p>Stress Temperature: Use conditions temperature (a temperature range of 25-30 °C is recommended) The device junction temperature should be held to an accuracy of ± 2 °C for the duration of stress/test. See JESD28 and JESD60.</p> <p>Drain-Source Voltage @ stress: Test at 3-5 different V_{DS} stress conditions (see JEDEC documents for appropriate V_{DS} values)</p> <p>Gate-Source Voltage @ stress: Worst-case V_{GS} taking operating conditions into account. (This is not necessarily at Peak I_{SUB} for NMOSFET or Peak I_G for PMOSFET devices, see JESD28 & JESD60).</p> <p>Readouts: Log time scale with minimum three log-time intervals per decade (at least 3 points per decade.)</p>
Model to be used	<ol style="list-style-type: none"> 1. The time Evolution of a selected device parameter shift $Y(t)$ (excluding saturation effects) follows either: <ul style="list-style-type: none"> a) A power law: $Y(t) = C t^N$. b) A log of time dependence: $Y(t) = C \log(t)$ 2. NMOSFET HC models for a given device geometry (**) Typical HC Models (Other may be applicable) (See JESD28-1) <ul style="list-style-type: none"> a) Drain-Source Voltage (V_{DS}) model: $t_{TARGET} = t_0 \exp(B/V_{D,USE})$ b) Substrate current model: $t_{TARGET} = C (I_{B,USE}/W)^B$ c) Substrate/drain current ratio model: $t_{TARGET} * I_{D,USE} = HW (I_{B,USE}/I_{D,USE})^{-M}$ 3. PMOSFET HC models for a given device geometry (**) Typical HC Models (Other may be applicable) (See JESD60-1) <ul style="list-style-type: none"> a) Drain-source Voltage(V_{DS}) model: $t_{TARGET} = t_0 \exp(B/V_{D,USE})$ b) Gate current method: $t_{TARGET} = C (I_{G,USE}/W)^B$ <p>(**) t_{TARGET} is the time needed to reach a given a target degradation level at use conditions.</p> <p>In AC operation some duty cycle assumptions at worst case operation may be needed for a correct lifetime projection.</p> <p>HC models parameters C, t_0, HW may depend on L_{EFF} (W_{EFF} is applicable)</p>

9.1 DC conducting channel hot carrier (HCI) (cont'd)

9.1.1 DC HCI test requirements (cont'd)

Sample size	<p><u>Required</u></p> <p>a) Test nominal devices from 3 lots, 3 wafers per lot, 5 sites minimum per bias condition, at 3-5V_{DS} stress conditions.</p> <p><u>Additional</u></p> <p>b) Test nominal devices from > 10 lots with different manufacturing dates. Test 10 sites per wafer at one V_{DS} stress condition and for a given L_{EFF}. Short In line HC stresses at worst case condition can be run to provide the statistics. The resulting distribution is a measure of the HC sensitivity to intrinsic process tolerances.</p> <p>NOTE 1 <u>Process Corners</u>: The hot carrier lifetime may vary widely across a typical process window. It is a sensitive function of gate length. For this reason, extraction of hot carrier lifetime for the nominal device can yield an optimistic result. It is therefore recommended to include in the evaluation test samples that give a measure of performance near the process corners.</p> <p>NOTE 2 Data collected in part (b) is intended as supplemental data, to be collected over time, at the same time that product yield data is collected. This is not necessarily a qualification gating item.</p>
Merit number	Nominal Lifetime projection at typical temperature, 1.1 V_{DD} and nominal channel length.
Other data required	Lot identification, Wafer No., Gate oxide thickness, Channel length, Stress temperature, I_{DSAT} (at use conditions)

9.1.2 Report requirements

- 1) Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
- 2) Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness, minimum drawn device lengths and widths, minimum electrical L_{EFF} , source and drain engineering, sidewall/spacer process.
- 3) Relevant spec limits: Effective channel length and width, drain current, threshold voltage, substrate current, Gate current, Channel off current, overlap capacitance.
- 4) Brief description of test structures and test conditions.
- 5) Sample size for each stress condition.
- 6) Measured parameter ranges: drain current, substrate current, etc.
- 7) Acceleration models used and extracted parameters for these models.
- 8) Extracted parameters for the specific hot carrier degradation model used.
- 9) Projected lifetime (at $V_{DD} = 1.1 V_{DD,USE}$) at the selected failure criterion for each device used in the calculation.
- 10) Lognormal sigma of the HC shifts for a large sample size.
- 11) Construct a 90% confidence interval about the best fit projected lifetime at 1.1 V_{DD} . Compare to the qualification pass/fail criteria (not specified in this document), to judge the risk that repeating the qualification will result in a failed outcome.

10 Gate oxide integrity (GOI)

10.1 Voltage ramp dielectric breakdown (V-RAMP) & charge to breakdown (QBD)

1. Follow the V-RAMP test procedure described in JEDEC standard JESD35.
 - Test is done in accumulation mode, at room temperature.
 - Test is done at wafer level.
 - Start voltage is V_{USE} after an initial prescreen at V_{USE} .
 - Ramp rate: 1 MV/cm-s; Step duration: 0.1 s.
 - Breakdown is defined as a change in current density between successive voltage steps as defined in JESD35.
 - Post-breakdown screen is done at V_{USE} .
2. The primary purpose of this test is to evaluate the extrinsic behavior of the MOS gate oxide being qualified.
3. The V-RAMP test is usually done in accumulation. Testing in inversion is also recommended. However, care should be taken to avoid difficulties caused by certain structures, if there is no low resistance current path to the substrate.
4. The V-RAMP test should be done on both NMOS and PMOS capacitors, for every type of oxide in the technology.
5. The preferred test structure is a capacitor array dimensionally representative of product (e.g. transistor array). Various, a combination of at least three different geometry devices may be tested: isolation Edge Block (Area), Isolation Edge Finger (trench or FOX edge) and Gate Edge Finger.
6. The sample requirement to demonstrate a given target defect density may be determined by using the formula below (see JESD35), where N is the total sample size, A_{TEST} is the gate area per test structure and D_0 is the target defect density:

$$N * A_{TEST} > -\ln(1-0.95)/D_0$$

7. Distributions, not averages should be quoted.
8. The charge to breakdown (Q_{BD}) may be calculated by integrating the current density through the capacitor until the last point before breakdown. Care should be exercised in interpreting Q_{BD} , particularly for thin oxides, where there is weak correlation to oxide quality, and where Q_{BD} is a function of stress voltage.

10.1 Voltage ramp dielectric breakdown (V-RAMP) & charge to breakdown (QBD) (cont'd)

10.1.1 VRDB/ QBD test requirements

Reference procedure	JEDEC Standard JESD35.
Test parameters	<p>Record the following parameters for each capacitor tested:</p> <ol style="list-style-type: none"> 1. Initial current at nominal use voltage 2. Ramp rate, step size and step duration. 3. Breakdown voltage for each DUT. 4. Failure criterion. One or more of the following will indicate the failure point: 10x increase in current, slope change, low-voltage current increase, increase in noise level. 5. Final current at nominal use voltage. <p>NOTE Refer to discussion on thinner oxides in JESD35.</p>
Test structures	<ol style="list-style-type: none"> 1. Test both NMOS and PMOS capacitors. 2. Test structures should include either: <ol style="list-style-type: none"> a) A capacitor array dimensionally representative of product (e.g. transistor array) or b) A combination of three different geometry devices: Isolation Edge Block (Area), Isolation Edge Finger (trench or FOX edge) and Gate Edge Finger. An effort should be made to have the total area, isolation edge and gate edge tested representative of their ratios in the product. 3. Capacitor area should be large enough to produce a clear picture of the defect tail in a reasonable sample size (e.g., 10 cm² total area per oxide type for D₀~1d/cm²). 4. Where more than one oxide is used, each oxide thickness is to be tested (e.g. LV, HV).
Vehicle	Wafer Level.
Method	Automated wafer level reliability test, where the voltage is ramped up from V _{USE} (accumulation) at 1 MV/cm-s until oxide breakdown occurs.
Model to be used	<p>None.</p> <ol style="list-style-type: none"> 1. Breakdown data is to be subdivided into three populations: mode A, mode B & mode C: <ul style="list-style-type: none"> - Mode A is the population which fails at V_{USE}. - Mode B is the population that fails at a voltage > V_{USE}, but presents a reliability hazard over the life of the product. This is essentially the population that fails outside the intrinsic population. Mode C is primarily the intrinsic population, failing beyond the useful lifetime of the product. 2. The breakdown voltage distribution is to be plotted on an extreme value cumulative distribution plot, and both the intrinsic slope and extrinsic slope determined, where feasible. For low defect density oxide, or where too small a sample is used, there may be too few data points to allow determination of the extrinsic slope. <p>NOTE The Weibull distribution is one specific form of the extreme value distribution.</p>
Sample size	<p>For each oxide type:</p> <ul style="list-style-type: none"> - Minimum three lots. - Both NMOS & PMOS capacitor test structures - Minimum 10 cm² total area. <p><u>Example:</u> Assuming capacitors with area of 0.3 mm², the number of wafers to be tested would be: 1000 mm² / (2 device types * 35 sites * 0.3 mm² * 3 lots) = 16 wafers per lot. Sample size to be increased proportionately for smaller area capacitors.</p>
Merit number	<p>Report the following for each of the structures tested.</p> <ol style="list-style-type: none"> 1. Percent mode A, B & C 2. Mode A defect density. 3. Mode B density. 4. Mode C median breakdown voltage. 5. Extreme value plot of V_{BD}, with intrinsic and extrinsic slopes extracted. (OPTIONAL)
Other data required	Lot Identification, Wafer No., Die Location, Structure Name, Gate Oxide Thickness, Current Density Prior to Breakdown, Voltage at Breakdown.

10.1 Voltage ramp dielectric breakdown (V-RAMP) & charge to breakdown (QBD) (cont'd)

10.1.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness.
3. Brief description of test structures (device type, gate area, poly edge, FOX edge)
4. Brief description of test conditions (temperature, polarity, stress voltage, fail limits)
5. Sample size for each stress condition.
6. Measured parameters from oxide characterization: Ellipsometry, I-V, C-V, QM analysis.
7. Measured initial leakage at V_{USE} . Data should be presented in an extreme value plot or similar format. Where leakage data includes values > 10X the media value, a wafer map representation may be required.
8. Extracted parameters from extreme value plot: Median breakdown voltage, intrinsic slope, extrinsic slope (if sufficient data).
9. Report the following:
 - a. Percent mode A, B & C for each structure and lot tested.
 - b. Mode A and mode B defect densities.
 - c. Mode C breakdown voltage (either T_{50} or T_{63})
 - d. Optional: Extreme value plots and distribution parameters.

10.2 Time-dependent dielectric breakdown (TDDB)

1. The TDDB test is used to model the intrinsic behavior in the technology being qualified using temperature and voltage acceleration.
2. The time to fail (t_{BD}) scales inversely with voltage, temperature and the oxide area being tested.
3. At least three defect generation mechanisms have been identified in the breakdown of gate dielectrics: Impact ionization and anode hole-injection at higher voltages, and trap creation at operating voltages. (Ref 7)
4. Current evidence points to a critical defect density (N^{BD}) which may be voltage and time dependent.
5. The statistics of gate oxide breakdown are described by the Weibull distribution (Ref. 1), which is defined by the characteristic life, t_{63} , and the Weibull slope,
$$F(t) = 1 - \exp[-(t/t_{63})^b].$$
6. For thinner oxides, the first breakdown –whether soft or hard (see note) - should be used in the statistical distribution.
7. Where a field dependence model is appropriate, it is important to model the oxide thickness and oxide field accurately by taking into account quantum mechanical effects, poly depletion, leakage current and series resistance effects. (Refs. 2 & 4)

NOTE The distinction between soft and hard breakdown is based on the post-breakdown behavior of the test structure, which depends in large measure on the energy dissipated in the filamentary short. Hard breakdown results in a resistive short (several orders increase in current). By contrast, soft breakdown results in a non-zero resistive path (a few-fold increase in current).

10.2 Time-dependent dielectric breakdown (TDDB) (cont'd)

10.2.1 TDDB test requirements

Reference procedure	None.
Literature references	<ol style="list-style-type: none"> 1) R. Degraeve et al, IEDM Tech Digest, p. 863, 1995. 2) E. Wu et al, Proc. IRPS, p. 184, 1997. 3) J. W. McPherson et al, IEDM Tech. Dig., p. 171, 1998. 4) N. Yang et al, IEEE Trans. ED-46:7, p. 1464, 1999. 5) M. A. Alam et al, Proc. IRPS, p. 21, 2000. 6) E. Wu et al, IEDM Tech Digest, p. 541, 2000. 7) J. H. Stathis, Proc. IRPS, p.132, 2001. 8) M. A. Alam et al, IEEE Trans. ED-49:2, p. 239, 2002.
Test parameters	<p>Record the following parameters for each capacitor tested:</p> <ol style="list-style-type: none"> 1. Initial current at nominal use voltage 2. Initial current at start of stress. 3. Failure time for each DUT. Fit data for each stress condition on a Weibull plot to obtain t_{63} and the Weibull slope (b). 4. Final current at nominal use voltage. (optional)
Failure criterion	<ul style="list-style-type: none"> ▪ Any of several failure criteria may be used, e.g. increase in current, increase in current at use voltage or lower, increase in stress current, increase in stress current noise. ▪ For thicker oxides (> 4 nm), a 2X to 10X increase in current is typical. ▪ For thinner oxides, the first quasi-breakdown (i.e. soft breakdown) is considered the failure point.
Test structures	<ol style="list-style-type: none"> a) Test NMOS and PMOS capacitors, preferably transistor arrays reflecting actual circuit topographies. b) Optional: It is suggested that 2 capacitors of similar layout but very different areas be tested. c) Leakage current, particularly for thinner oxides, may limit test capacitor area to ~ 0.1 mm². d) Available test structures should allow testing in both inversion and accumulation. e) The test structure layout should minimize resistive voltage drop. f) Where more than one oxide is used, each oxide thickness is to be tested (e.g. LV, HV). <p>For specific test structure criteria, see JEDEC standard JESD35.</p>
Vehicle	Package or Wafer Level
Method	<ol style="list-style-type: none"> 1. Constant voltage stress (CVS) at various stress voltages and temperatures. 2. Preferably, test should be done both in accumulation and inversion. As a minimum, accumulation test data should be provided. 3. Voltage acceleration: Use > 3 voltages above $V_G > V_{DDMAX}$. 4. Temperature acceleration (optional): Use 2-3 temperatures in the range of 25-200 °C. 5. If only one temperature is used, stressing at the maximum operating temperature is recommended. 6. Stress until at least 63% of the samples have failed.
Model to be used	<p>Use an appropriate model to extrapolate to use conditions for the actual product die:</p> <p>1. Voltage and temperature acceleration – Test structure (oxide thickness > 4nm):</p> <ol style="list-style-type: none"> a) The following model for voltage acceleration is supported by published data and widely used down to ~4nm oxide thickness, $t_{BD} = t_0 \exp(-g E_{OX})$ <p>t_{BD} is the characteristic lifetime for the Weibull distribution (t_{63}), or the lifetime at $F_{WEIBULL}=0.63$. [Any other point on the distribution, t_x at $F_{WEIBULL}= x$, may be used.]</p> b) An Arrhenius temperature dependence is usually assumed: $t_{BD} \propto \exp(E_A/kT)$ <p>If E_A is not determined experimentally, a value of 0.5eV may be assumed.</p> c) The lifetime of the test structure at use conditions is then given by $t_{BD}(oper) = t_{BD}(test) * \exp\{-g E_{OX}(oper)/ E_{OX}(test)\} * \exp\{(E_A/kT_{TEST}) - (E_A/kT_{TEST})\}$

10.2 Time-dependent dielectric breakdown (TDDB) (cont'd)

10.2.1 TDDB test requirements (cont'd)

<p>Model to be used (cont'd)</p>	<p><u>2. Voltage and temperature acceleration – Test structure (~2nm < T_{OX}< 4nm):</u></p> <p>d) A conservative approach would use the exponential dependence described in (a) above. For a given oxide thickness, this is equivalent to,</p> $t_{BD} = t_1 \exp(-B V_G), \quad \text{where } V_{OX} = E_{OX} * t_{OX} = V_G - \delta.$ <p>Other models have recently been proposed, but may not be widely used. If any of these models is to be used, the data should support the assumptions in lifetime projection, and the derived model parameters.</p> <p>e) One recently proposed model for extrapolation down to 2 V is a power law dependence on V_G [E. Wu, IEDM 2000]:</p> $t_{BD} = t_0 V_G^{-N}$ <p>Extrapolation below 2V would still assume exponential dependence (linear on a log scale). The power law is determined experimentally.</p> <p><u>3. Area and failure rate scaling – Test structure to chip:</u> The lifetime obtained for the test structure may be scaled to the product chip at a specified failure rate target using the expression,</p> $t_{CHIP} / t_{TEST} = \{(A_{TEST} / A_{CHIP}) * (F_{CHIP} / F_{TEST})\}^{1/b}$ <p>where b is the Weibull slope.</p>
<p>Sample size</p>	<ul style="list-style-type: none"> ▪ Minimum one capacitor with representative topography for each device type (NMOS & PMOS) and oxide thickness ▪ Minimum 2 lots ▪ Minimum 2 wafers per lot ▪ Minimum 8 DUTs per wafer for every stress condition (voltage and temperature combination) <p>Example (3 voltages @ 1 temperature): 1 array capacitor * 2 device types * 3 voltages * 8 DUTs * 2 wafers * 2 lots = 192 DUTs</p> <p>NOTE Sample size should be increased for thinner oxide, since the Weibull slope is known to increase with decreasing thickness.</p>
<p>Merit number</p>	<p>Report either (a) or (b) below for every type of oxide tested (e.g. NMOS & PMOS for thin and thick oxides), at a target operating voltage, temperature, projected failure rate and for a specified product total oxide area:</p> <p>a) The lifetime at 0.01% cumulative failures, for a 0.1 cm² total oxide area or a specified product area.</p> <p>b) The projected failure rate at 10 years, at a target operating voltage, temperature and lifetime, for a 0.1 cm² or a specified product total oxide area.</p>
<p>Other data required</p>	<p>Lot Identification, Wafer No., Die Location, Structure Name, Gate Oxide Thickness, Current Density Prior to Breakdown</p>

10.2 Time-dependent dielectric breakdown (TDDB) (cont'd)

10.2.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness.
3. Brief description of test structures (device type, area, poly edge, FOX edge)
4. Brief description of test conditions (temperature, polarity, stress voltage, fail limits)
5. Sample size for each stress condition.
6. Measured parameters from oxide characterization: Ellipsometry, I-V, C-V, QM analysis.
7. Measured parameters from TDDB stress: Initial current density, time to breakdown, final current density
8. Extracted parameters from Weibull plot: characteristic life t_{63} , Weibull slope b .
9. Extracted parameters for oxide degradation model, e.g. Voltage acceleration factor g , activation energy E_A .
10. Projected lifetime at maximum use conditions.
11. Optional: Construct a 90% confidence interval about the projected lifetime distribution produced in item 10 above. Compare this confidence interval to the qualification pass criteria, (the pass criteria is not specified in this document), to judge the risk that repeating the qualification will result in a fail outcome. Note: this calculation may not be very meaningful unless the sample size is significantly higher than the minimum given in the table.

10.3 Plasma process-induced damage (P2ID)

1. The primary goal of this test is to confirm that the P2ID design rules are achievable by the process.
2. This test may be done as part of the qualification, or as an engineering study
3. This test is to be done on MOS transistors.
4. In many cases, it is essential to apply a stress to reveal latent damage.
5. Fowler-Nordheim (F-N), hot carrier stress (HC), conducting and non-conducting and Negative bias temperature instability (NBTI) stress may be used to reveal latent damage.
6. The effect of P2ID is reflected by the distributions before and after stress, for reference and antenna structures, of one or more of the following parameters: Threshold voltage (V_T), transconductance (G_M), drain saturation current (I_{DSAT}), drain off current (I_{DOFF}) and gate leakage at low voltage (I_{LEAK}).
7. Elapsed time considerations must not be ignored. Plasma damage may be present, with adverse effect on device reliability, even if yield at $t = 0$ is not.
8. Voltage ramp breakdown, Q_{BD} and TDDB tests have been used to monitor possible P2ID damage. However, the sensitivity of a given test or structure appears to vary with oxide thickness.
9. For thinner oxides ($\leq 5\text{nm}$), weaker parametric shifts, or no shifts at all, may be observed for a given applied stress. Initial I_{LEAK} at low voltage has been reported to be a sensitive indicator of damage. However, care should be exercised in the selection of test structures and the interpretation of data.

10.3 Plasma process-induced damage (P2ID) (cont'd)

10.3.1 P2ID test requirements

Reference procedure	<p>None.</p> <p>References:</p> <ol style="list-style-type: none"> 1. C.R. Viswanathan, 1997 Int'l Symposium on P2ID, pp. 181-185 2. K. P. Cheung, IRPS 1997 Tutorial Notes Topic 4 3. T. Hook et al, 1996 Int'l Symposium on P2ID, pp. 164-167. 4. A. Sridharan et al, 1997 P2ID, pp. 29-32. 5. K. P. Cheung et al, 2000 Int'l Symposium on P2ID, pp. 10-13.
Test parameters	<p>Wafer map distributions of reference and worst case antenna device parameters: V_T, G_M, I_{DSAT}, I_{DOFF}, and I_{LEAK}, before and after FN, HC or NBTI stress. The failure criterion is one of the following:</p> <ul style="list-style-type: none"> ▪ Parameter value is outside a defined spec. limit ▪ Parameter difference for reference and antenna device exceeds a defined percentage limit ▪ Parameter shift exceeds a defined percentage limit. ▪ Parameter spatial variation exceeds a defined percentage limit <p>The selected parameter(s) and defined pass/fail limits are to be demonstrated to be appropriate for the specific process.</p>
Test structures	<ul style="list-style-type: none"> ▪ Minimum geometry (L&W) and minimum L (wide W) NMOSFET & PMOSFET devices for each gate oxide thickness. ▪ Comparison between reference and antenna devices should be carried out on the same identical geometry and same die. ▪ The following structures of each type are to be tested: <ul style="list-style-type: none"> - Reference device: protected from plasma damage. - Devices with worst case antenna ratios for each process layer: poly, contact, metal1, etc.
Vehicle	Wafer level measurements at room temperature
Method	<p>Identical steps should be applied to reference and antenna devices:</p> <ol style="list-style-type: none"> 1. Measure parameter values across wafer. Parameters to be measured to include one or more of the following: V_T, G_M, S, I_{DSAT} and I_{DOFF}. <p>NOTE Gate leakage current should be measured at low voltage (~1V): gate to bulk and gate to source/drain.</p> <ol style="list-style-type: none"> 2. Apply stress to reveal damage using one of the following: <ol style="list-style-type: none"> a) FN Stress (gate injection). Optimum stress level to be determined for the specific process. The stress level should be sufficient to repopulate existing traps without adding excessive new damage (e.g., 10 mA/cm² for 10 sec). b) HC or NBTI stress. Stress at room temperature for conducting hot carrier, and at maximum temperature of operation (or burn-in) for NBTI or non-conducting hot carrier. Optimum stress level to be determined experimentally for the specific process. 3. Re-measure parameter values across wafer. 4. Map parameter shift across wafer. <p>CAUTION A finite charging time may be associated with FN stress or gate leakage measurements on test structures with large antenna ratio, due to the high capacitance. This may lead to an overestimation of applied stress or gate leakage current.</p>
Model to be used	None
Sample size	Suggested: 180 (20 Die * 3 Wafers * 3 Lots) This should be uniformly spaced across the wafer.
Merit number	<p>Transistor device parameters:</p> <ul style="list-style-type: none"> ▪ Percent Variation across wafer, wafer to wafer and lot to lot. ▪ Percent difference between reference and antenna structures, on a site by site basis ▪ Percent shift pre and post stress. ▪ Include wafer maps of the above distributions
Other data required	Lot Identification; wafer number; die Location; gate Oxide Thickness; details of transistor/capacitor geometry and of antenna layout (finger or area, contact array, etc.)

10.3 Plasma process-induced damage (P2ID) (cont'd)

10.3.2 Report requirements

- 1) Fab name and location; process name, lot number, wafer number and date code, and certification that material tested represents the current process being qualified. Describe protection scheme.
- 2) Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness, minimum drawn device lengths, minimum L_{EFF} .
- 3) Relevant spec limits: Effective channel length, drain current, threshold voltage, and substrate current, off current.
- 4) Brief description of test structures and test conditions.
- 5) Sample size per lot for each measurement.
- 6) Median value and standard deviation for each distribution of measured and calculated parameters for reference and antenna device before and after stress: Leakage current, threshold voltage, drain current and deltas.
- 7) Wafer maps for each measured/calculated parameter before and after stress.

11 Threshold voltage stability

11.1 Ionic contamination – bias temperature stress

This test may be done as part of the qualification, or as an engineering study. The primary goal is to confirm that the ionic contamination level introduced into the process wafers does not adversely affect the reliability or parametric control of the process.

NOTE Either the Bias Temperature Stress (BTS) (Sect. 11.1) or the Triangular Voltage Sweep (TVS) (sect. 11.2) may be used and the results reported as shown below. Demonstrate no measurable ionic contamination.

11.1.1 Bias temperature stress (BTS) test requirements

Reference procedure	None.
Test parameters	Threshold voltage shifts on parasitic (field) or gate oxide devices
Test structures	NMOS and PMOS transistor structures, with or without self-heating, processed to final metal.
Vehicle	Wafer or packaged device.
Method	Heat up device to > 200 °C, apply +0.1-0.5 MV/cm field between gate and bulk, for 60 sec (or shorter for T>200 °C). Cool down with bias applied and measure V_T^+ . Heat up device again, apply reversed field to gate for 60 sec (or shorter for T>200 °C). Cool down with bias applied and measure V_T^- . $\Delta V_T = V_T^+ - V_T^-$. V_T should be measured within 10 minutes of cool down.
Failure criteria	V_T shift
Model to be used	None
Sample size	3 lots, 1 wafer per lot, 2 devices per wafer.
Merit number	Distribution of ΔV_T
Other data required	Normal batch data

11.1 Ionic contamination – bias temperature stress (cont'd)

11.1.2 BTS report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness.
3. Brief description of test structures (device type, area, poly edge, FOX edge)
4. Brief description of test conditions (temperatures, polarities, stress voltages, stress times, fail limits)
5. Sample size.
6. Initial threshold voltage, threshold voltage shift (ΔV_T).

11.2 Ionic contamination – triangular voltage sweep

This test may be done as part of the qualification, or as an engineering study. The primary goal is to confirm that the ionic contamination level introduced into the process wafers does not adversely affect the reliability or parametric control of the process.

NOTE Either the bias temperature stress (BTS) (Sect. 11.1) or the triangular voltage sweep (TVS) (sect. 11.2) may be used and the results reported as shown below. Demonstrate no measurable ionic contamination.

11.2.1 Triangular voltage sweep (TVS) test requirements

Reference procedure	None.
Literature references	M. W. Hillen and J. F. Verwey, Chapter 8 of Instabilities in Silicon Devices, Vol. 1, edited by G. Barbottin and A. Vapaille, 1986. E. H. Nicolian and J. R. Brews, MOS Physics and Technology, 1982.
Test parameters	Mobile ion concentration from capacitor displacement current.
Test structures	a) NMOS and PMOS capacitor b) Metal-Insulator-Metal Capacitor
Method	At the temperature of > 200 °C apply +1.0 MV/cm and hold for 90 sec (or shorter for T>200 °C). Ramp down from +1.0 MV/cm to -1.0 MV/cm with 0.01 MV/cm-sec ramp rate while measuring current through the capacitor. Hold at -1.0 MV/cm for 90 sec (or shorter for T>200 °C). Ramp up from -1.0 MV/cm to +1.0 MV/cm with 0.01 MV/cm-sec ramp rate while measuring current through the capacitor. Calculate mobile ion concentration from $N_i = (\text{area under } I_{CAP} - t \text{ curve}) / [(\text{capacitor area}) \times (\text{electron charge})].$
Failure criteria	Ionic concentration (Ni) level above foundry-specified limit.
Model to be used	None
Sample size	3 lots, 1 wafer per lot, 2 capacitors per wafer
Merit number	Distribution of Ni
Other data required	Normal batch data

11.2 Ionic contamination – triangular voltage sweep (cont'd)

11.2.2 TVS report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness.
3. Brief description of test structures (device type, capacitor area, poly edge, FOX edge)
4. Brief description of test conditions (temperatures, polarities, stress voltages, ramp rate, hold times)
5. Sample size.
6. Ionic concentration.

11.3 Negative bias temperature instability in PMOS devices (NBTI)

1. This test is intended to determine the degradation in threshold voltage as a result of gate bias at high temperature. This degradation is a particular concern in PMOS devices in a dual poly process, due to boron diffusion (NBTI).
2. This mode of degradation gets worse with increasing temperature.
3. Testing should be done on the minimum geometry device. Additional device lengths may be tested for modeling purposes. However, this degradation mode has a weak dependence on channel length.
4. The evaluation should include a statistically valid sample to assess process corners.
5. The failure criteria for the monitored parameters will depend on the specific requirements of the technology.

11.3.1 Bias temperature stress test requirements

Reference procedures	JEDEC Committee Ballot JC-14.2-02-222: "A Procedure For Measuring P-Channel MOSFET Negative Bias Temperature Instabilities".
Reference literature	<ol style="list-style-type: none"> 1. G. La Rosa et al, IEEE Proc. IRPS, 1997, p. 282. 2. Y. F. Chen et al, IEEE Int'l Integrated Reliability Workshop, Final Report, 2000, p. 98.
Test parameters & failure criteria	<ul style="list-style-type: none"> ▪ A DUT is considered to fail when the threshold voltage changes by more than the specified failure criterion after NBTI stress at maximum negative gate voltage for an equivalent end of life (e.g., 10 years operating life). <p>The failure criterion is a user-specified voltage shift in V_{TLIN} at end of life.</p>
Test structures	PMOSFET: Min. geometry (L & W) device with separate substrate pad, for each gate oxide thickness. See JESD28 & JESD60 for requirements.
Vehicle	Wafer Level or Packaged Level
Method	<ul style="list-style-type: none"> ▪ DC Negative Gate Bias Stress with $V_{DDMAX} < V_{GS} < V_{BD}/2$ (from voltage ramp breakdown test). All other pads grounded. <u>Avoid excessive FN stress.</u> ▪ Test to be done at the maximum operating temperature (e.g., 125 °C), held to an accuracy of ± 2 °C for the duration of stress test. A higher stress temperature may be used if the activation energy is measured. ▪ <u>Readouts (at stress temperature):</u> Multiple Stress Cycle with a time accuracy of $\pm 1\%$. Times between stress cycles and intermediate measurements must be kept to a minimum.
Typical model	<p>Typical model (others may be applicable):</p> $DV_T = -A \times (1/W)^n \times (1/L)^m \times \exp(-C/V_G) \times \exp(-\Delta H/kT) \times t^P$ <ol style="list-style-type: none"> a) Time Dependence follows a power law: $\Delta V_T \sim t^P$, b) Bias dependence: Gate oxide field 1/E acceleration method: $\Delta V_T \sim \exp(-C/V_G)$ c) Temperature dependence: Arrhenius with observed delta H from 0.2 to 0.6 eV (must measure).
Sample size	5 devices per wafer per bias condition x 3 lots.
Merit number	V_T shift at end of life at 1.1 V_{DD} , lognormal median and sigma, at the maximum operating temperature.
Other data required	Lot identification, Wafer Number, Gate oxide thickness, Channel length.

11.3 Negative bias temperature instability in PMOS devices (NBTI)

11.3.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Relevant process features: device isolation scheme (LOCOS, STI), oxide thickness, minimum drawn device lengths, minimum L_{EFF} .
3. Relevant spec limits: Effective channel length, drain current, threshold voltage, and substrate current, off current.
4. Brief description of test structures, test conditions and model used.
5. Sample size for each stress condition.
6. Measured parameter ranges: drain current (I_{DSAT} & I_{OFF}), substrate current, etc.
7. Extracted parameters for BTS degradation model(s), where applicable.

12 Technology qualification vehicle (TQV) tests

12.1 Long term life test

An appropriate technology qualification vehicle - SRAM or circuit of equivalent complexity is used to get a first look at the expected long-term failure rate of the process. An SRAM size of 2MB, 4MB & 8 MB are suggested for the 0.18um, 0.15um and 0.13um generations, respectively. For other qual vehicles (e.g. ASIC), a number of circuits providing an equivalent density should be used.

CAUTION An SRAM is an excellent vehicle where the primary concern is defect density. However, it has far too uniform a topology to be a good overall qualification vehicle in cases where divergent topologies may give rise to specific reliability concerns. Other vehicles may need to be used to provide a more thorough evaluation.

The usefulness of a life test is dependent on an assessment of the dominant failure modes, as determined from a prior thorough analysis of failure modes (FMEA). See EIA/JEDEC publication JEP131.

12.1 Long term life test (cont'd)

12.1.1 Operating life test requirements

Reference procedures	JESD47, <i>Stress-Test Driven Qualification of integrated Circuits</i> . JESD22- A108, <i>Temperature, Bias, and Operating Life</i> . JESD74, <i>Early Life Failure Rate Calculation Procedure for Electronic Components</i> . JEP122, <i>Failure Mechanisms and Models for Silicon Semiconductor Devices</i> . JESD85, <i>Methods for Calculating Failure Rates in Units of FITs</i> . JEP131, <i>Process Failure Mode and Effects Analysis (FMEA)</i> .
Test structures	Appropriate technology qualification vehicle (TQV)
Vehicle	Plastic package or other appropriate package.
Method	<p>Option #1 (No voltage acceleration):</p> <ul style="list-style-type: none"> As Per JESD22-A108 Bias Life with $T_A = 125\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$. Full Functional Burn-in with $F > 100\text{ kHz}$ Total stress hours: 1008 hours. Test Points at 0, 48, 168, 504 and 1008 hours (2, 7, 21 & 42 days). <p>A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package.</p> <p>Option #2 (With voltage acceleration – see discussion under circuit bias configuration):</p> <ul style="list-style-type: none"> As Per JESD22-A108 Bias Life with $T_A \geq 125\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$. Full Functional Burn-in with $f > 100\text{ kHz}$ <p>Total stress hours and read points depend on the total acceleration factor. The total stress duration is intended to meet or exceed an equivalent field lifetime under use conditions.</p> <p><u>DRIFT ANALYSIS (optional)</u> For a statistically significant sample of devices per lot, serialize devices</p> <ul style="list-style-type: none"> Option #1: Take read and record data of key parameters drift (most sensitive to drift) at 0, 48, 168 and 500 Option #2: Take read and record data of key parameters drift at suitable intervals Analyze data to determine potential drift and report in tabular or graphical form for each parameter
Circuit bias configuration	<p><u>Option #1</u> (No voltage acceleration): $V_{CC_STRESS} = V_{CC_OPERATING}$</p> <p><u>Option #2</u> (With voltage acceleration): $V_{CC_STRESS} = \lambda V_{CC_OPERATING}$, where V_{CC_STRESS} must not exceed the device functional limits.</p> <p>NOTE 1 Unless otherwise specified, the operating voltage is the maximum operating voltage specified for the device.</p> <p>NOTE 2 In option #2, the voltage acceleration model should be obtained from specific failure data for the product under test.</p> <p>NOTE 3 The nomenclature V_{CC}, or alternatively V_{DD}, refers to the voltage(s) applied to the power supply pins.</p>
Criteria For failure	Full Functional Test and, where appropriate, I_{DDQ} and Leakage Tests.
Failure analysis	A detailed electrical/physical analysis (as required) should be done on all failures, leading to a root cause determination. This is important for ensuring that the correct acceleration model is used.

12.1 Long term life test (cont'd)

12.1.1 Operating life test requirements (cont'd)

Model to be used	<p>a) No voltage acceleration ($V_{CC_STRESS} = V_{CC_OPERATING}$):</p> <ul style="list-style-type: none"> - Arrhenius model for temperature acceleration factor (AFT): $AFT = \exp(E_A/k[(1/T_{USE})-(1/T_{STRESS})])$ $AFV = 1$ - Total acceleration factor $AF = AFT * AFV = AFT$ - T_{USE} & T_{STRESS} are junction temperatures in kelvin. - k = Boltzman's constant = $8.62E-05$ eV/K - Activation energy is to be determined from the dominant failure mechanism. (See JEP122.) <p>b) With voltage acceleration ($V_{CC_STRESS} > V_{CC_OPERATING}$):</p> <ul style="list-style-type: none"> - Correct voltage acceleration factor is to be derived for the product being stressed. If the voltage acceleration is defect driven, the following model may be used: $AFV = \exp(\alpha (V_{CC_STRESS} - V_{CC_OPERATING}))$ - Total acceleration factor $AF = AFT * AFV$ <p>NOTE 1 For the purpose of calculating the temperature acceleration factor, T_{USE} is typically NOT the maximum operating temperature. Rather, it represents an average junction temperature over the life of the product. Typical values of T_{USE} are 55 °C (consumer), 70 °C (commercial), and 85 °C (industrial).</p> <p>NOTE 2 There is no universally agreed value of E_A to be used for temperature acceleration of product failures. In the absence of a reliable model, a value of $E_A = 0.7$ eV has historically been used. It is the responsibility of the technology owner to demonstrate that a conservative model is used.</p>
Sample size	<p>Approximately equal numbers of samples shall be selected from each of three lots (minimum). The sample size shall be sufficient to demonstrate the required FIT rate, (e.g., 192 units per lot x 3 lots minimum to meet 100 FIT at 1000 hours). The FIT rate should be calculated using Chi-Square statistics at 60% confidence limits (see JESD85).</p> $l = c^2(x,n) / (2N \cdot AF \cdot t_{STRESS})$ <p>where:</p> <ul style="list-style-type: none"> $c^2(x,v)$ = Chi Square at (x, n), from Chi Square tables $x = (1-C.L.)$ and $n = (2r+2)$ C.L. = Confidence limit r = # of rejects N = Total sample size AF = Acceleration factor t_{STRESS} = Total stress time
Merit number	<ul style="list-style-type: none"> - % Failures for each lot at each read-out point. - Reliability/Failure rate Distribution Analysis with an appropriate failure distribution model. - FIT rate at 1000 hours or final test point (exclude early life failures)
Other data required	Standard Lot Data

12.1 Long term life test (cont'd)

12.1.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. % Failures for each lot at each read-out point.
5. Target defect density and FIT rate requirements.
6. Calculated FIT rates at the specified read-points. Infant mortals (< 48 hours if no voltage acceleration) are excluded in the calculation of long term operating life. Specify the criteria and method of calculating FIT rate.
7. Appropriate failure analysis reports.
8. Corrective actions taken.
9. Drift analysis results. (optional)

NOTE Early life failures are excluded from Long Term Life FIT rate calculation. They are separately accounted for in the DPPM limits for early life.

12.2 Early life test

An appropriate technology qualification vehicle (TQV) is to be used to get a first view on the expected infant mortality rate of the process. It may be possible to utilize early data from the long term life test to fulfill the objective of this section.

12.2 Early life test (cont'd)

12.2.1 Early life test requirements

Reference procedure	JESD47, <i>Stress-Test Driven Qualification of integrated Circuits</i> . JESD22- A108, <i>Temperature, Bias, and Operating Life</i> . JESD74, <i>Early Life Failure Rate Calculation Procedure for Electronic Components</i> . JEP122, <i>Failure Mechanisms and Models for Silicon Semiconductor Devices</i> . JESD85, <i>Methods for Calculating Failure Rates in Units of FITs</i> .
Test structures	Appropriate technology qualification vehicle
Vehicle	Plastic Package or other appropriate package.
Method	As Per JESD22- A108 Bias Life with $T_a = 125^\circ\text{C}$ and $125^\circ\text{C} < T_j < 150^\circ\text{C}$, 48 hours <ul style="list-style-type: none"> • Dynamic Burn-in with $F > 100$ kHz • Test Points at 0 & 48 hours. Intermediate readout points may be added as required. A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package.
Circuit bias configuration	$V_{CC_STRESS} = V_{CCMAX}$ (typically $1.1 \times V_{CC_NOMINAL}$)
Criteria for failure	Full Functional Test and, where appropriate, I_{DDQ} and Leakage Tests.
Model to be used	<p>a) Arrhenius model for temperature acceleration factor (AFT)</p> $AFT = \exp(E_a/k[(1/T_{USE}) - (1/T_{STRESS})])$ <ul style="list-style-type: none"> - T_{USE} & T_{STRESS} are junction temperatures in kelvin. - k = Boltzman's constant = $8.62E-05$ eV/K - Activation energy is to be determined from the dominant failure mechanism. <p>b) Unless an experimentally validated voltage acceleration model has been derived, the following model is recommended:</p> $AFV = \exp[g_v \cdot (V_{STRESS} - V_{USE})]$ <ul style="list-style-type: none"> - g_v is a voltage acceleration parameter - The values of g_v for different failure mechanisms (e.g. metal particle, oxide defect) are to be determined experimentally - If $V_{CC_STRESS} = V_{CCMAX}$, then $AFV = 1$ <p>c) Total acceleration factor $AF = AFT \cdot AFV = AFT$</p>
Sample size	Approximately equal numbers of samples shall be selected from each of three lots (minimum). The sample size shall be sufficient to demonstrate the required DPPM rate, (e.g., at 60% confidence, 307 units per lot x 3 lots minimum to meet < 1000 DPPM with zero failures, or 673 per lot if one failure is allowed)
Merit number	<ol style="list-style-type: none"> 1. Percent failures for each lot at each readout point 2. Total failures in DPPM (defective parts per million) or early failure rate derived from accelerated stress.
Other data required	Standard lot data

12.2 Early life test (cont'd)

12.2.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. % Failures for each lot at every readout point.
5. Total failures in DPPM (defective parts per million) at a projected number of use hours (e.g. 3000 hours)
6. Assuming that EFR data follows an exponential distribution, DPPM is to be calculated using chi-square statistics (see JESD74):

$$\text{DPPM} = [1\text{E}6 * (\text{chi-square } c,d) / 2N] \quad @ \quad t_{\text{USE}} = t_{\text{STRESS}} * \text{AF}$$

where:

c	=	confidence level
d	=	degrees of freedom = 2*number of failures + 2
N	=	sample size
t _{USE}	=	Equivalent use hours
t _{STRESS}	=	Stress hours
AF	=	Total acceleration factor

To convert to DPPM at a different t_{USE}, the result can be normalized using the following relationship:

$$[\text{DPPM @ time } t_2] = [\text{DPPM @ time } t_1] * [t_2/t_1]$$

12.3 Temperature cycling test

12.3.1 Temperature cycling test requirements (package level)

Reference procedures	JESD47, <i>Qualification Methods</i> JESD22-A104, <i>Temperature Cycling</i> J-STD-020, <i>Moisture level preconditioning</i> JESD22-A113, <i>Preconditioning of Surface Mount Devices Prior to Preconditioning</i>
Test structures	Appropriate technology qualification vehicle
Vehicle	Plastic Package or other appropriate package.
Method	Preconditioning per appropriate MSL Level per J-STD-020 and JESD 22-A113 Temperature Cycle: 1. -65 to 150 °C (Condition C) 500 total cycles or 2. -55 to 125 °C (Condition B) 1000 total cycles Test points at 0, 100, 500, 1000 cycles. Alternatives with technical Justification may be used (see JESD47).
Circuit bias configuration	None (This test is unbiased.)
Criteria for failure	Full Functional Test and I _{DDQ} and Leakage Tests; Any requirements per J-STD-020 and JESD22-A113. Note; Sensitivity Characterization per J-STD-020 to be available
Model to be used	Coffin Mansion etc. (See JEP122)
Sample size	<u>Follow option (a) or (b):</u> a) A minimum of 231 DUTs from three lots with no more than 90 DUTs from any one lot, b) 45 parts from 3 lots for an initial foundry qual, with the understanding that data from later product quals and/or quality monitor stress can be summed up to meet the 231 total.
Merit number	- % Failure. - Distribution Analysis if failures are present
Other data required	Standard Lot Data

12.3.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g. SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. Percent failure.
6. Description of the plastic package (type, # pins, dimensions, lead-frame)

12 Technology qualification vehicle (TQV) tests (cont'd)

12.4 Temperature-humidity-bias (THB)/ highly accelerated stress test (HAST)

Either THB or HAST is required.

12.4.1 THB/HAST test requirements

Reference procedures	JESD47, <i>Qualification Methods</i> . J-STD-020, <i>Moisture level preconditioning</i> . JESD22-A113, <i>Preconditioning of Surface Mount Devices Prior to Preconditioning</i> . JESD22-A101, <i>Steady State Temperature Humidity Bias Life Test</i> . JESD22-A110, <i>Highly Accelerated Stress Test (HAST)</i> .
Test conditions	Static bias = V_{CCMAX} (typically $1.1 V_{CCNOM}$) Biasing guidelines: See JESD22-A101 (THB) or JESD-A110 (HAST) <ul style="list-style-type: none"> • THB: 85 °C/85%RH, 1000 hours • HAST: 131 °C, 85%RH, 96 hours. For interim readouts, devices should be returned to stress within the time specified in JESD22-101 or JESD22-110.
Test structures	Appropriate technology qualification vehicle. If a dc test structure is designed it should be set up for zero power dissipation under bias and maximum rated voltage for the technology. (Functional test structures will have transistor leakage)
Vehicle	Plastic package or other appropriate package.
Method	Preconditioning per appropriate MSL Level per J-STD-020 Full Functional Test and I_{DDQ} and Leakage Tests. Read points: <ul style="list-style-type: none"> • THB: 0, 168, 500 and 1000 hours • HAST: 0, 96 hours
Model to be used	See JEP122 (Peck etc).
Sample size	<u>Follow option (a) or (b):</u> a) A minimum of 231 DUTs from three lots with no more than 90 DUTs from any one lot, b) 45 parts from 3 lots for an initial foundry qual, with the understanding that data from later product quals and/or quality monitor stress can be summed up to meet the 231 total.
Merit number	% Failure
Other data required	Standard lot data

12.4.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g. SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. Total failures in DPPM (defective parts per million)

12 Technology qualification vehicle (TQV) tests (cont'd)

12.5 Yield data and defect density calculation

The Technology Qualification Vehicle (TQV) is used to get a first view on the expected yield of the process.

12.5.1 Detailed yield results

Reference procedure	None
Test parameters	Full Functional Test and I _{DDQ} and Leakage Tests
Test structures	Appropriate technology qualification vehicle
Vehicle	Wafer Probe
Method	NA
Model to be used	Foundry Will specify Yield Model
Sample size	12 wafers from each of 6 lots
Defect density	Defects per square centimeter
Other data required	Area of SRAM or other qualification vehicle, # of Critical Layers Used

12.5.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g. SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Number of devices tested, devices passed and percent yield for each wafer tested.
5. Defect density per square cm.

12 Technology qualification vehicle (TQV) tests (cont'd)

12.6 ESD characterization

The technology qualification vehicle (TQV) is used to get a first look at the ESD robustness of the process and product (especially I/O) design. As a minimum, human body model (HBM) test data should be collected. The inclusion of charged device model (CDM) data is highly recommended. The collection of machine model (MM) data, which is of interest to some customers, is optional.

12.6.1 ESD tests

Reference procedure	JESD22-A114, <i>Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)</i> . JESD22-A115, <i>Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)</i> . JESD22-C101, <i>Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components</i> . ESD STM5.1, <i>Electrostatic Discharge Sensitivity Testing – Human Body Model</i> . ANSI ESD STM5.2, <i>Electrostatic Discharge Sensitivity Testing – Machine Model</i> . ANSI ESD STM5.3.1, <i>Charged Device Model (CDM) – Component Level</i> .
Test parameters	Full Functional Test and I _{DDQ} and Leakage Tests
Test structures	I/O and power pins of appropriate technology qualification vehicle
Vehicle	Packaged TQV
Method	<u>HBM</u> : a) Test all I/O and power pin combinations per JESD22-A114-B, Table 2. b) Test in a calibrated HBM test setup using the appropriate waveform as specified in JESD22-A114-B, Table 1.
Model to be used	None
Sample size	Three devices for each voltage level tested.
Failure criteria	a) A part fails if it no longer meets the part specifications using functional and parametric testing. b) To qualify for an ESD voltage class, all devices tested must pass that voltage level in all pin combinations.
Merit number	HBM voltage level class as specified in JESD22-A114.
Other data required	Tester waveforms

12.6.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g. SRAM, ASIC), etc.
3. Test methodology & test coverage, test speed (frequency), I_{DDQ} limits.
4. HBM ESD classification.

12 Technology qualification vehicle (TQV) tests (cont'd)

12.7 Latch-up characterization

The technology qualification vehicle (TQV) is used to get a first look at the latch-up immunity of the process and ruggedness of the product design. This is a package level test.

12.7.1 Latchup test

Reference procedure	JESD78, <i>IC Latch-Up Test</i> .
Test parameters	Full Functional Test and I _{DDQ} and Leakage Tests
Test structures	I/O and power pins of appropriate technology qualification vehicle
Vehicle	Packaged TQV
Method	Samples to be tested at room temperature (Class I) and maximum ambient temperature (Class II). a) I-Test: For all devices under test, sequentially test all input and I/O pins by applying positive and negative current trigger pulses per JESD78, section 4. b) V-Test: For all devices under test, test all voltage supply pins by applying over-voltage trigger pulses per JESD78, section 4. c) After each trigger pulse, the current I-supply for each supply pin is measured.
Model to be used	None
Sample size	A minimum of six devices are to be tested.
Failure criteria	For a successful test, all devices must pass. A test device fails if any of the following occurs: a) I _{SUPPLY} for any supply pin exceeds the failure criterion for any supply pin after any input or I/O pin current trigger. b) I _{SUPPLY} for any supply pin exceeds the failure criterion for any supply pin after any supply over-voltage trigger pulse. c) Device no longer meets functional, I _{DDQ} and leakage tests.
Merit number	Class (room or max temperature) Maximum passing current trigger and voltage trigger levels
Other data required	Tester waveforms

12.7.2 Report requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g. SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Latch-up test conditions: Trigger test conditions, test temperature, failure criteria.

13 Process control monitor (PCM) characterization

13.1 PCM data

- The process control monitor (PCM) refers to the suite of test structures usually placed in the scribbleline (alternatively named kerf, street or test key) separating product die on the wafer.
- The parameter given in this section should be viewed as a suggested minimum set of E-test parameters. The foundry may choose a different set of parameters and/or tests to address specific yield, performance and reliability issues. The optimum set of parameters will depend on the specific customer product requirements.
- This list is intended for correlation of qualification data to reliability models, circuit yield and performance improvement.
- PCM parameters are to be provided for all wafers from an agreed number of lots. As a minimum, these should include wafers used in qualification reliability testing (EM, SM, HCI, GOI, etc.)
- Additional parameters may be included to meet specific customer needs or requirements.
- It is highly recommended that the same parameters (or an agreed subset) be reported for subsequent prototype and production material, as part of a standard reporting schedule.
- Test procedures are referenced where available. In all cases, the foundry should provide their specifications covering the test conditions and algorithms used, as well as the sampling plan.
- Individual site data may be provided. Histograms, probability plots and trend charts are highly desirable. As a minimum, mean, standard deviation, minimums and maximums should be provided for each lot.
- Reference procedures: JEDEC JEP132, and ASTM F616-86, 617-86 & 1096-87.

13.1.1 Requirements for logic circuits

1. MOSFET related parameters for both N and P channel MOSFETS
 - Long and wide MOSFET (NMOS and PMOS):
 - Linear threshold voltage: Single point method at a fixed current recommended. Alternate method(s) should be documented.
 - Optional: Gated diode breakdown with floating source.
 - Optional: Gamma Measured at $[V_{BS}]$ between $0 - (V_{DD}/2)K'$ (beta) (K_P) u $C_{OX} B_{VDSF}$.
 - Shortest channel MOSFET (Minimum L NMOS and PMOS):
 - Linear threshold voltage (@ $V_{DS} = 0.1 V$) and saturation threshold voltage (@ $V_{DS} = V_{DDMAX}$). Single point method at a fixed current recommended. Alternate method(s) should be documented. Optional: Repeat at $V_{sub} = -1.0 V$ for NFET and $V_{nw} = +1.0 V$ for PFET.
 - Maximum substrate (or well) current I_{SUB} : Measure at $[V_{DS}] = \text{Max. } V_{CC}$ and $[V_{GS}]$ that gives max. substrate current.
 - Drain current I_{DSAT} : Measured at $[V_{DS}]=[V_{GS}]=[V_{DDNOM}]$, $[V_{BS}]=0$. Optional: Repeat at $[V_{DS}]=[V_{GS}]=[V_{DDMAX}]$.
 - Drain OFF current I_{DOFF} : Measured at $[V_{DS}] = V_{DDNOM}$, and $V_{GS} = V_{BS} = 0$. Optional: Repeat at $[V_{DS}]=[V_{DDMAX}]$.
 - B_{VDS} transistor breakdown $[V_{GS}] = [V_S] = [V_{BS}] = 0$, @ $1\mu A I_{DSS} (I_{D0}) (I_{OFF})$
 - Delta L Channel length reduction (specify method)
 - Delta W Channel width reduction (specify method)
 - RS, RD Series resistances (from Long and Short transistors)

13.1.1 Requirements for logic circuits (cont'd)

2. Poly and metal 1 field V_T with minimum isolation spacing (NMOS and PMOS)
 - Isolation Test (e.g. field threshold voltage V_{TF} , or punch-through test). Specify Method.
3. Sheet resistances
 - Gate (poly): N+ and P+, where applicable
 - Well (N and/or P)
 - N+ diffusion
 - P+ diffusion
 - Metal (for all metal layers)
4. Contact resistance (Single contact and contact strings)
 - Gate (poly) Contact resistance
 - Well Contact resistance
 - N+ Contact resistance
 - P+ Contact resistance
 - Via (for all available via types)
 - N+ leakage measurements (from contact strings)
 - P+ leakage measurements (from contact strings)
5. Capacitances
 - Area capacitances: N+ and P+ diffusions
 - Overlap capacitances: NMOS & PMOS
6. Gate oxide integrity & gate oxide thickness
 - Gate oxide breakdown from V-RAMP test
 - Leakage at V_{DDMAX} (NMOS/PMOS area/field/gate intensive capacitors, thin/thick oxides)
 - Gate oxide thickness (from C-V, F-N or charge pumping): To be determined for NMOS and PMOS capacitors in both accumulation and inversion. For thinner oxides (especially below ~ 5nm), QM effects and poly depletion should be taken into account. (See e.g., E. Wu et al, Proc. IRPS 1997, p. 184 and N. Yang et al, IEEE Trans. ED 46, no. 7, 1999, p. 1464).
 - Optional gate oxide parameters: flat-band voltage, interface states density (via C-V or charge pumping).
7. Metal integrity
 - Non-planar technologies: Isolation & Continuity Metal1/Metal2/Metal3 over topologies for filament (also known as short, ribbon, stringer).
8. Hot carriers
 - I_{GATE} , I_{SUB} and I_D at V_{DDMAX} ($1.1 \cdot V_{DD}$) and $V_{GS} = V_{DDMAX}$ [NMOS & PMOS L_{MIN} FET]
 - I_{GATE} , I_{SUB} and I_D at V_{DDMAX} ($1.1 \cdot V_{DD}$) $V_{GS} = V_{GS}$ @ worst-case degradation condition [NMOS & PMOS L_{MIN} FET]
 - Short HCI stress on NMOS and PMOS L_{MIN} FETs under the following conditions:
 - NFET: Maximum substrate current
 - PFET: Maximum well current & $V_G = V_D$ condition
 - Optional: Charge pumping interface state parameters.

13.1.1 Requirements for logic circuits (cont'd)

9. Ionic contamination
 - BTS: Delta V_T & I_{OFF} .
10. NBTI
 - Short high temperature or field stress.
11. PID
 - Short hot carrier stress on NMOS/PMOS FETs connected to antennas to obtain ΔV_T and ΔI_{DSAT} .
12. EM
 - Short high temperature isothermal stress or similar test.

13.1.2 For mixed signal/analog circuits add the following parameters

1. MOSFET related parameters long and wide MOSFET (e.g., 50/50) (NMOS and PMOS)
 - Gamma measured at [VBS] between 0-0.5, and $VDDMAX/2 - VDDMAX$.
2. Mid channel (2X or 5X of minimum drawn channel length) (NMOS and PMOS)
 - Output conductance [GDS]. Specify range.
 - Transconductance [GMMAX] or [Peak GM]
 - Asymmetry 180 degree rotated (or source and drain reversed) MOS transistor measurement (I_{ds} % diff.)
3. Interlayer capacitors (POP, MIM, etc.)
 - TOX Interlayer dielectric thickness
4. Resistors (Implant or thin film resistors such as poly)
 - Contact resistance
 - Sheet resistances (If different than other measured sheet resistances)
 - Width reduction Calculated from resistance measurements on two resistors with different widths
 - Resistor values
 - Resistances for specific widths already measured for width calculations
5. BIPOLAR transistor parameters
 - For NPN, Lateral PNP, Substrate PNP, Isolated vertical PNP whenever applicable
 - Current gain [HFE] at defined I_C , VCE. Two measurements: one at low I_C and a second one at HFEMAX point.
 - Saturation current [IS]
 - Base-Emitter Voltage [VBE] at defined I_C , VCE.
 - Early voltage [VEARLY] extracted from two defined VCE for defined I_B
 - Collector-Emitter breakdown voltage [BVCEO] at defined I_C
 - Collector-Base breakdown voltage [BVCBO] at defined I_C
 - Collector-Emitter breakdown [BVCEC] with base-emitter shorted at defined I_C .
 - It is desirable to obtain this data for two or more geometries of a particular transistor type (e.g., NPN1x, NPN10x, etc.).

14 Construction analysis

14.1 Construction analysis

Construction analysis is an essential tool to aid in evaluating process limitations and interpreting yield and reliability data. Construction analysis data provided by the foundry as part of the qualification package allows the customer to better understand the dependencies of their product on specific design rules. This may not substitute for detailed construction analysis done by the customer on the customer's own product.

Constructional analysis shall be performed on wafer or die to check the quality features. Any anomaly which has been encountered during the constructional analysis shall be documented and communicated to the appropriate engineering group for corrective action. Additional work shall be supplemented as required by the process technology.

The constructional analysis results (visual or measurements) shall be documented in detail to demonstrate process attributes distribution. All visual documentation (Optical or SEM photos) shall display best case, typical, and worst case features. The parametric measurements shall record low, average, high and sigma values.

14.1.1 Construction analysis requirements

Reference procedure	None
Test parameters	A DUT is considered to fail if the design rule and physical measurement do not match in size shape or function.
Test structures	a) Topographical SEM photos of minimum Metal, poly b) Cross sectional SEM photos of all critical levels including each metal level, via, contact, poly, oxides and silicon isolation scheme.
Vehicle	Fully processed baseline wafers.
Method	a) Optical photographs for wide angle views and orientation location b) SEM of each individual layer and c) TEM of gate oxide and flash oxides.
Model to be used	
Sample size	Three lots with a minimum one die.
Merit number	The variation in film thickness and/or line-width should be consistent with design manual assumptions.
Other data required	Line width, thickness, composition of metal lines, via dimensions and alignment to metal lines.

14.1.2 Reporting requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Back end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric.
3. Relevant design rules: minimum widths, minimum spaces, contact and via sizes.



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