



FSA MIXED-SIGNAL/RF PDK CHECKLIST

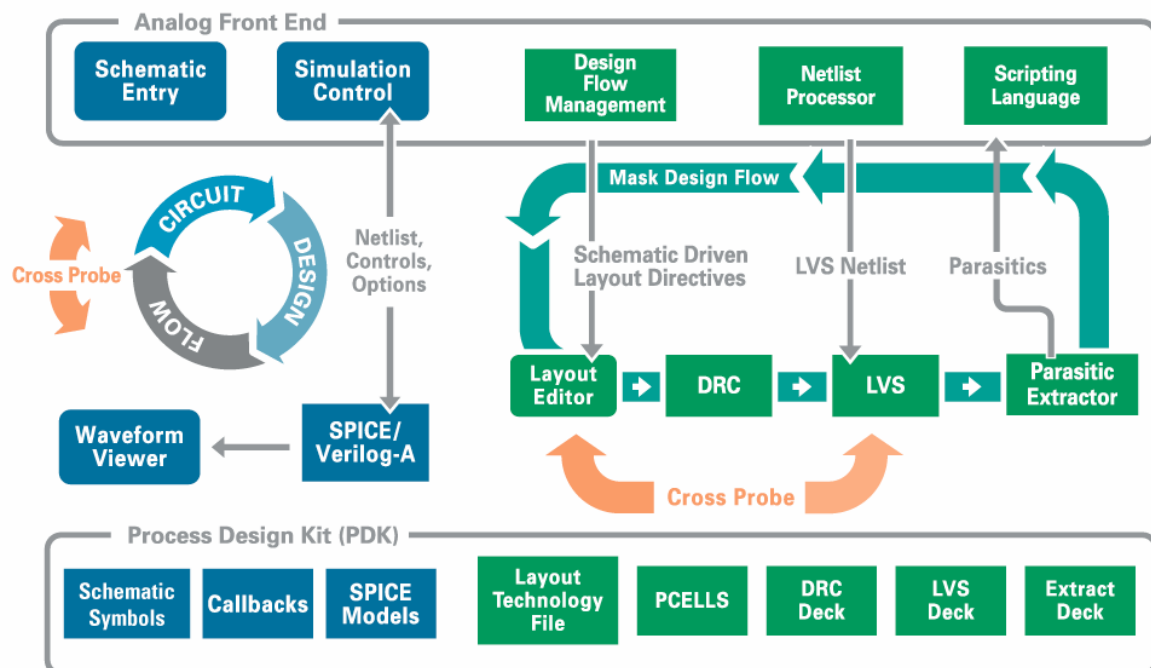
Users Guide
Version 2.0

What is the FSA Mixed-Signal/RF PDK Checklist?

The FSA Mixed-Signal/RF Process Design Kit (PDK) Checklist is a document completed by the PDK developer and delivered with each new release of a mixed-signal/RF PDK. The first page contains a process overview, relevant contact information and foundry source document references. The second page includes an electronic design automation (EDA) tool version and a device list with the deliverables and tests performed for each device. The Mixed-Signal/RF PDK Checklist references the FSA Mixed-Signal/RF SPICE Model Checklist for modeling details.

This document serves as a combination ingredients list and “nutrition facts label” for a mixed-signal/RF PDK. This document helps you obtain a better understanding of the source data, completeness and quality of the PDK before using it to design ICs or to modify it to fit into your in-house design flow.

The following diagram is an abstract of a typical mixed-signal/RF process from a foundry and a design flow from an EDA vendor interacting with a typical PDK. Each blue area represents a “front-end kit” (e.g. foundry deliverable for a process or PDK still under development) used by a circuit designer. The green areas represent a “back-end kit” used by a layout designer, which completes the PDK. Together they provide a design environment for mixed-signal/RF design. The Mixed-Signal/RF PDK Checklist summarizes what you have and where to find additional information.



Revision History

Mixed-Signal/RF PDK Checklist (Version 1.0)

- March 2004 – initial release

Mixed-Signal/RF PDK Checklist (Version 2.0)

- April 2006
- Included references to the FSA Mixed-Signal/RF SPICE Model Checklist adopted in August 2005 and referenced specific models per device with model name
- Removed redundant fields: SPICE Model Type, 1/f Noise, HF Noise and Stat Mod
- Expanded the definition of sim-test to include parameter extracted and parasitic extracted simulations
- Expanded definitions of foundry contacts, foundry documents and EDA tools
- Added revision history

Understanding and Using the Sections of the PDK Checklist

Section 1 – Foundry and Support Contact Information

This section describes how to contact the foundry if questions arise relating to the PDK.

- **Foundry** – name of foundry company and fab location (or number if relevant).
- **Process** – process code and modifiers that uniquely define the process and all process options that could affect the model or differentiate the model from another process derivative.
- **PDK Support Contact** – how to contact the foundry if questions arise relating to the PDK. It may contain a Web site URL, name, phone, fax and/or e-mail.

Section 2 - Foundry Process Documents

This section includes references to: (1) foundry documents used to create the PDK; (2) documents describing the source of data used in the PDK; or (3) the methodology and tradeoffs used to obtain PDK data. Each foundry has a different method of naming and bundling these documents into single or multiple subject documents.

- **Document Number & Title** – identifier that is used to link the document and the process, and its derivatives.
- **Section** – describes which volume or section (used when foundries put many of the documents described in this section into a single manual).
- **Revision** – many foundries use a version numbering system (0.X for pre-production, 1.X for risk production and 2.X for full production) of a model or document.
- **Date** – release date of the document or data file.
- **Design Layout Rules** - document (if separate or if in a single design manual, which section) that addresses the layout geometry rules for the process. This document (or a separate document) may include the electrical rules or process control monitor (PCM) specification for the process and the design rule checking (DRC)/layout vs. schematic (LVS)/ layout parameter extraction (LPE) runset that interprets and verifies the latest design rules (often a separate foundry document).
- **Layer Map** – document (if separate or if in a single design manual, which section) that addresses GDSII layers, colors and stipple patterns used to describe the layout for the layout editor, DRC, LVS and parasitic extraction tools.
- **DRC Runset** – executable file used by the DRC software program that contains absolute (and sometimes recommended) widths, spacings, overlaps and other rules.
- **LVS Runset** – executable file used by the LVS software program that extracts the intended devices and their parameters to compare with schematic netlists. This is

sometimes referred to as the layout parameter extraction runset and is sometimes confused with the layout parasitic extraction runset.

- **Parasitic Extraction Runset** – executable file used by the parasitic extraction software program that extracts parasitic capacitance, resistance and/or inductance from circuit layout. This is sometimes referred to as the layout parasitic extraction runset and is sometimes confused with the layout parameter extraction runset used by the LVS program.
- **Design Manual (Devices)** – name of a document that includes the design layout rules, layer map, DRC, LVS, LPE and parasitic runsets.
- **Electrical Parameters** – PCM parameters provided by the foundry to define the acceptable process corners.
- **Electrostatic Discharge (ESD) Guidelines** – guidelines that define the appropriate structures to be used to achieve various levels of ESD tolerance.
- **SPICE Model Library** – all model files (.lib or separate model cards).
- **Mixed-Signal/RF SPICE Model Checklist** – reference to the FSA Mixed-Signal/RF SPICE Model Checklist(s) that describe(s) the details of the SPICE models used in the PDK.
- **RF Parameters/Modeling** – document (if separate or if in a single design manual, which section) that addresses RF parameters and modeling issues.
- **Noise Model** – document (if separate or if in a single design manual, which section) that addresses noise model issues.
- **Matching Model** – document (if separate or if in a single design manual, which section) that addresses local process variation and mismatch (LPVM) issues.
- **Parasitic Methods** – document (if separate or if in a single design manual, which section) that addresses the methodology of extracting parasitic capacitance, resistance and inductance. It accounts for the difference between the intentional device and extracted device, and the parasitic elements within the device model and outside the device model to be accounted in the interconnect model for parasitic extraction software.

Section 3 - EDA Tools Supported and Verified for Use with the PDK Document

This section states the EDA tools supported and verified for use with the PDK. Other tool versions may or may not operate correctly with the PDK. The Checklist assumes that the EDA tools operate the same on all hardware platforms if the software version has the same version number. A single PDK can support multiple circuit simulators, DRC/LVS packages or other multiple tools. For the common case of multiple circuit simulators, the generation of netlists and model parameter verification is included as additional columns in the device tables on page 2 of the Checklist. If multiple simulators or other tools have the same level of PDK support (e.g. signoff), they may share an entry and column in the device tables.

- **Type** – foundry name for the class of the EDA tool (e.g. schematic capture, circuit simulator, RF simulator, DRC/LVS verification program).
- **Vendor and Tool** - known product name for the EDA tool (e.g. Agilent ADS, Cadence Spectre, Simucad SmartSpice, Synopsys HSPICE).
- **Level Support** – full support, full support with exceptions, or some defined subset of support with a note below, if necessary.
- **Version** – many EDA vendors use a version numbering system for their products and product platforms.
- **Version Date** – release date of the EDA tool.

Section 4 - How to Understand and Use the Device Tables

The device tables are designed to quickly give you an overview of the devices that are supported in the PDK, and are sorted by the following device types:

Device Type	Device Examples
MOS	NMOS/PMOS LV/HV, LVth/HVth, thick oxide, floating gate
BJT	NPN/PNP, LV/HV, lateral, vertical
Diodes	N+/PW, P+/NW, Zener
Capacitors	Poly-poly, MIM, MOS, MOM, tunnel, hi-Q
Resistors	N-diff, p-diff, n-well, poly0, poly1, polyn, fuse, metal
Inductors	Standard, differential
Varactors	MOS, junction, hyperabrupt
Other	Other foundry-defined devices not in the categories above

Device types are not standardized in the Checklist because of the wide variety of definitions for these devices. If the device is RF qualified (MOS, BJT, RES, CAP IND, etc.), it will be noted by the device name, comments or HF noise model column entries. The columns in the device table help you to judge the completeness of the PDK and to understand how the EDA tools listed on page 1 of the Checklist support each device. The meanings of the columns are as follows:

- **Device Type** – see table above.
- **Device Name** – foundry-defined unique name that invokes the schematic symbol and model card.
- **Model Name** – foundry-defined unique name of the SPICE model that is called when the device is simulated. This name is used in the SPICE netlist to refer to the device.
- **Comment** – a reference to a comment field to be found after the device table. Comments can be used for explanations, exceptions or limits of the device. If PDK code is delivered in non-modifiable object code, it will be noted by a comment, otherwise it will be in modifiable source code.
- **Terminals** – defines the number of terminals on the device.
- **Symbol (Schematic Symbol)** – if this box is checked, a schematic symbol exists with all terminals, is on grid and matches EDIF 2 0 0 standards.
- **Sim-Net-A** (SPICE netlist for circuit simulator A, B, C or D, as listed in the EDA tools section on page 1 of the Checklist – if this box is checked, the SPICE netlist for circuit simulator A, B, C or D was generated when the schematic symbol was invoked.
- **LVS Net** – if this box is checked, the extracted netlist successfully matched a schematic for that symbol.
- **SDL Net** – if this box is checked, the schematic-driven layout directives were generated when the schematic symbol was invoked.
- **GDS** – if this box is checked, a foundry-supplied layout for the device is included in the PDK.
- **PCELL Params** – number of scalable PCELL parameters for a device. Other documentation gives the working range (min, max, default) of each parameter. This is a proxy for the PCELL complexity you can use to determine the flexibility of the PCELL.
- **Sim-Test-A** (simulation test for simulator A, B, C or D, as listed in the EDA tools section on page 1 of the Checklist – if this box contains the letter “S,” the schematic symbol has been tested to invoke the SPICE model with correct parameters over the range of PCELL parameters. The model simulates and produces verified simulation results for the specified simulator. If this box contains the letter “L,” the “S” criteria was satisfied, the intentional device was extracted from GDSII layout using the layout parameter extraction runset and the simulation test passed as above. If this box contains the letter “P,” the “L” criteria was satisfied, the device was extracted from GDSII layout using the parasitic extraction runset and the simulation test passed as above.
- **DRC Test** – if this box is checked, all the layer and device layout rules have been implemented in the DRC rule deck and verified with a test structure.
- **LVS Test** – if this box is checked, a layout parameter netlist was extracted and successfully compared with the schematic symbol.

- **PCELL Test** – if this box is checked, an array of PCELLS over the range of the PCELL limits was instantiated and passed DRC.

PDK Checklist Feedback

Please send feedback on the usability and clarity of the FSA Mixed-Signal/RF PDK Checklist and/or Users Guide to the FSA Mixed-Signal/RF PDK Working Group at ken.brock@simucad.com.

Acknowledgments

FSA acknowledges the contributions of the following people in volunteering their participation and effort to develop and review the FSA Mixed-Signal/RF PDK Checklist:

Michael Axelrod – Tower Semiconductor	Paul Koch – Cadence Design Systems
Fereydoun Babaei - 1st Silicon	Keung Lam - 1st Silicon
John Barr – Agilent	David Lan – TSMC
Brian Bart – Simucad	Jessica McNaughton – Jazz Semiconductor
Chris Baumann – Atmel	Mishel Matloubian – Mindspeed Technologies
Ken Brock – Simucad	Robert Milkovits - Jazz Semiconductor
Laura Carlson – PolarFab	Pekka Ojala – Exar Corporation
Clif Chen – VIS Micro	Douglas Pattullo – austriamicrosystems
Mojy Chian – Mindspeed Technologies	Chris Powell – Zarlink
Marty Chiu – Simucad	David Schwan – Micro Linear
Marty Dahlke – PolarFab	Scott Springer – IBM
Nick English – OK Initiative	Jim Victory – Jazz Semiconductor
Roberto Gaertner – ZFOUNDRY	Jesse Wang – TSMC
John Garcia - HPL	Long-Ching Yeh - UMC
Riccardo Giacometti – Agilent Technologies	
Philippe Jansen – IMEC	

Important Disclosures

Copyright© 2006 by FSA. All rights reserved. FSA grants a worldwide license to all PDK developers to add their data, contact information and logo to a copy of the FSA Mixed-Signal/RF PDK Checklist and distribute it to their partners, prospects and customers; however, all references to FSA, including FSA logo and FSA references may not be altered in any way. FSA makes no claims to the accuracy of the data entered on an FSA Mixed-Signal/RF PDK Checklist.