



FSA MIXED-SIGNAL/RF SPICE MODEL CHECKLIST

Taxonomy and Definitions

Version 1.0, August 2005

Definitions for FSA Mixed-Signal/RF Model Checklist

The words/phrases and corresponding definitions in this document were selected to provide a common vocabulary and taxonomy for modeling engineers, process/device engineers, IC design engineers, and ICCAD engineers to discuss modeling concepts and issues. Each topical section (classification, extraction, noise, statistical variation, and validation) and subsection is sorted alphabetically.

Model Classification

Definitions for Model Classification

- **Active Device** – a circuit component with the ability to electrically control electron flow. (for example MOS, BJT).
- **Baseband** (or low frequency) model – a model that is used at lower frequencies (< 1-2 GHz) that has not been modified for RF operation.
- **Behavioral Model** - a set of equations written in Verilog-A and parameters for those equations to be used in a SPICE-like simulator that can input the Verilog-A language
- **Compact Model** – a set of equations and parameters for those equations to be used in a SPICE-like simulator.
- **Core Device** – the device type used for most high-performance digital functions and some high-speed analog functions; usually designed with minimum dimensions of the used geometry.
- **Design Rules** – a set of rules that define the allowed dimensions and tolerances of layers and their associated devices that can be combined, through logical operations, to create a manufacturable mask set.
- **Device** - the basic design element supported by a semiconductor process technology (e.g., transistors, resistors, capacitors, inductors).
- **Device Class** (category) - general functional category to which a device may be assigned (e.g. MOS, bipolar, resistor, capacitor, inductor, etc.).
- **Device Size** - special case of style in which the differences in behavior are considered scalable (e.g., modifying gate width in a MOS device).
- **Device Style** (lateral) - lateral variations within a device type that have the purpose of achieving specified differences in device performance, (e.g. modifying lateral layout of EBC of a bipolar transistor to achieve different V_a specifications).
- **Device Type** (vertical) - the unique combination of vertical structures that are used to construct and differentiate devices within a class, e.g. poly1 resistor, poly 2 resistor.
- **Dummy** – an element that is added to maintain dimensional control of the device in the manufacturing environment.
- **Extracted Device** - devices which do not appear in the schematic diagram but which are added to the electrical circuit representation (netlist) through analysis of the physical circuit implementation.

- **Finger** – an individual device that can be combined with identical circuit elements with common terminals to increase the parametric performance of the device, or to allow improved matching of the device.
- **Global Model** – a single model that fits across the whole length/width/voltage/temperature range of the device.
- **I/O Device** – the device type that is typically used for I/O functions. The I/O device usually supports a larger (legacy) power supply voltage than the core, and thus can also be used for analog function that requires larger voltage headroom.
- **Instance Parameters** (allowed design variables) - the properties assigned to an instance of a device that are passed to the simulator and model through the netlist and which describe directly controlled items like device size (e.g. L & W for a MOS device) and calculated items like sidewall capacitance.
- **Intentional Device** - devices which appear in the schematic diagram; these are the design elements of the circuit design.
- **Lateral Device** – a device that is built in the plane which is parallel to the wafer surface.
- **Length, L** – the direction in a lateral device that is usually parallel to current flow, or voltage drop; Length and width are interchangeable in a vertical device, and usually define device area.
- **Low Vt Device** - An analog device that is similar to the zero Vt device, except that it is an enhancement mode device, and may have been modified from the original zero vt device for improved MOS performance.
- **Main Device Element** - the portion of a device (intentional or extracted) that performs its primary desired function or most significant behavior.
- **Model Binning** – the entire allowed length width geometry range of the modeled device is divided into rectangular width and length regions, or bins; A different set of parameters is extracted for each bin. The built-in bilinear parameter interpolation scheme can be used to maintain length-width continuity at the bin boundaries.
- **Model General Behavior** - portion of a model that represents the generic behavior of a device class and type; can be made from compact model equations, behavioral models, and/or sub-circuits.
- **Model Process Parameters** - portion of a model that makes its general behavior and performance related to a specific process technology (e.g., model cards).
- **Model** - the representation of a device used by simulation to represent its function and performance characteristics; models are made from a combination of general behaviors and parameters.
- **NLE (Non Linear Effects)** – any relationships that are not purely resistive in nature.
- **NQS (Non Quasi-Static Effects)** – channel behaviors that cannot be modeled with a simple lumped impedance but require the use of transmission line distributed impedance.
- **Parameter Binning** – a subset of model parameters that can be bi-linearly interpolated over $1/L$ and $1/W$ by specifying a constant parameter, length, width and length, width product term for each of those model parameters.
- **Parasitic Device Element** - the portion of a device (intentional or extracted) that is present as a by-product of the physical implementation of the main device elements.
- **Passive Device** - a component incapable of controlling current by means of another electrical signal (e.g., varactor, resistor, capacitor, inductor).
- **Pcell (Parameterized cell)** - a software script that builds devices based on the technology design rules and user defined inputs.
- **Primary Device(s)** - devices in the supported device list that is built from the structures defined for principal devices with specific additional structures, usually involving one or more dedicated, controllable process steps (e.g., poly resistor built from gate poly with dedicated silicide block mask and implant).
- **Principal Device(s)** - the 1 or 2 devices in a technology definition around which the architecture of the process technology is defined, designed, and optimized (e.g., NMOS and PMOS devices in a digital CMOS process); Principal devices have the tightest specification tolerances.

- **Regional Scalability** – local width and length regions for which a model is deemed scalable, while it is not scalable over all allowed widths and lengths (e.g., minor deviations in width and length in an RF model might be allowed, whereas, general global variation in width and length would not be allowed).
- **RF Model** - a model in which macro model components have been added or built-in model parameters are invoked to account for the influence of parasitic devices that become apparent at high frequency (> 1-2 GHz).
- **Scalability** – the ability of a model to cover the necessary operational width and length space (e.g., baseband MOS devices that are either binned or global, are scalable for all widths and lengths that are larger than the minimum value defined in the design rules. RF models are usually not fully scalable, thus discrete models must be extracted for all width and length combinations that will be used in the technology).
- **Secondary Device** - a device in the supported device list that is built from structures that are defined, designed, and controlled for principal and/or primary devices; these are sometimes referred to as “free devices” or “intentional parasitic devices” (e.g., using metal interconnect to create an inductor or capacitor); Secondary devices typically have the widest specification tolerances.
- **Structure** - a building block that is the result from specific semiconductor manufacturing steps (e.g., implants, diffusions, contacts, interconnects, vias), that is used to construct a device; It is possible for structures to also be considered as a device.
- **Subckt (or Macro) Model** – a model that includes an intrinsic compact model and an extrinsic part to model parasitic components to form an equivalent circuit over a specified range.
- **Supported Device List** - the set of devices that are supported and controlled as part of a process technology definition; supported devices may be intentional or extracted.
- **Vertical Device** – a device that is built in the plane that is perpendicular to the wafer surface.
- **Width, W** – the direction that is perpendicular to the length of a lateral device; Length and width are interchangeable in a vertical device, and usually define device area.
- **Zero vt, or Native Device** – a device that is usually used for analog function (as a MOS capacitor, for superior MOS matching or for increased voltage headroom), which has a threshold voltage that is close to 0V, operating in either enhancement or depletion mode. The device is built in the original low doped silicon substrate that is neither nwell or pwell. In most common CMOS technologies, the zero vt device is an NMOS in p- substrate.

Extraction Information

Definitions for Extraction Information

- **Bias Condition** – value of the voltage, current or power applied to a device for its operation during a measurement.
- **Breakdown** – the point at which a device suffers permanent damage.
- **Corners** – a set of process/device quantities identifying boundaries of interest of the whole process variability (e.g., min/max for: oxide thickness, threshold voltage, drain current, etc.).
- **Extracted Parameters** – calculated values of model parameters for a given device.
- **Global Optimization** - optimization of model parameters values to fit all available curves.
- **h, z, and y Parameters** – parameters calculated from s-parameters.
- **Local Optimization** – optimization of model parameters values to fit a subset of available curves.
- **Measurement** – the result of the electrical equipment, software tools, and techniques used to measure a device’s electrical performance.
- **Model Parameters** – variables used in the SPICE’s model equations.
- **Parameter Sensitivity** – sensitivity of a parameter to the quality of fit.
- **Quality of Fit Information** – quantitative measure of goodness of model with respect to measured device’s characteristic.

- **Single or Multi-Geometry Optimization** - optimization of model parameter's values to fit multiple device sizes.
- **S-Parameters** – electrical quantities (power ratios) used to describe device behavior at frequencies where voltages/currents cannot be defined/measured.
- **Safe Operating Area** – the area in which a device will not incur permanent damage and operate within the reliability specification limits.
- **Self Heating** – rise in temperature caused by internal power consumption as opposed to ambient temperature.
- **Temperature Condition** – package temperature (for measurements on packaged parts) or chuck temperature (for measurements on wafer).
- **Worst/Best Case Model** – SPICE models representing device's electrical behavior for corners rather than for typical/average conditions.

Model Validation

Definitions for Model Validation

File Format

- **Model Filename** – unique ascii text filename from foundry. User organization may change the filename if changed or released to a design retaining a copy of original model file with revision history of the file.
- **Model Pin Lists** – terminal list of modeled devices with/without back bias pins.
- **Model Source and Developer** – who is the provider of the original model.
- **Model Type** - binned, single region, behavioral, sub-circuit used.
- **Model Version** – a system for revision sequencing and tracking model changes; includes a number and date of released version.

Electrical Specification vs. Model

- **Automated Model Checking** - computer tools to help automate electrical behavior vs. model validation.
- **Device Critical Dimensions** – MOS case: Lmin, Wmin, etc.
- **Device Model Key Physical Parameters** – MOS case: Vt, Tox, DeltaL, etc.
- **Layout Design Rules** - foundry document that defines physical layout sizing, positioning rules.
- **Operation Ranges** – voltages, currents, temperatures or other environmental conditions are the devices expected to operate and last their expected lifetime.
- **PCM (Process Control Monitoring)** - also known as Etest; parametric data usually collected on scribe lane or other device test structures at wafer functional test time used to find and control range of process targets and variation; statistical data collected from this used to create control charts, compute Cp, Cpk, help tune model corner skews.
- **PCM Data Supporting Process Specs** – foundry-provided raw PCM data to end user to assist determination of 'near typicalness' of silicon received for model validation and/or to assist model corner skews.
- **Power Supply Variations** – corners are also modulated by +/- n% power supply variation.
- **Process Corners** – CMOS case: Fastn/Fastp (FF), typical (T), Slown/Slowp(SS), hybrid corners: Fastn/Slowp (FS), Slown/Fastp(SF); Corners can be constructed to represent 3sigma, 2sigma or 1sigma of total process spec variation.

Measurements vs. Simulations

- **Absolute Maximum Error** – worst-case error of given data scan set.
- **Accuracy of Measured Data** – for a given sweep, the physical measurement accuracy for the output expressed in % of maximum and/or absolute units (eg 1mV max error for Vds).

- **Binned Model** – e.g., CMOS case: channel width/length space is divided into 2 or more abutting rectangles with each rectangle having a separate set of model parameters.
- **Corner Generation Methods** – methods to create corner models include a) Pure construction method using +/- 3, 2 or 1 sigma process variation on key parameters, b) Methods taking parameter covariance into account, c) some form of Monte-Carlo, d) 'dial a sigma' or e) "dial a spec".
- **Expected Goodness of Fit** - expected worst-case error given the type of error measurement and the scan (sweep) or measured data set.
- **Goodness of Fit** – some statistical measure of total or average or maximum error between corresponding measured and simulated data points; maximum fit error over that range expected over that range of validity (e.g., Fit <= 10% RMS over -55C to 150C).
- **Measurement Data** – TCAD simulations or physical measurements of device behavior (for MOS case e.g. IV data = IdVd, IdVg, etc.; CV data = Cgb, Cgg, etc.); other data can include noise, magnetic flux, photo output.
- **Model Validation Automation** – methods used to check goodness of fit using software tools found to be acceptable for validating model behavior and fit.
- **Range of Validity** - device model physical dimensions (e.g. W, L, fingers, contacts), biases (e.g. -0.5v to 1.2*Vdd), temperature ranges (-55C, 125C) over which model has been generated and over which its "Goodness of Fit" applies.
- **Relative RMS Error** – RMS error in percent.
- **Required Model Outputs** - model outputs based on design style – Pure Digital, vs. Analog/Mixed-signal vs. RF. Output(s) are expected to pass 'goodness of fit' criteria for key outputs. (e.g. CMOS digital case: Id in Saturation, Linear and Subthreshold scans).
- **RMS (Root Mean Square) Error** - the square root of [(sum of all simulated minus measured error data pairs squared) divided by total number of data pairs].
- **Skew** – +/- adjustments made to key 'physical like' parameters in each corner model's header region.
- **Standard Sweeps** – a set of measured data points or scans (sweeps) that illustrate goodness of fit (e.g., CMOS - IdVd scan with stepped Vgs and fixed backbias that defines the Vgs steps, Vds data scan list, and Vbs used with a minimum Vgs constrained to be > abs Vt to avoid high % error).
- **Systematic Errors in Data** – Data that shows evidence of a systematic error such as excess probe to pad contact resistance or other problem.

Anomalies

- **Convergence Problems** - to search for model behavior areas, which might have algorithmic convergence problems.
- **DSS (Device Simulation Standard) Decks** – a set of SPICE simulation decks each of which focuses on exercising the model to generate simulation data or curves to look for particular problems or behavior.
- **Expected Device Effects** – simulated semiconductor behavior that includes normal temperature dependence signs, slopes, short channel effects, continuity in model output value and derivatives. Analog design requires higher order derivative smoothness.
- **Model Rejection Criteria** – a set of errors that can be described in a machine readable format and entered into an automated anomaly checker to accept or reject a model.
- **Model Symmetry** - symmetry performance of model (e.g., – CMOS symmetric behavior if source and drain terminals are exchanged).
- **Parasitic Device Validation** – model files that have models for various problematic or useful parasitic devices.
- **Physical Behavior Curves** – sweeps that indicate physical semiconductor behavior that include no unusual kinks, negative impedances, cusps, and discontinuous jumps which may occur at 'bin' boundaries (CMOS case - W/L bin boundaries usually have finite jumps at their edges) not known to reflect 'physical' type effects.

Statistical Variation

Definitions for Statistical Variation

- **'Paper,' 'Development,' 'Production' models** – during the development of a new technology, design IP needs to be developed in parallel with the process technology. Models are usually developed and released in 3 phases: (1) paper models, based on TCAD sims, early silicon or extrapolated data, (2) development models, based on the technology at or just after the process freeze and (3) production models, based on die from a qualified process that has run a significant yielding, reliable volume of product. Specification guardbanding should get tighter at each phase. In the interest of IP development schedules, the differences between the development and production model should be minimal; production model corners should be at or inside the development model corners. Nominal silicon specs should not change more than a few percent. This is to ensure that IP developed during the development phase still works in production and that IP developed in the production phase realizes the advantage of tighter, mature manufacturing models and practices.
- **'Process' Monte Carlo** – the simulation tool selects random values for selected first order model parameters to skew for each simulation run. Large numbers of individual simulations (>35) are necessary to establish the statistical relationship between input and output parameters and the resulting circuit operation. The distribution of the local model parameter skews can be 'Gaussian' or transformations of Gaussian or 'Uniform'. The models can be set up so that elements in the simulation netlist are 'correlated', 'partially correlated' or 'uncorrelated'. Monte Carlo methodology should be noted in the model library header.
- **"Matching" Monte Carlo** – for the analog or memory design case, it is often important that active and passive devices in close proximity are 'matched'. Ideally, their device characteristics would be identical. In the real world, the device characteristics vary by small, but finite amounts. Matching monte carlo model libraries can be set up to model this effect.
- **BPV (Backward Propagation of Variance)** – a simple, efficient, and generic method of statistical circuit modeling that guarantees that the statistical circuit models match variations in key device performances. Originally described in several papers by Colin McAndrew.
- **Correlation** – for Monte Carlo simulations, process characterization can establish whether one device type is correlated to another, whether they are the same device type, the complementary device type or other active and passive device types in the same technology. The correlation can be established locally, within the die, between die, wafers, lots and fabs. Correlation can be established using PCA or the analysis of a linear correlation matrix. Correlated and uncorrelated parts can be coded into the Monte Carlo model library. Monte Carlo model library headers must note whether components are 'correlated', 'partially correlated' or 'uncorrelated'. Correlated and partially correlated models should be used with care by the designer, they do not contain the guardband built into the uncorrelated models.
- **Cp** (double sided process capability ratio) – Cp is a manufacturing index that measures if a process is capable of running within its specification limits, relative to the natural variability of the process. Cp is the ratio of spec limits to 6σ . Cp >1 implies that a process is capable of meeting the specification limits. Cp does not imply that the process is running within specification limits.
- **CpK** - Cpk is another manufacturing index that measures how close a process is running to its specification targets. The larger the index, the less likely it is that a measurement will be outside the specs. Customers usually want a Cpk of 1.33 [equivalent to 4σ].
- **Extracted Model** – the model that is created from the golden die on the golden wafer. All model accuracy measurements should be compared against the extracted model.

- **Golden Wafer or Die** – the wafer or die chosen to represent the nominal process condition for model extraction. The model created from the golden die from the golden wafer is the 'extracted' model. The golden die should be chosen such that it is as close as possible to the nominal die representing the 'process of record'. For a process with multiple CMOS device types, all device types used in the model library should be modeled from the golden die. In practice, because of the statistical nature of manufacturing, it is difficult to produce a golden die that meets all nominal parametric criteria of the process of record. In this case, the devices should be within 1σ of nominal. The model library header for each active and passive device in the model library must include traceable information about the die, and its corresponding wafer, lot and fab, used for model extraction.
- **Guardband** – the extra widening of a parametric specification to account for variance and measurement intangibles, such as measurement equipment inaccuracy, simulation inaccuracy, inaccurate predictive models, unknown process tolerances, specifications that do not require to be tight to assure component operation, requirement to minimize risk that a function must operate within its specification range, unknown temperature or voltage condition of the device under test. Wide guardbands penalize the design environment. Nonexistent or tight guardbands either demonstrate that the manufacturing process is well characterized or that manufacturing is penalized. The magnitude of the spec guardband should become smaller as a technology matures.
- **Lot** – a number of wafers processed together as a single batch
- **Model Corners** – a model that defines the extreme ranges of operation for a selected parametric sensitivity. These are known as 'F' for fast, and 'S' for slow Idsat corners, and often 'S' for Strong and 'W' for weak for corners that do not represent digital performance. For CMOS operation, NMOS and PMOS are usually in close proximity and well matched, so the NMOS and PMOS corners are grouped as 'FF', 'TT' and 'SS' for fast NMOS and PMOS, typical NMOS and PMOS and slow NMOS and PMOS respectively. The model can either be extracted from a golden die processed at the strong and weak condition, or can be skewed by modification of first order parameters. Model parameter modification can be direct, or made by using $N\sigma$ parameters. Model corners are specific to the sensitivity of the circuit being simulated. A digital circuit is sensitive to Idsat, while an analog circuit, for example, might be sensitive to MOS capacitance, hence the parametric values for corners that define the best and worst case Idsat are different than the corners that define MOS capacitance. Also known as 'process' corners. Process corners should represent a 3σ statistical probability that the corner will occur. If every variable is skewed in turn to its maximum strong and weak condition, the response range will be much wider than that which would occur by chance. Therefore, for a 3σ response (i.e., MOS Idsat), each predictor model parameter (i.e., MOS T_{ox} , V_t , DL, DW etc.) should be skewed in a typical range from 2σ to 2.5σ . The model library header and specification should list how the corners are derived and should define the response parameter that the corners serve.
- **Nominal or Typical Model** – the nominal model is either the same as the extracted model, if the golden die represents the nominal process condition, or it is a modification of the extracted model to shift, or skew, the model from measured and extracted to nominal process conditions. This model is listed as 'T', 'typical' or 'nominal'.
- **OCV (On Chip Variation)** – parametric variation across a chip due to the variation in process, voltage or temperature. Process variation is due to the inherent statistical nature of being able to reproduce a local feature. (i.e., MOS threshold voltage, oxide thickness, length, width). Voltage variation is due to local IR drop of the power supply within the chip. Temperature variation is caused by local variation in power output and self heating.
- **Off-Diagonal Corners** – for example, in CMOS, the models that define the condition for strong N weak P and weak N strong P. Due to the matching of some of the first order parameters between N and P devices, these 'corners' are usually not the true, rectangular off-diagonal points, but are closer to the nominal than the strong N strong P and weak N weak P corners.

- **Parametric Skew** – modifications made to the value of selected first order model parameters that move the model response from one known condition to another. Skews can conveniently be defined by $N \sigma$ parameters, to maintain the statistical nature of the model variation.
- **Parametric vs. Functional Yield** – in general, good parametric yield relates to good parametric control practices. A die that passes parametric sort/test implies that all parametric responses for the die pass the parametric specs (for example; I/O Vil, Vih, analog reference voltages, static I_{dd} etc.) as defined by PVT simulations. High parametric yield implies good corner modeling and IP simulation methods, good component parametric control and fab process control practices. A die that passes functional test implies that there are no fab related defects that interfere with individual component operation. Other aspects of the operation of the device, such as failure during speed tests can relate to parametric yield (i.e. control of metal sheet resistance and dimensions and dielectric thickness) or functional yield (i.e. resistive via).
- **PCA (Principal Component Analysis)** – a tool to determine correlated and uncorrelated components of datasets. The principal components analysis is a mathematical way to determine the linear transformation of a sample of points in N-dimensional space, exhibiting the properties of the sample most clearly along the coordinate axes. Along the transformed axes the sample variances are the extremes (maxima and minima), and the uncorrelated parts of the components. The name derives from the principal axes of an ellipsoid (e.g. the ellipsoid of inertia), which are just the coordinate axes in question.
- **PFA (Primary Factor Analysis)** – a form a statistical analysis that focuses on one or both of the following tasks—an assessment of underlying relationships or dimensions in the data (or what is being measured), and the replacement of original variables with fewer, new variables. PCA accomplishes basically the same analysis, is more conservative, and is the preferred method when building a model to predict parameter values from factors.
- **PCM (Parametric Control Module)** - electrical structures that are placed in the scribe line between die or within the die to evaluate the parametric performance of the die. The scribe line structures are measured after processing has been completed and before die sort. Structures placed within the die are measured at die sort. For die with very high yields, parametric test might be skipped. The parametric spec limits of the components on the PCM module should directly or indirectly relate to their corresponding simulated values at the model corners. Direct measurement might include the measured vs. simulated value of MOS I_{dsat}. Indirect measurement might include the measurement vs. simulated value of MOS ring oscillator propagation delay. A distinction must be made between 'disposition' parameters that relate directly to whether the wafer was process correctly, and whether it should proceed to die sort, or 'monitor' parameters that are used for engineering data collection. Either classification can be used for device model evaluation.
- **Physical Model Parameters** – parameters that have been extracted where every effort has been used to maintain their physical nature so that parameters can be skewed with more confidence. For MOS devices, these might include model parameters that relate to DL, DW, Tox, Vtlin, Cj, MSO capacitance Rext, etc.
- **POR (Process of Record)** – the process of record is the process sequence and conditions that create reliable, production worthy die. During process development, process variables are altered to meet the required parametric specifications. At the time in the technology development that the process meets those specifications and reliability has been demonstrated, further process changes are not allowed (or the process is 'frozen'). Ideally, models should be extracted from material that has been built at or after the process freeze date. If process changes occur after the process has been frozen, or the process is moved to another manufacturing facility or a tool used to manufacture the die is changed, such that the 'form fit or function' of the process changes, models should be checked to make sure that the pertinent parameters measured on the new process meet model specs.

- **PVT (Process, Voltage and Temperature) Corners** – model extraction engineers imply that the models are accurate across the voltage corner, defined by the simulator, as well as for the ‘temperature’ and ‘process’ corners defined by the model. Circuit designers usually include process, voltage and temperature corners to simulate the best and worst case operating conditions of the circuits.
- **Sigma, σ** - the standard deviation of a set of parametric measurements. The value of $N\sigma$ defines the probability that the measurement will occur in the range from the mean to $N\sigma$. Typically, specification limits are set as $\pm 3\sigma$.
- **Sample** – the number of units tested
- **SPC (Statistical Process Control)** – a statistical methodology to demonstrate that a manufacturing process is running in control.
- **Specification** – also known as a ‘spec’. (1) upper and lower limits applied to data derived from a manufacturing process to demonstrate that the process meets its defined tolerances; (2) Document that describes a procedure.
- **Within Die, Within Wafer, Within Lot, Within Fab Variation** – certain analog components need to be matched, it is also important to maintain parametric control within each die. At the other extreme, model corners and parametric specifications should be established, with enough guardband, so that the product can be transferred with ease, from fab to fab, and ideally from one process flow to another. Within die, within wafer, within lot, and within fab variance can be established by considering the root mean square of all variance components. Foundries should understand each of these components and how they relate to the model specs. Customers should ask for traceability so that test results can be traced back to individual fab, lot, wafer and die.

Noise

Definitions for Noise

- Γ_{opt} – source impedance corresponding to the minimum noise figure.
- **1/f Noise** – noise generated in a device that is inversely proportional to frequency, showing a decreasing linear dependence with a slope ~ 1 on a LogLog plot of noise spectral density vs frequency. 1/f noise is prominent in MOSFET devices due to interface traps at the silicon oxide surface causing carrier number fluctuations and scattering mechanisms. In BJTs, 1/f noise is present across the PN junctions. 1/f noise is present in poly silicon and silicon resistors. 1/f noise is also present in metal resistors such as thin film resistors though much smaller than silicon resistors.
- **MOSFET 1/f Noise Model** – there are three 1/f noise models available in commercial simulators associated with the BSIM model. Models other than the BSIM model are not addressed here and the foundry should specify if models other than BSIM are supplied.
 - BSIM noise model, NOIMOD=2,3 for all simulators with parameters NOIA, NOIB, and NOIC
 - SPICE ID based noise model, Noimod=1,4 for all simulators with parameters KF, AF, and EF.
 - Transconductance (GM) based noise model, Spectre:Flkmod=1, HSPICE/ADS: Nlev=2 with parameters KF and AF.
- **MOSFET Shot Noise Model**
 - Transconductance (GM) based noise model, Noimod=1,3 for all simulators
 - Inversion charge based noise model, Noimod=2,4 for all simulators
- **NFmin** – minimum noise figure is a best-case measure of the additional noise introduced by the DUT (device under test) in a 2-port measurement.
- **RF (or HF) Noise** – measure of device noise at high frequencies, typically in the GHz range. RF noise characterization includes measurements that yield the 4 RF noise parameters NFmin, Rn, Real(Γ_{opt}), Imag(Γ_{opt}). There are no additional noise sources in a device at RF frequencies, however inaccuracies in the shot noise models can become of increasing importance. Thus, a foundry may provide corrections through additional noise sources in a subcircuit model representation.
- **Rn** – the equivalent noise resistance.

- **Shot Noise** – noise generated in semiconductor devices induced by carriers crossing PN junctions. Shot noise is constant with frequency. There are no parameters to extract for shot noise in standard active device models such as BSIM for MOSFETs, Gummel-Poon, HICUM, and Mextram for BJTs.
- **Substrate Isolation** – a 2-port RF characterization of the isolation between the active device region and substrate of a given technology. For the purpose of this forum, the foundry will indicate if 2-port RF isolation characterization is provided. Substrate isolation is a measure of the immunity to substrate noise generated by one portion of a circuit to influence another circuit.
- **Thermal Noise** – noise generated by thermal fluctuations, constant with frequency, dependent on the effective resistance of the device.

IMPORTANT DISCLOSURES

Copyright© 2005 by FSA. All rights reserved. FSA grants a worldwide license to all model developers to add their data, contact information and logo to a copy of the FSA Mixed-Signal/RF SPICE Model Checklist and distribute it to their partners, prospects and customers; however, all references to FSA, including FSA logo and FSA references may not be altered in any way. FSA makes no claims to the accuracy of the data entered on an FSA Mixed-Signal/RF SPICE Model Checklist.