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Low-cost error resilient circuits for digital control paths

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Agenda

1. Single event upset (SEU)
2. Well proven mitigation techniques
3. Critical space application
4. Innovative error resilient architectures
5. Takeaways

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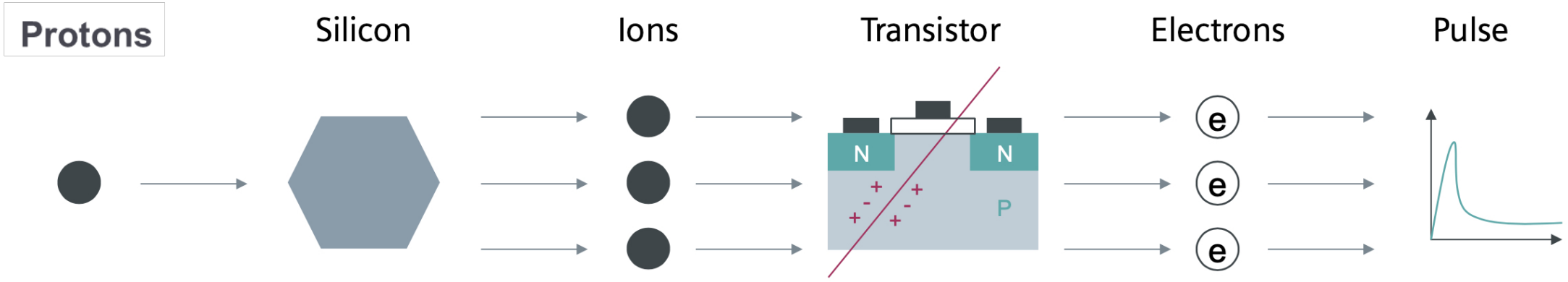
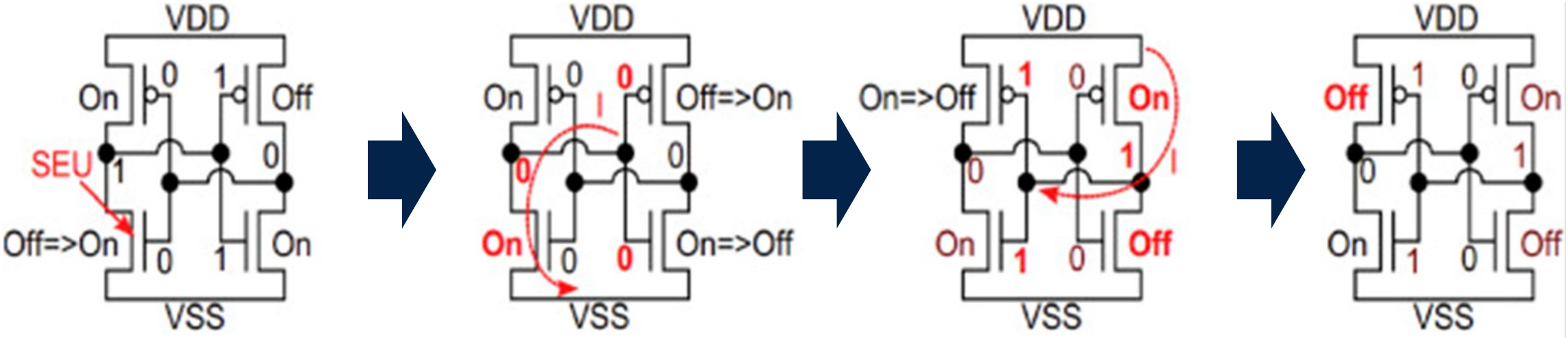
Single event upset (SEU)

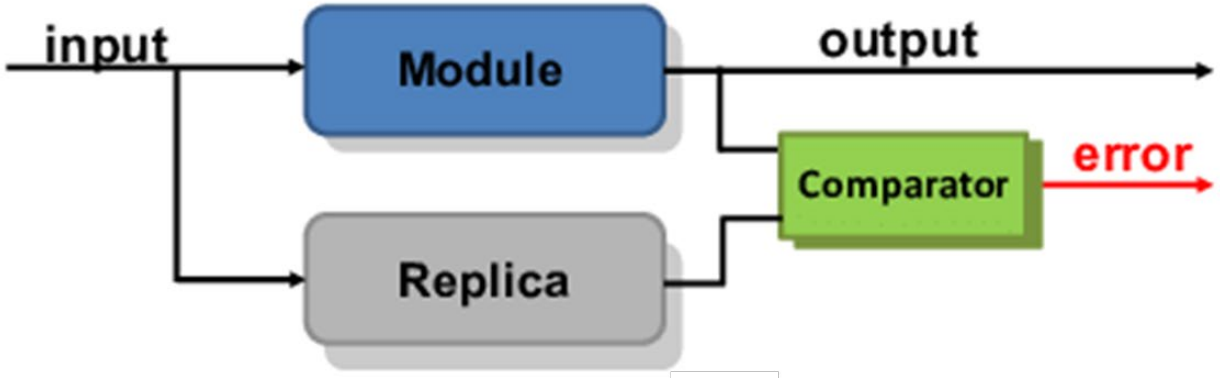




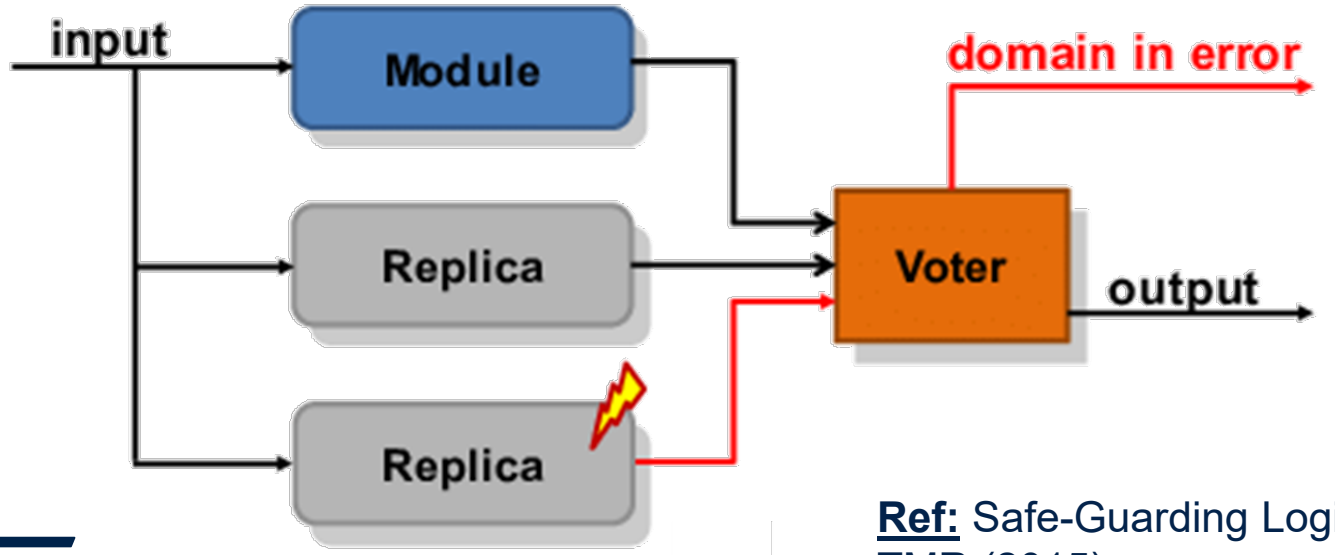
Ref: Single Event Upset (electrical-engineering.academy)

Ref: Understanding radiation effects in SRAM-based field programmable gate arrays for implementing instrumentation and control systems of nuclear power plants - ScienceDirect

Dual vs Triple Modular Redundancy



- Dual Modular Redundancy
- Error Detection



- Triple Modular Redundancy
- Error Detection & Correction

Ref: Safe-Guarding Logic, Registers, Clock Routing, IP, and I/O's Using TMR (2015)

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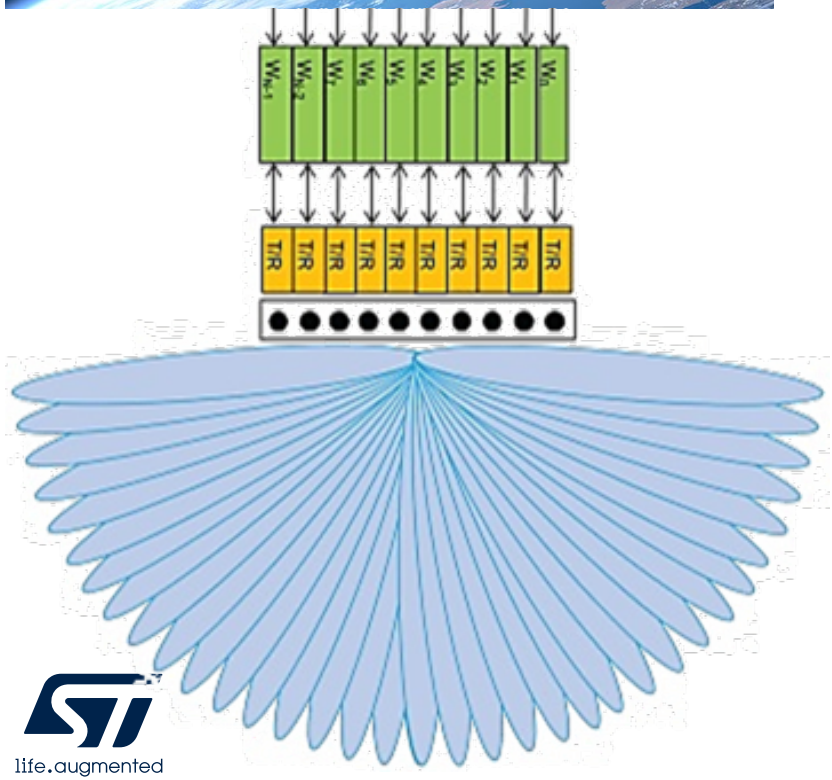
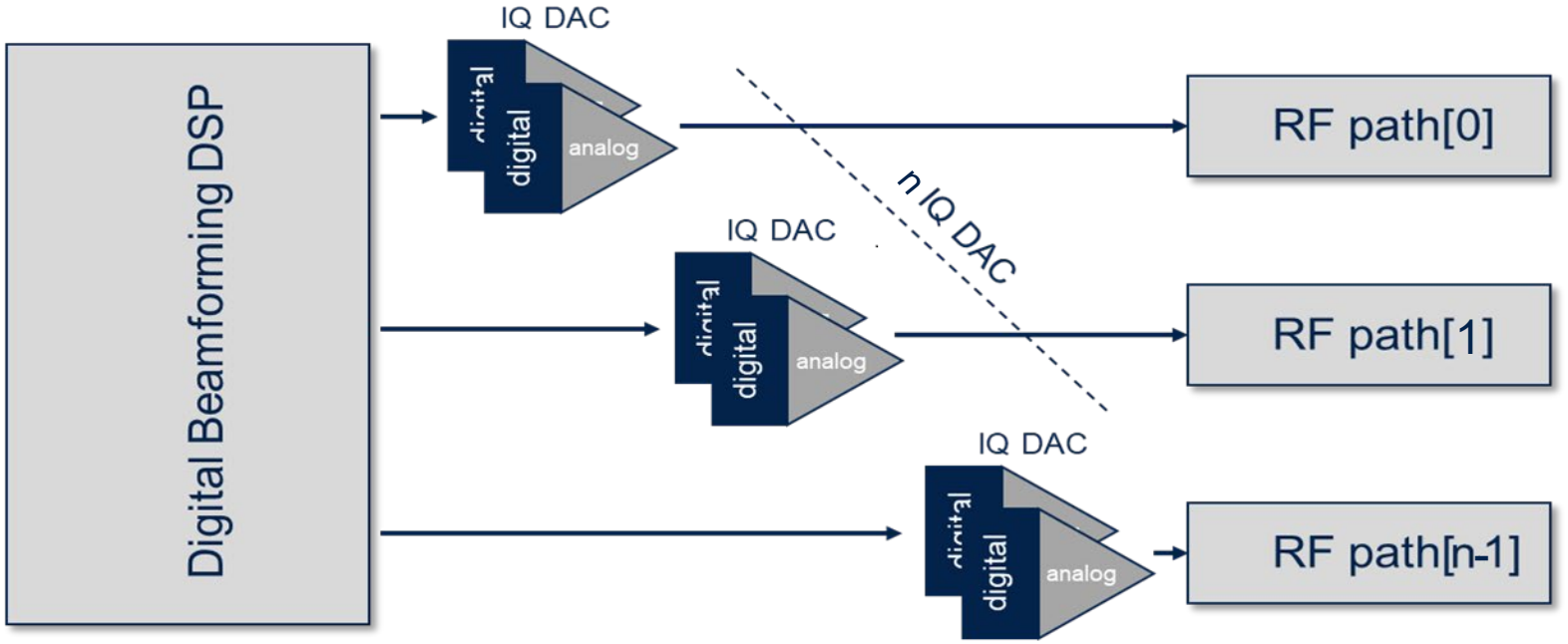
Critical space application: Digital Beam Forming (DBF)





- Mission critical RF application
- GHz Speed control and data paths
- Exposure to high cosmic radiation
- Continuous data sync mandatory

IQ = In-phase/Quadrature

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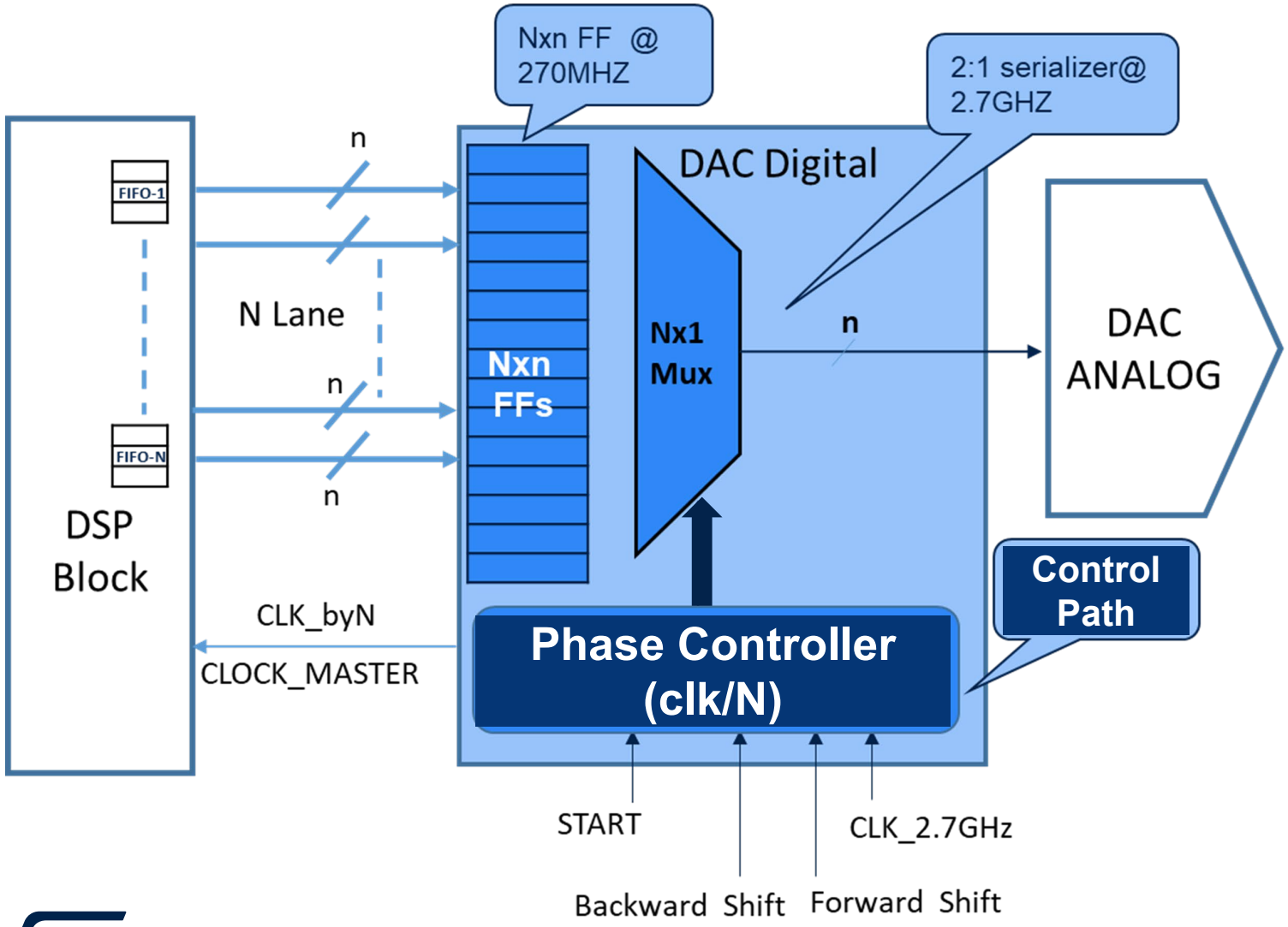
Critical space application: DBF circuit



- 2.7 GHz Serializer
- Phase Controller runs at divide by N clock
- Fault in Divider
  - ➔ Controller failure
  - ➔ System Failure
- Need for an error resilient divider
- Low Power requirements

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Error resilient high-speed phase-divider

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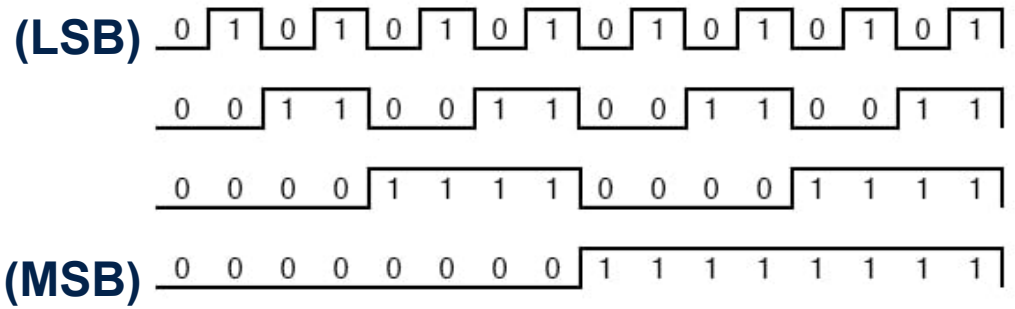
Error resilient high-speed phase-divider (1/4)

Divider partitioning into LSB & MSB counters

- Ring counter: N registers for N unique index values
- Ring not scalable for higher divisions
- Binary/Grey counter: N registers for 2^N index values
- Recommend two partitions
- Greater than 2 partitions cause excess latency



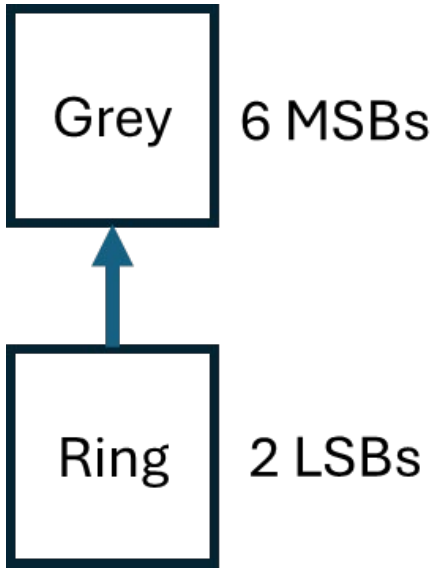
FAST
LSB Ring Counter

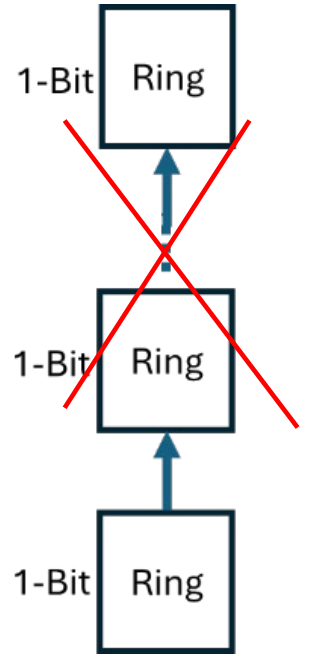
→

SLOWER
MSB Grey Counter

Low Power

→





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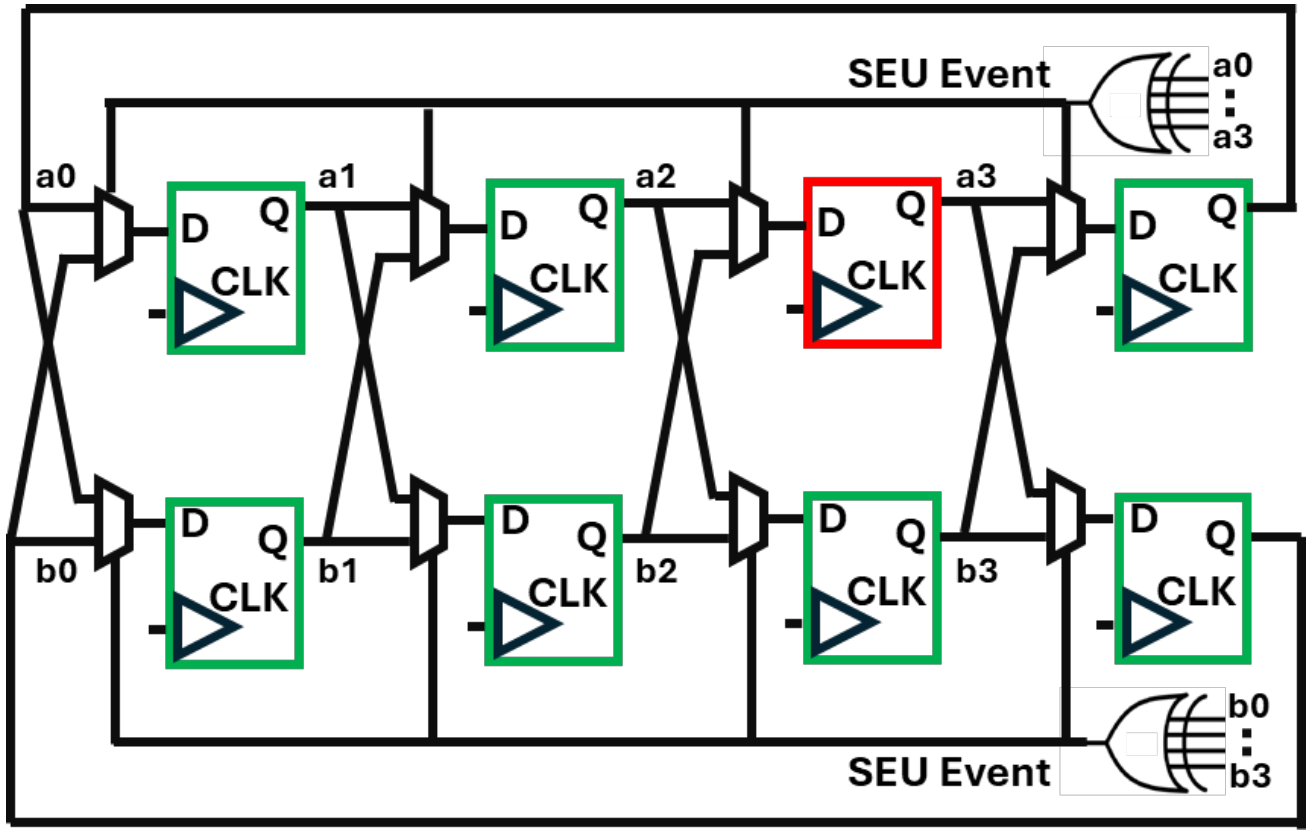
Error resilient high-speed phase-divider (2/4)



Divide by 4 example

- Ring Counter @ 2.7GHz
- Recoverable DMR (Dual Modular Redundancy) architecture
- SEU Event
  - ➔ Fault in Divider
  - ➔ Parity failure
  - ➔ Counter recovery
- Low critical path
- Minimal area & power tradeoffs

Index	a3	a2	a1	a0
1	0	0	0	1
2	0	0	1	0
4	0	1	0	0
8	1	0	0	0

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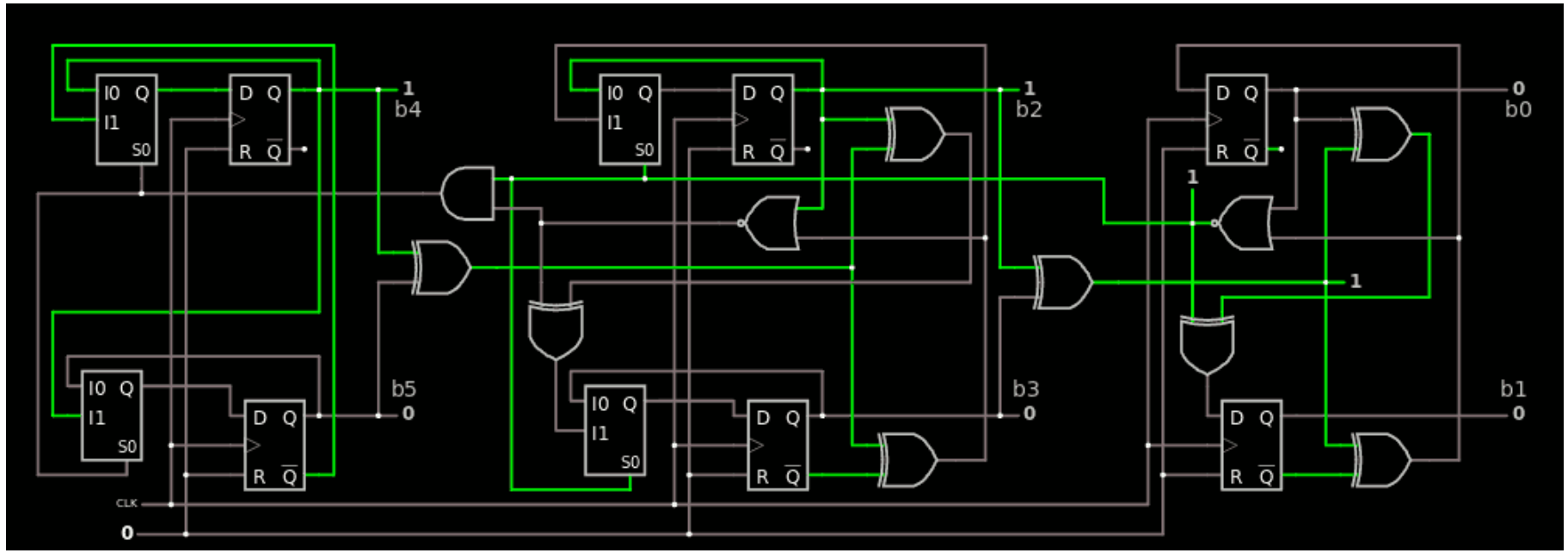
Error resilient high-speed phase-divider (3/4)

A 6-bit Grey counter



Index	6b GC
0	000000
1	000001
2	000011
3	000010
4	000110
5	000111
6	000101
7	000100

- Synchronous Grey counter
- Critical path is 5 XOR gates
- 2^6 sequential index values

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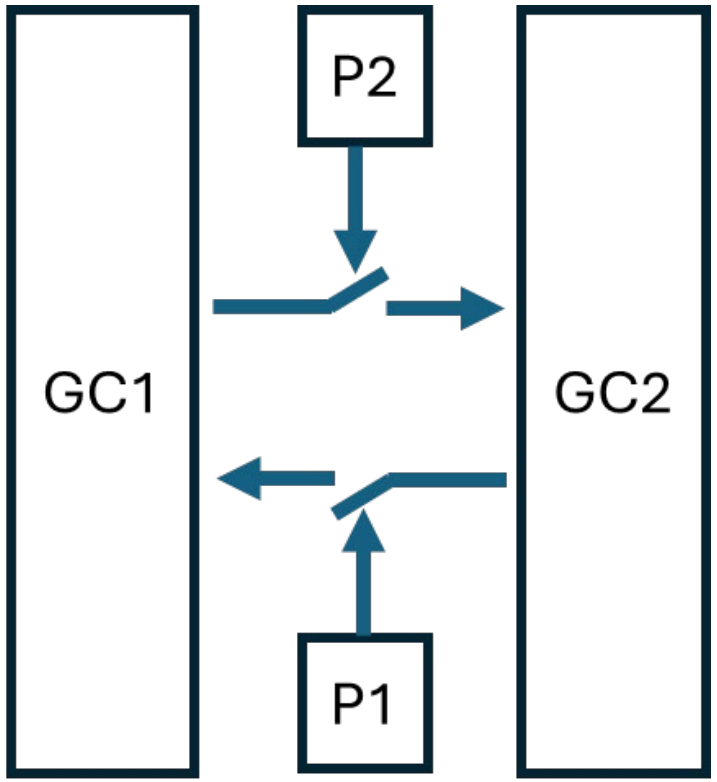
Error resilient high-speed phase-divider (4/4)

Index	6b GC	Parity
0	000000	0
1	000001	1
2	000011	0
3	000010	1
4	000110	0
5	000111	1
6	000101	0
7	000100	1



DMR Grey counter

- MSB low speed section
- Dual lock step grey counters
- Parity monitoring
- Parity fault drives state transfer
- Low power index generation
- SEU resilient real time operation

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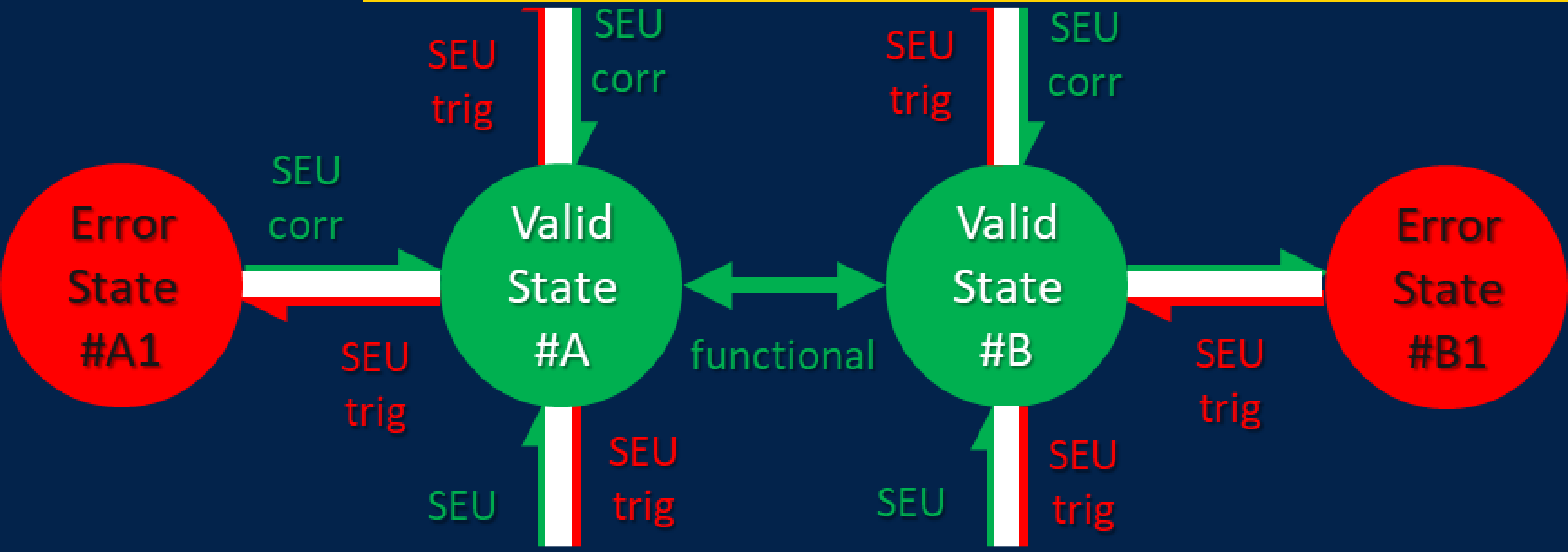
Error resilient state machine



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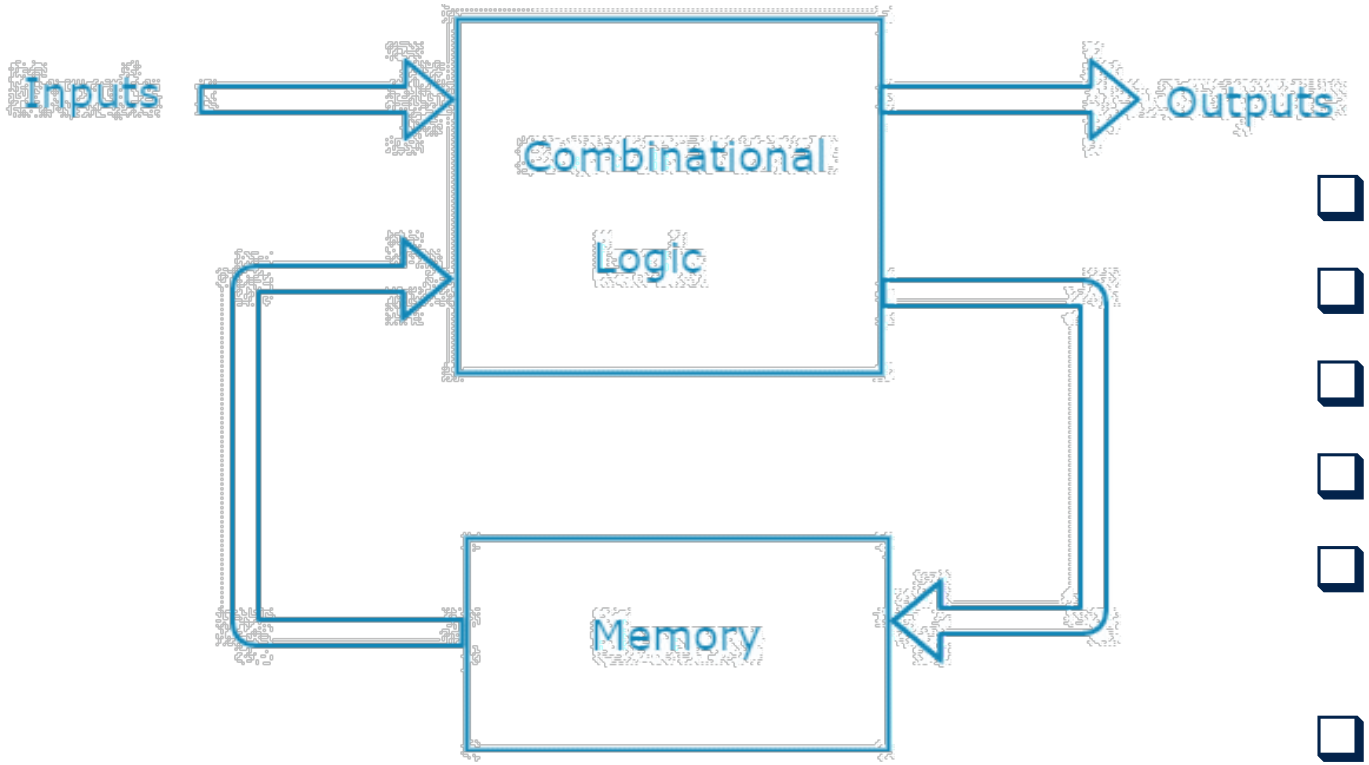
Digital state machines

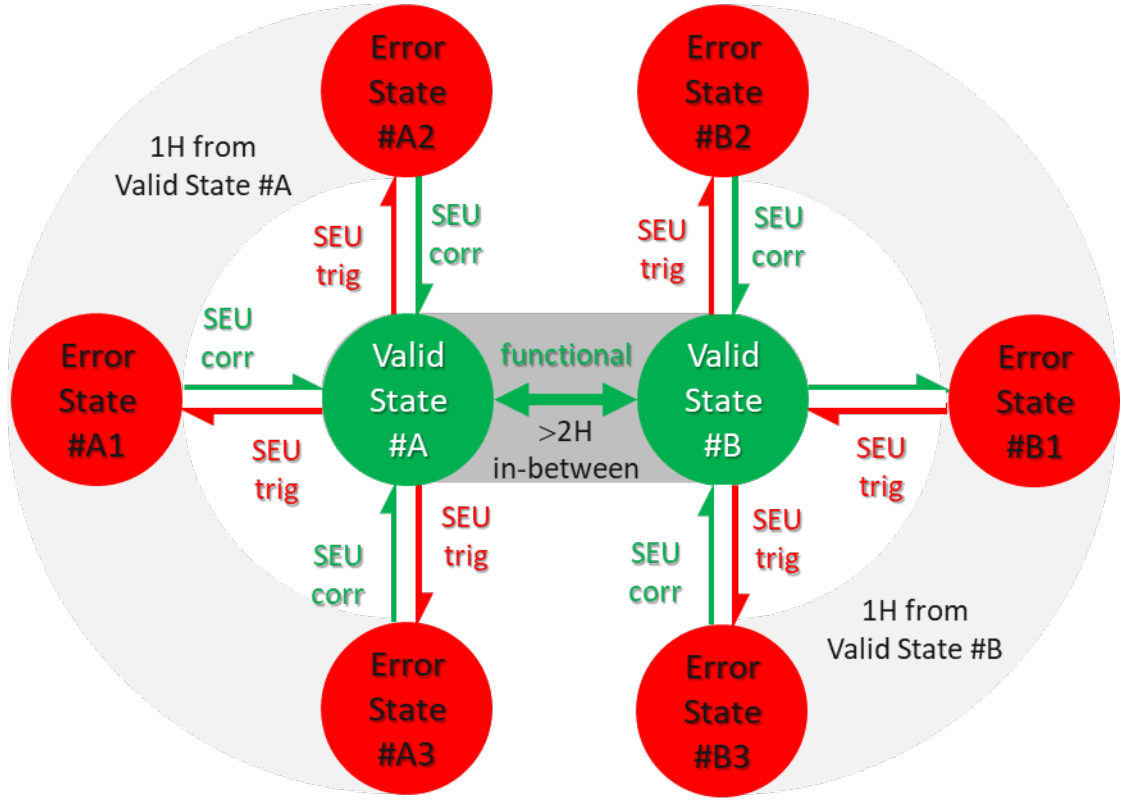


- Order of states not fixed
- Valid and invalid transitions defined
- Even a minute variation catastrophic
- Feedback mechanism traps errors
- ECC (Error Correcting Codes) adds overhead
- DMR/TMR large overheads

Example of an 8 states machine resilience

State	Binary	One-Hot	H-2	H-3
S0	000	00000001	0000	000000
S1	001	00000010	0011	000111
S2	010	00000100	0101	011001
S3	011	00001000	0110	011110
S4	100	00010000	1001	101010
S5	101	00100000	1010	101101
S6	110	01000000	1100	110011
S7	111	10000000	1111	110100

Area	🙂	☹	🙂	🙂
Speed	🙂	🙂	🙂	🙂
Detection (D)	☹	🙂	🙂	🙂
Correction (C)	☹	☹	☹	🙂
Resilience (D+C)	☹	◐	◐	🙂



H = Hamming distance = number of bits changed between two states

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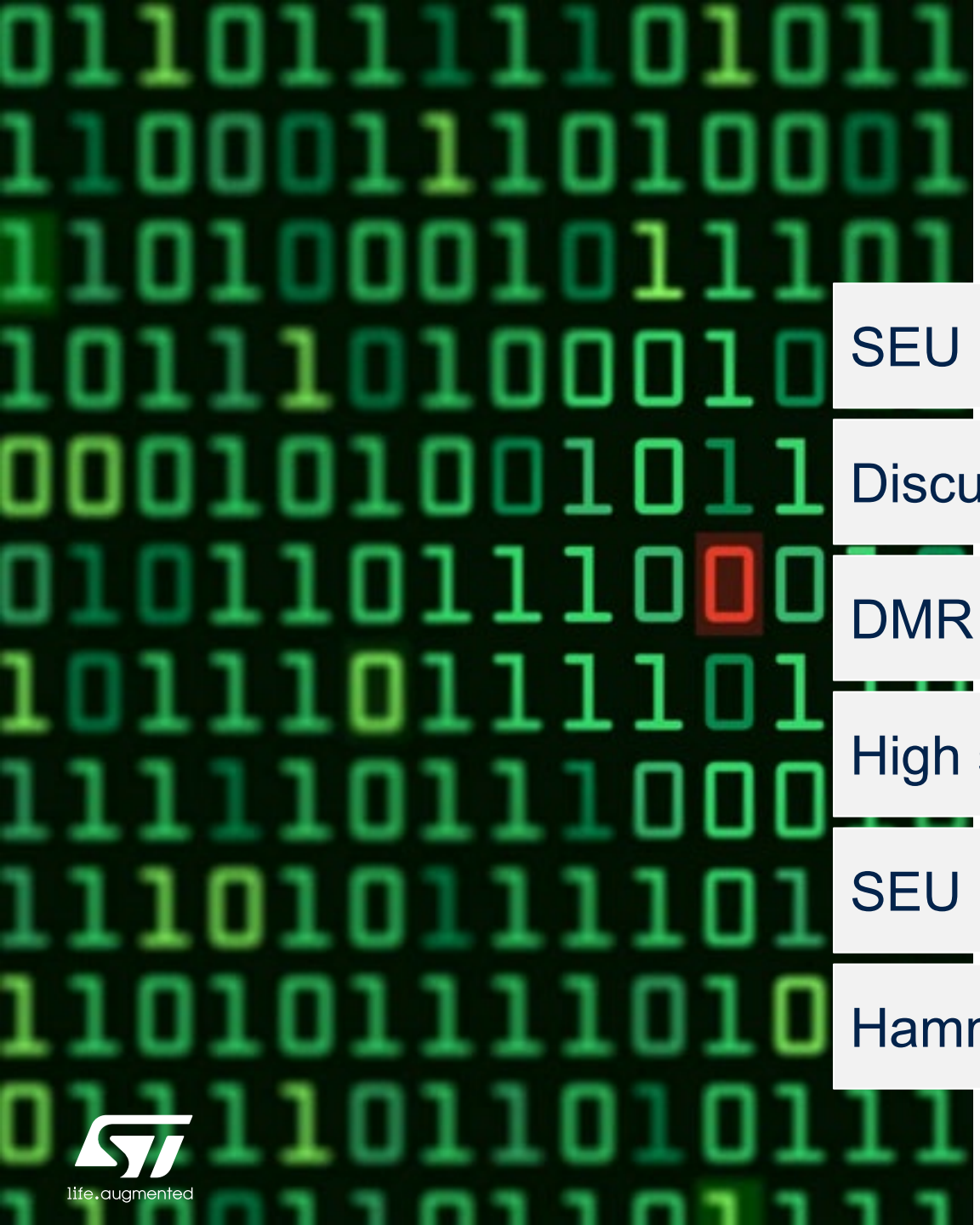

Takeaways

- SEU impact critical for control path circuits
- Discussed methods to mitigate SEU
- DMR in index generators for SEU immunity
- High speed dividers by deploying multistage DMR
- SEU impact on state machines
- Hamming-3 coded states best for SEU immunity

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Thank you

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