Low power architectures for clock domain crossing in SoC design

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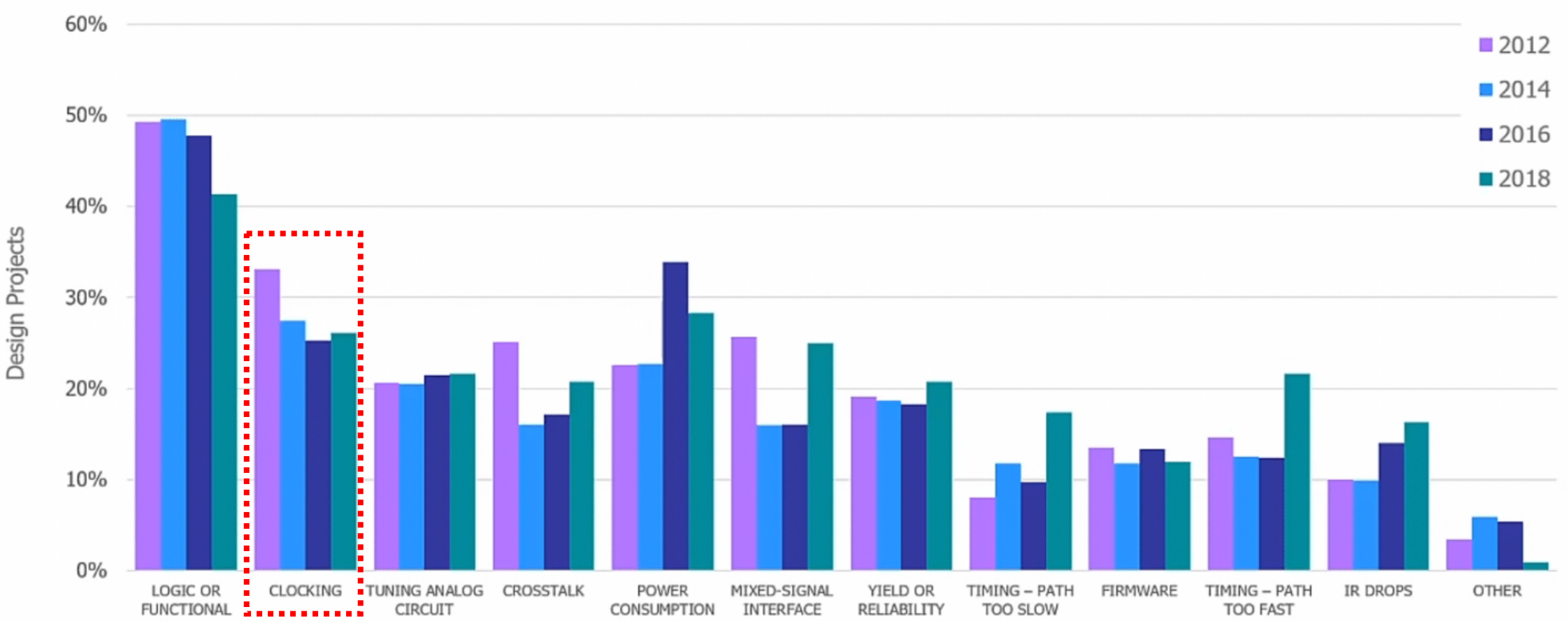
Agenda

1. Motivation & background
2. Synchronous FIFO
3. Control Path Synchronizer
4. Reset synchronizer
5. Key takeaways

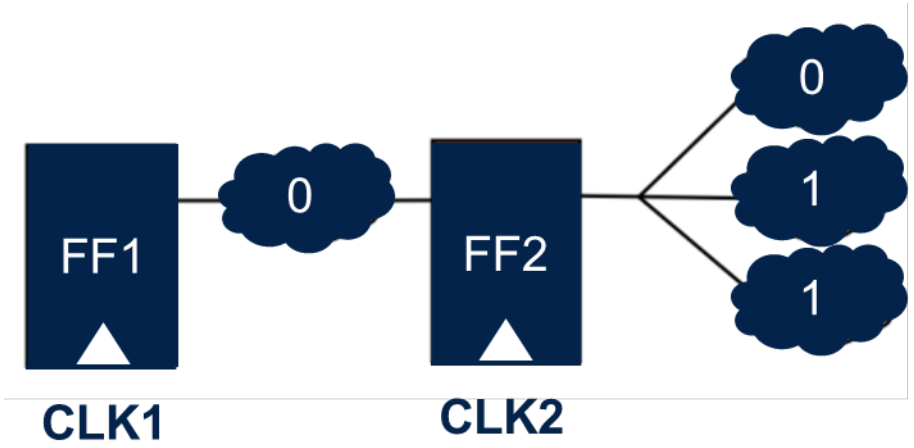
Sources of chip failure

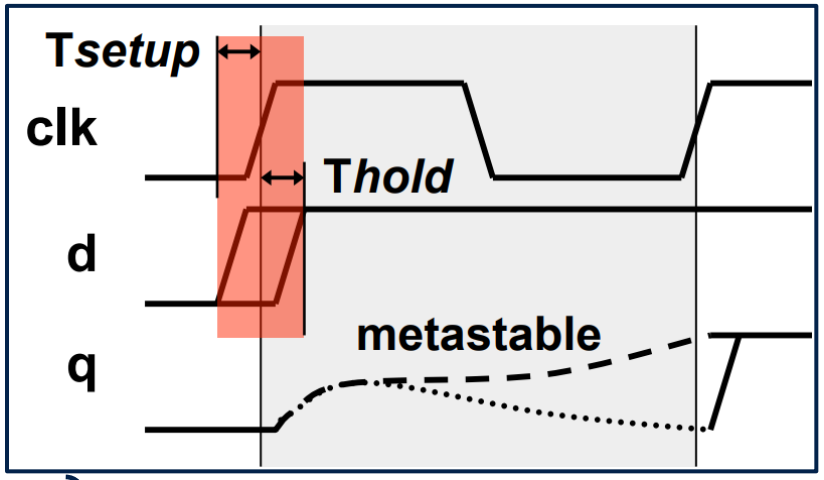


CDC issues are a primary cause of chip failure

Reference: Why Chips Die (semiengineering.com)

Clock Domain Crossing: metastability & MTBF





$$MTBF = \frac{e^{Ts/Tc}}{T_w F_c F_d}$$

Mean **T**ime **B**etween **F**ailures

- T_s = settling window
- T_c = settling time constant
- T_w = window of susceptibility

Technology & implementation

- F_c = clock frequency
- F_d = data update rate

Concept & application

MTBF quantifies the reliability of a system

Techniques & challenges in CDC management

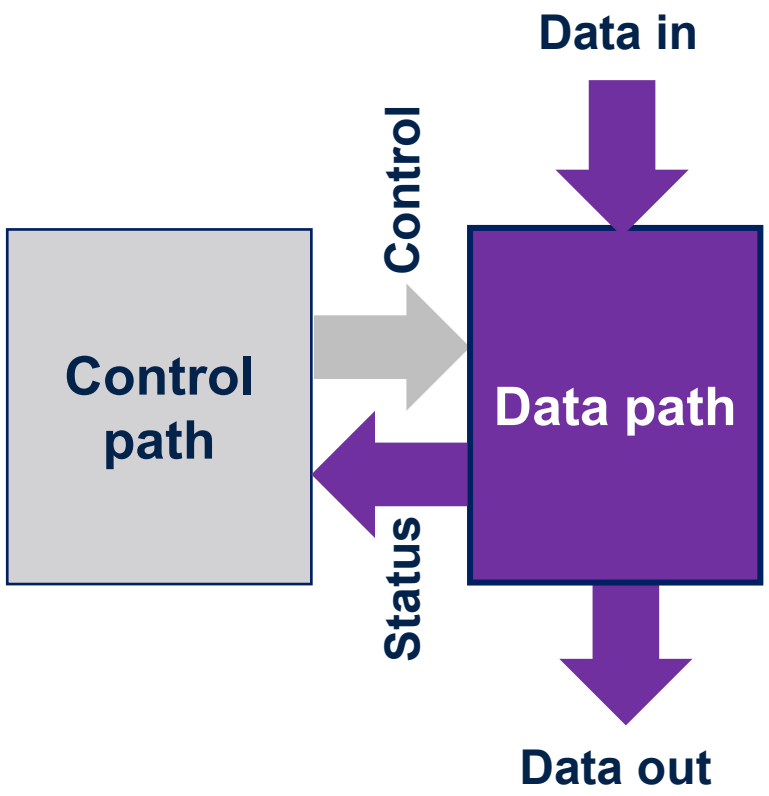
Control path

Common techniques

- Multi-flop synchronizers
- Pulse stretching and detection
- Gray-coded counters for status flags

Challenges:

- Metastability
- Glitch-free signaling
- Safe reset synchronization



Data path

Common techniques:

- FIFOs
- Dual-port RAM
- Handshake-based protocols

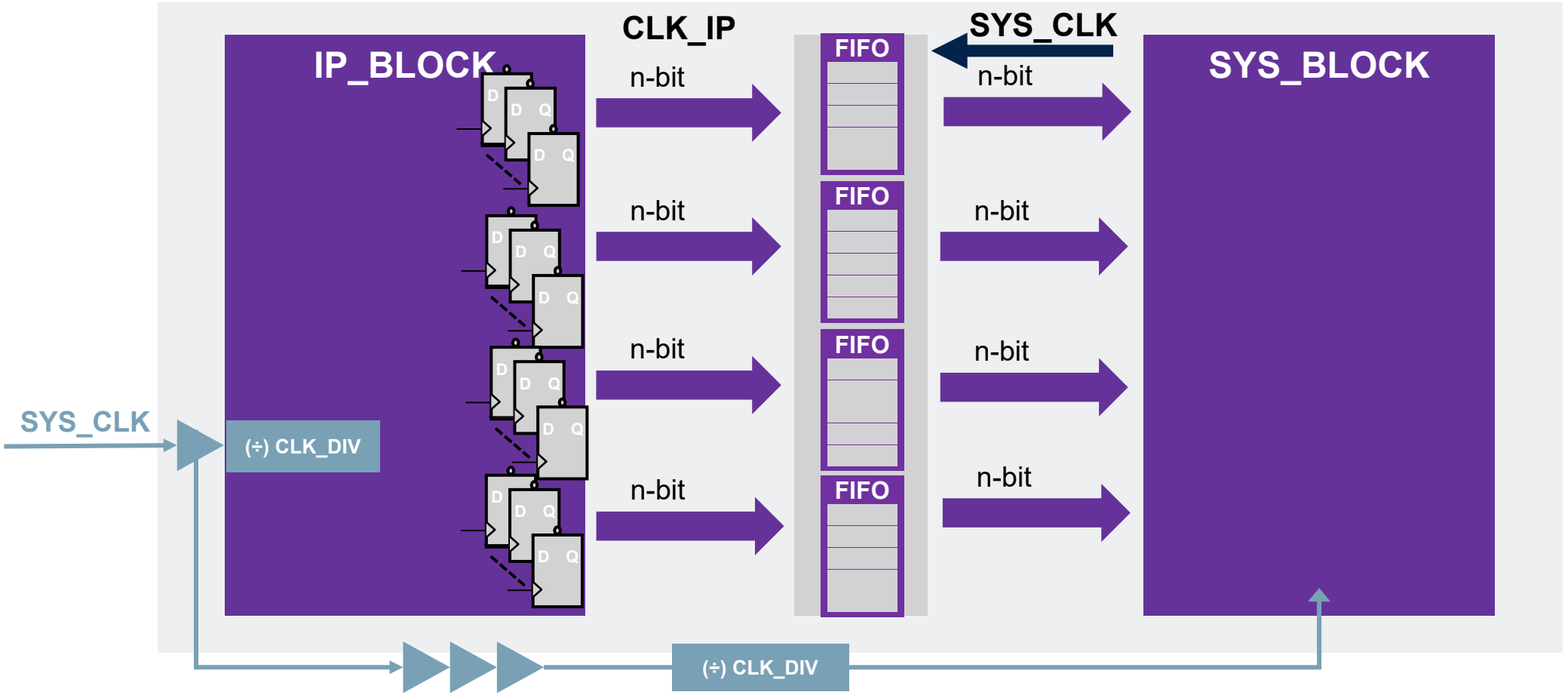
Challenges:

- Data integrity
- Latency
- Throughput

Need for low latency, low power CDC architectures

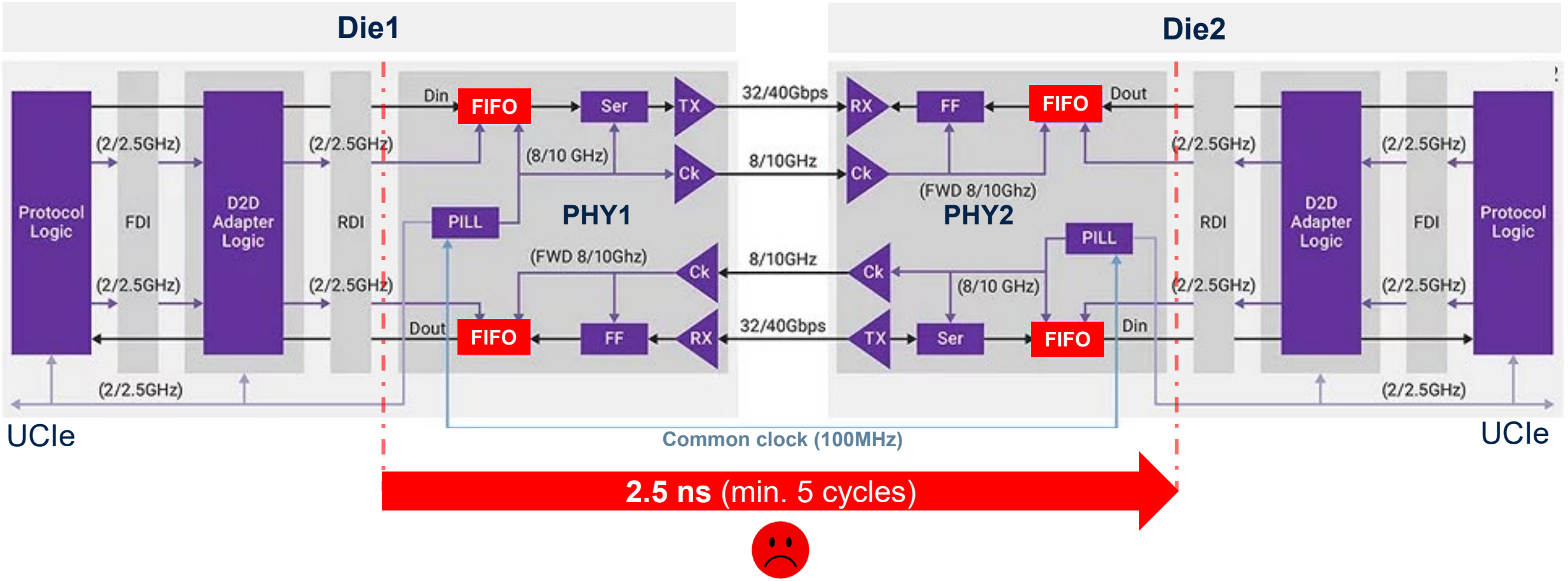
Synchronous FIFO

FIFO in a monolithic SoC connectivity



Trade-offs in area, power, latency for reliable data path CDC

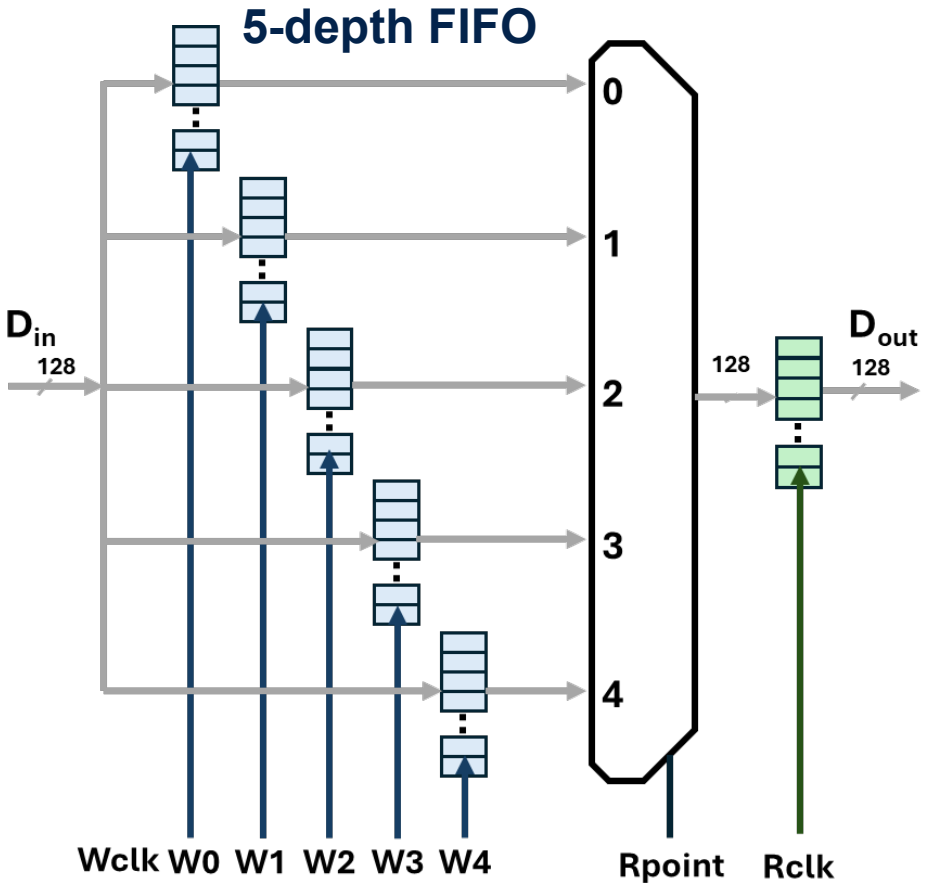
FIFO in die-to-die connectivity

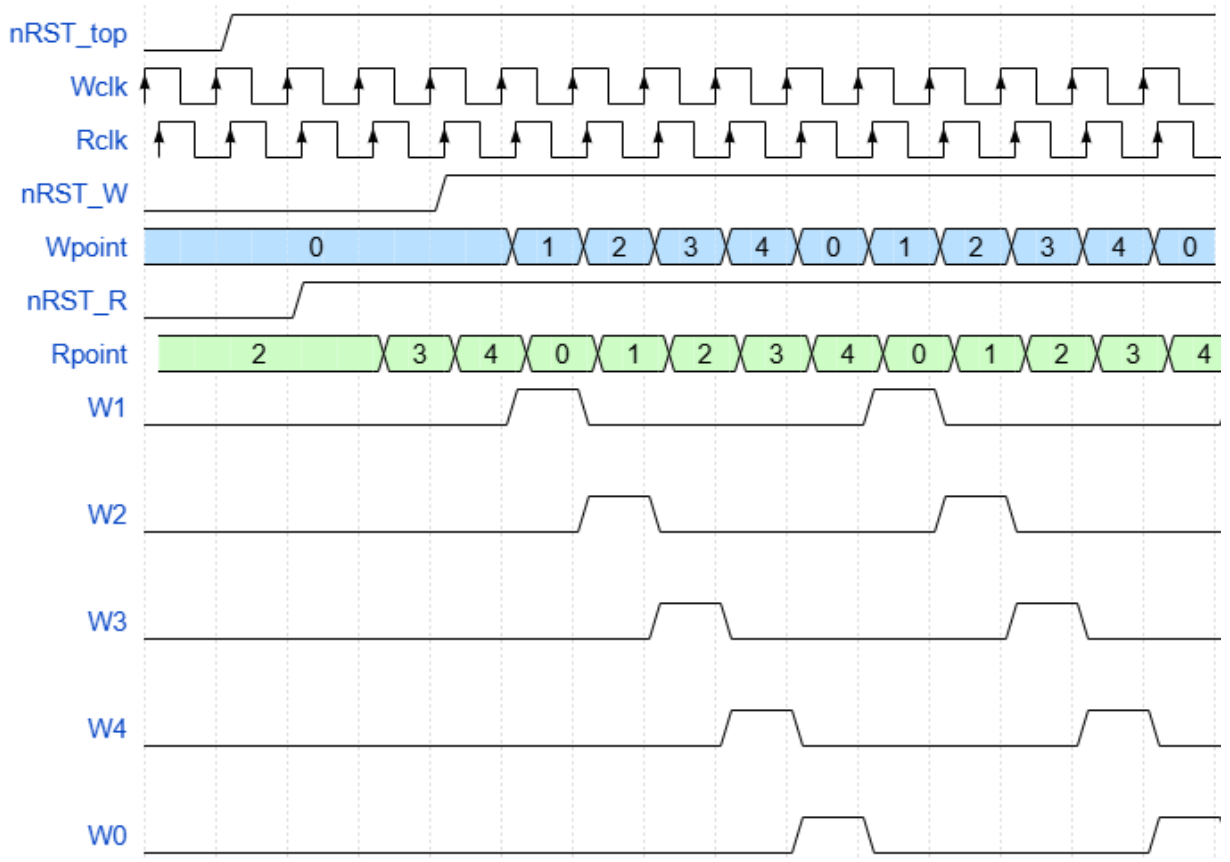


Major challenge in FIFO to overcome latency!

Ref: https://zhuanlan.zhihu.com/p/17350321598

Synchronous FIFO implementation

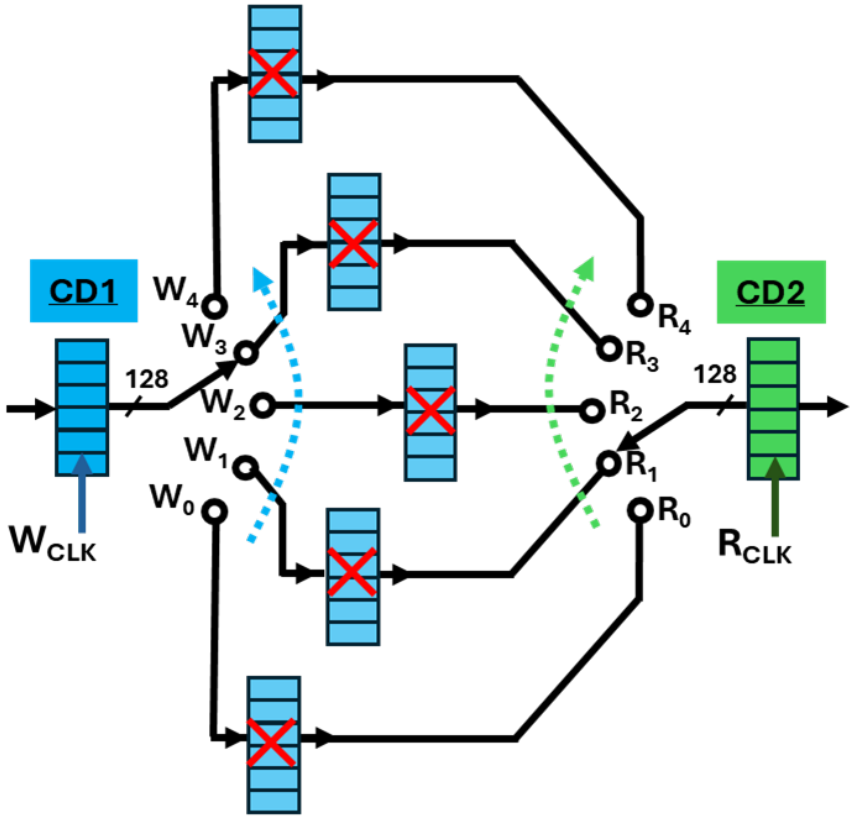




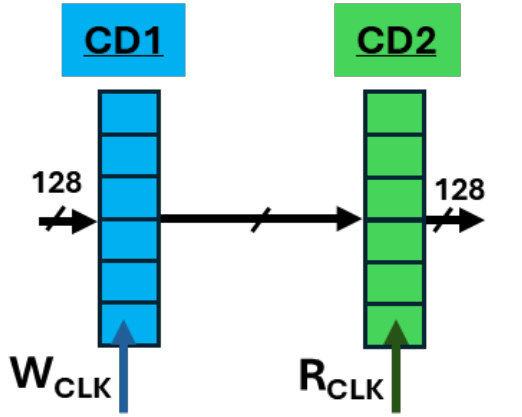
Data latency: **2–4 clock cycles** (best to worst case)

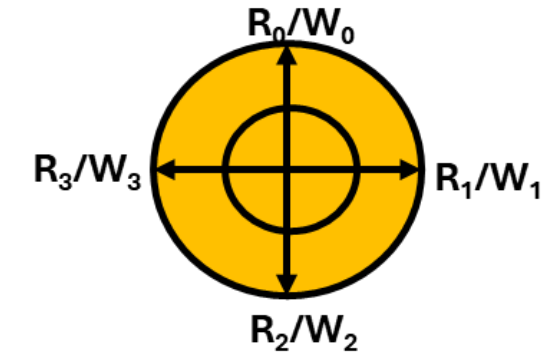
Proposed architecture

Standard synchronous FIFO



Proposed synchronous FIFO

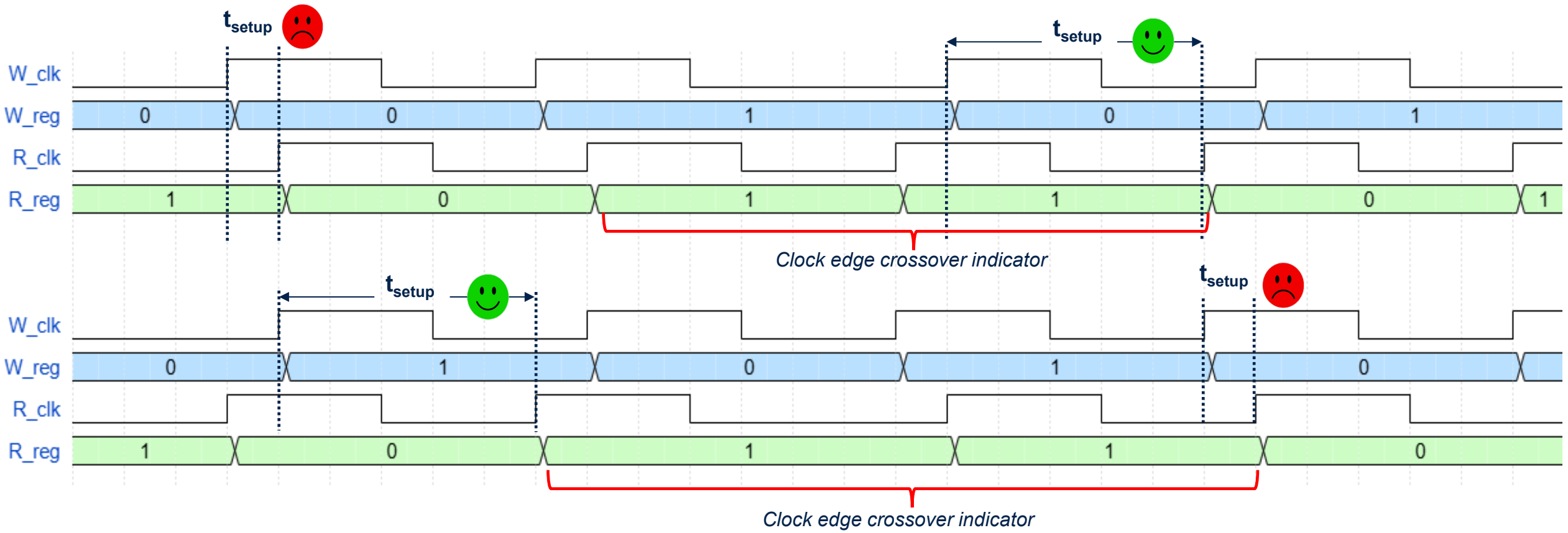




R/W clock phase select

Calibrate for maximum phase margin

Clock phase selection



Maximize the setup timing between launch & capture clocks

Key results & advantages

5-Depth FIFO characteristics	Contemporary solutions	Proposed innovation
Write clock 250MHz	768 FFs	**128 FFs**
NAND gates	1536	**256**
Read clock 1GHz	128 FFs	128 FFs
Latency (UI)	3.25	**1.25**
DFT Flip Flops	896	**256**

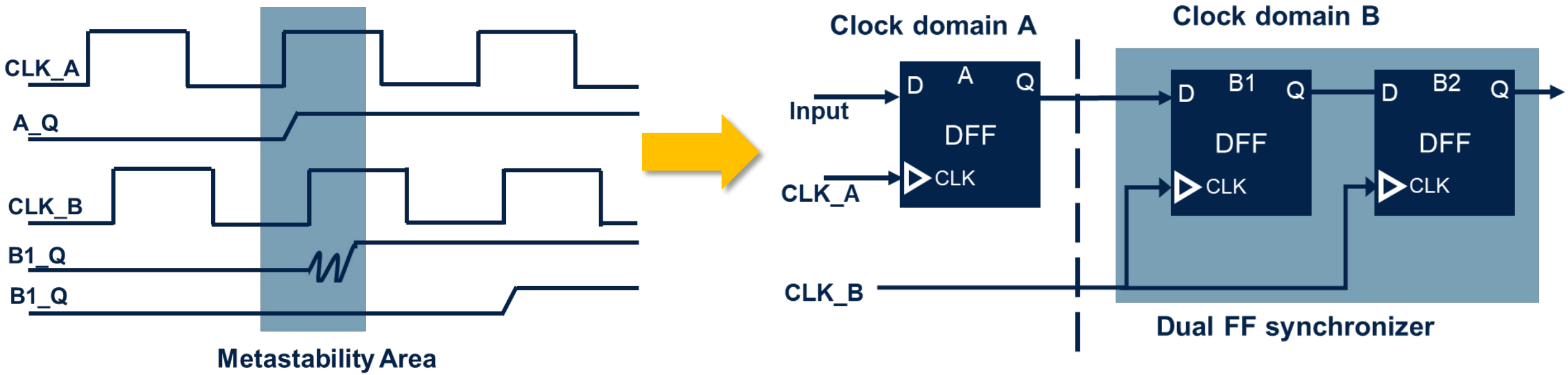
Plug & play replacement

Zero tradeoffs

Lower data-transfer latency, drastic reduction in area & power

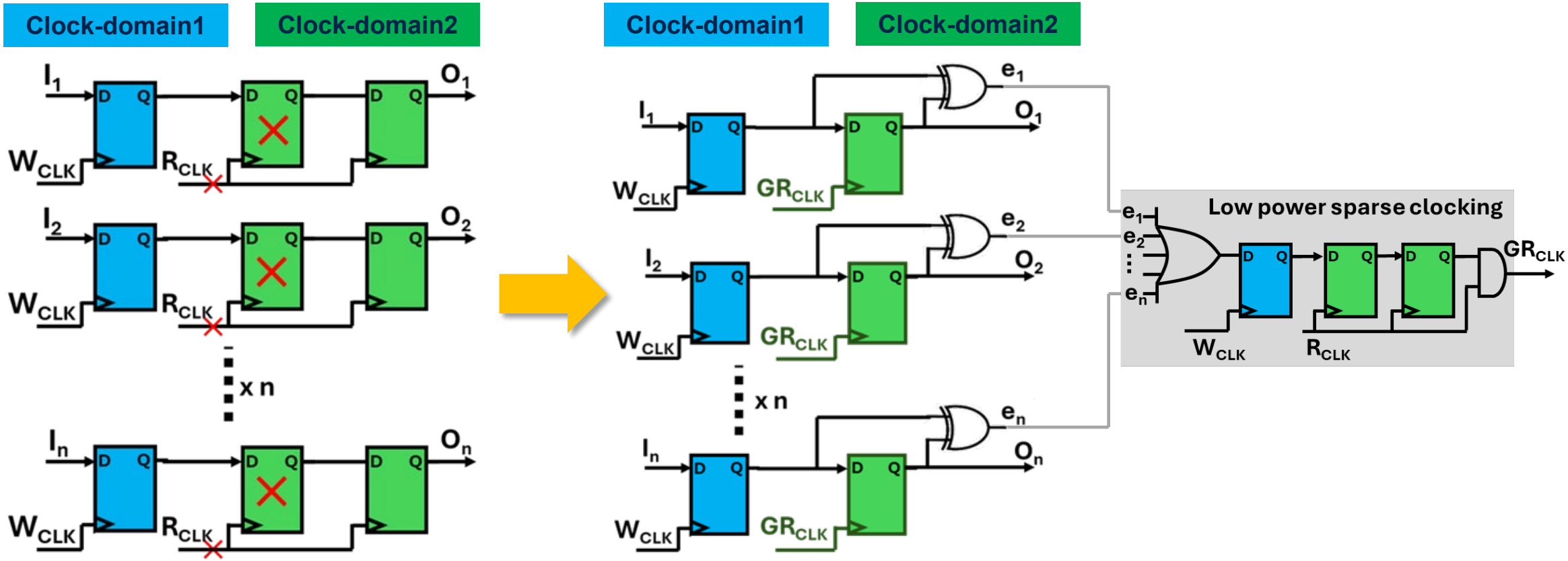
Control Path Synchronizer

Conventional control path synchronizer



Continuous clock toggling leads to dynamic power consumption

Clock-gated synchronizer architecture



Clocking of destination FFs triggered only on signal transitions

Key results & advantages

8 x 2-stage Sync. @600MHz	Contemporary (µW)	Proposed (µW)	Gain
10% data toggle	39	22	**41%**
1% data toggle	30	8	**72%**

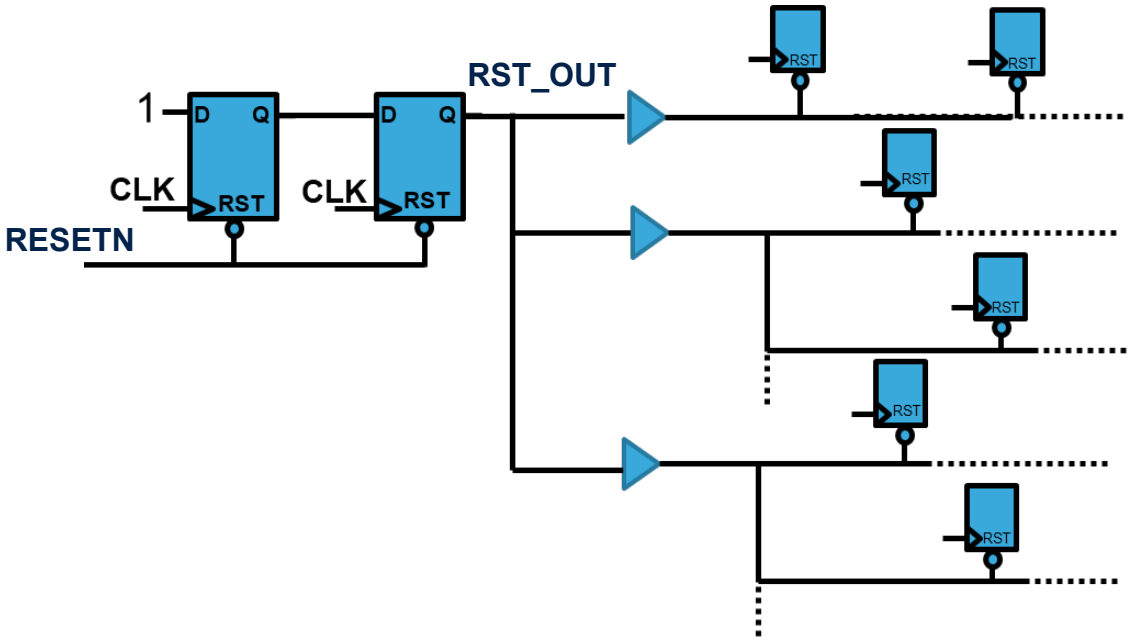
Over 30% area reduction

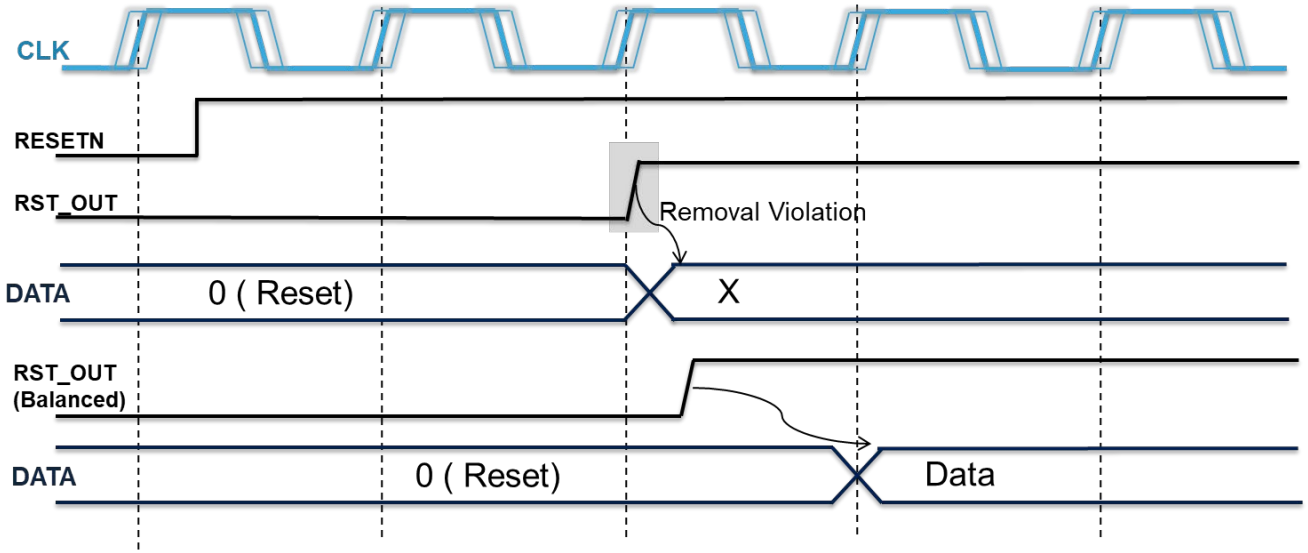
Scriptable insertion in RTL

Exceptional power efficiency during sparse signal toggling

Reset synchronizer

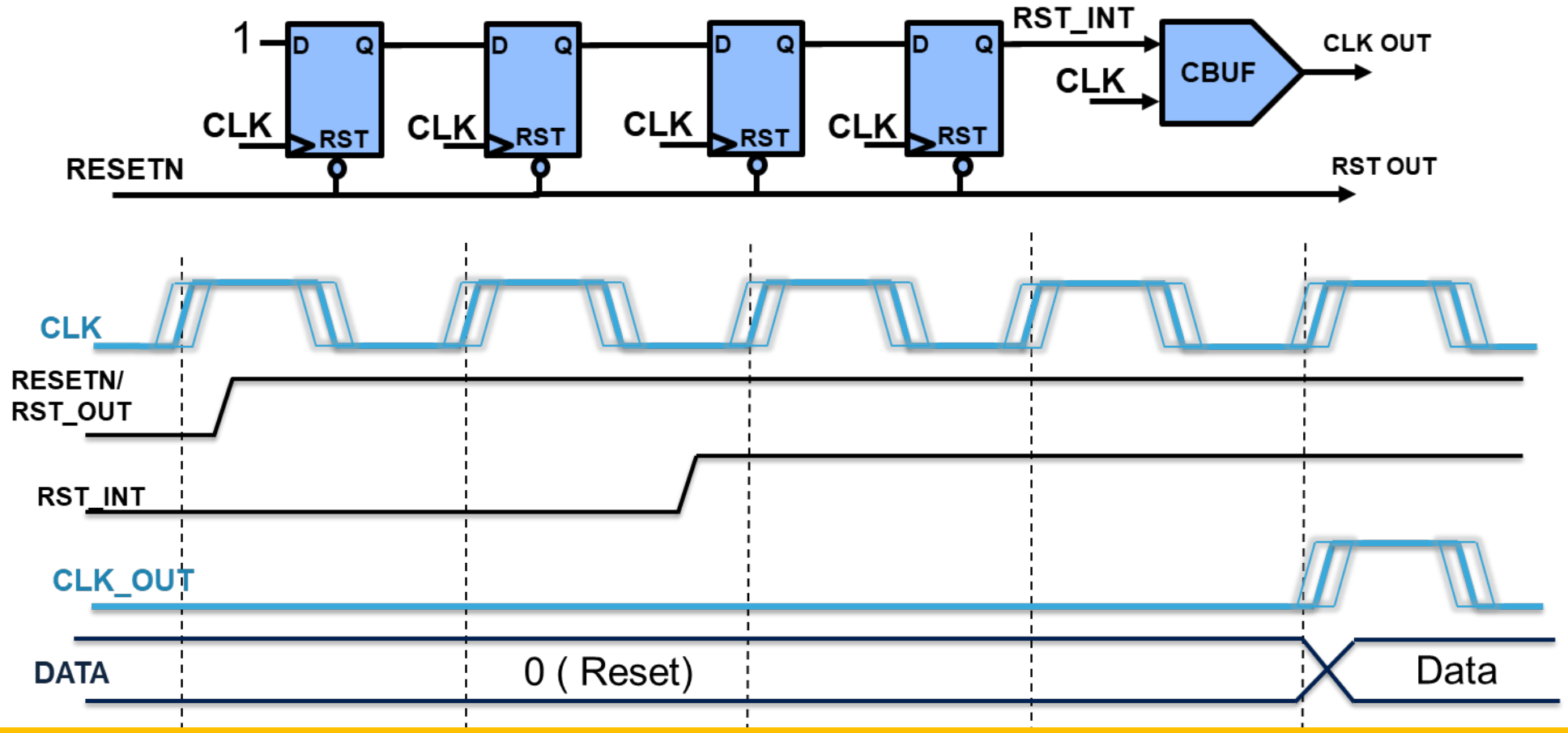
Contemporary reset synchronizer





Reset de-assertion timing closure is a persistent challenge

Proposed clock gated reset synchronizer



Proposed architecture trivializes global reset timing

Key results & advantages

Reset Recovery Violation			
Frequency	WNS (nS)	TNS (nS)	No. of paths
4 GHz	-0.4758	-1.9773	6
2.4 GHz	-0.6702	-936.1055	**3427**
Reset Removal Violation			
Frequency	WNS (nS)	TNS (nS)	No. of paths
4 GHz	-0.5964	-132.39	**379**

The bigger the design, the more the savings

Makes reset implementation easy in GHz speed designs

Applicable to all asynchronous reset types

An optimized architecture to alleviate reset tree timing criticality

Key takeaways

- Presented novel **low power** techniques
- Demonstrated significant **area & power savings**
- Proposed techniques with **minimal to zero trade-offs**
- **Deterministic optimizations** early in the design flow
- **Simplify** implementation and verification cycles
- **Stringent protocol latency** specifications feasible

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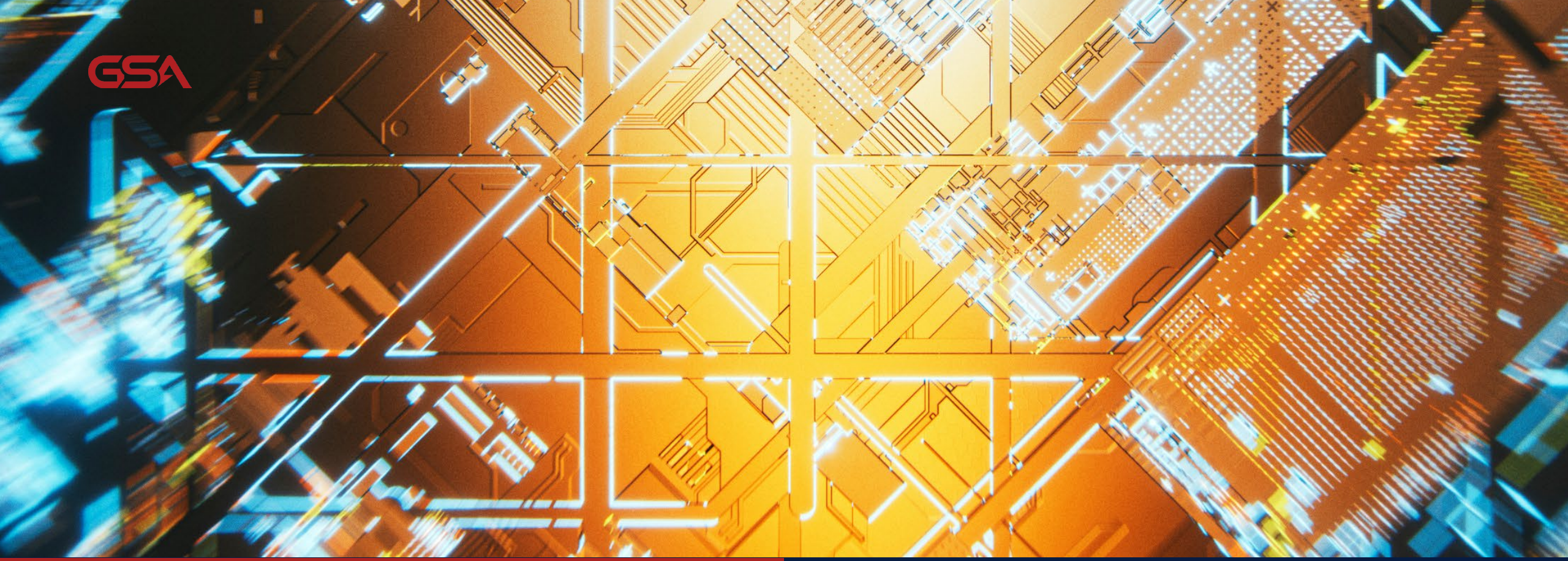
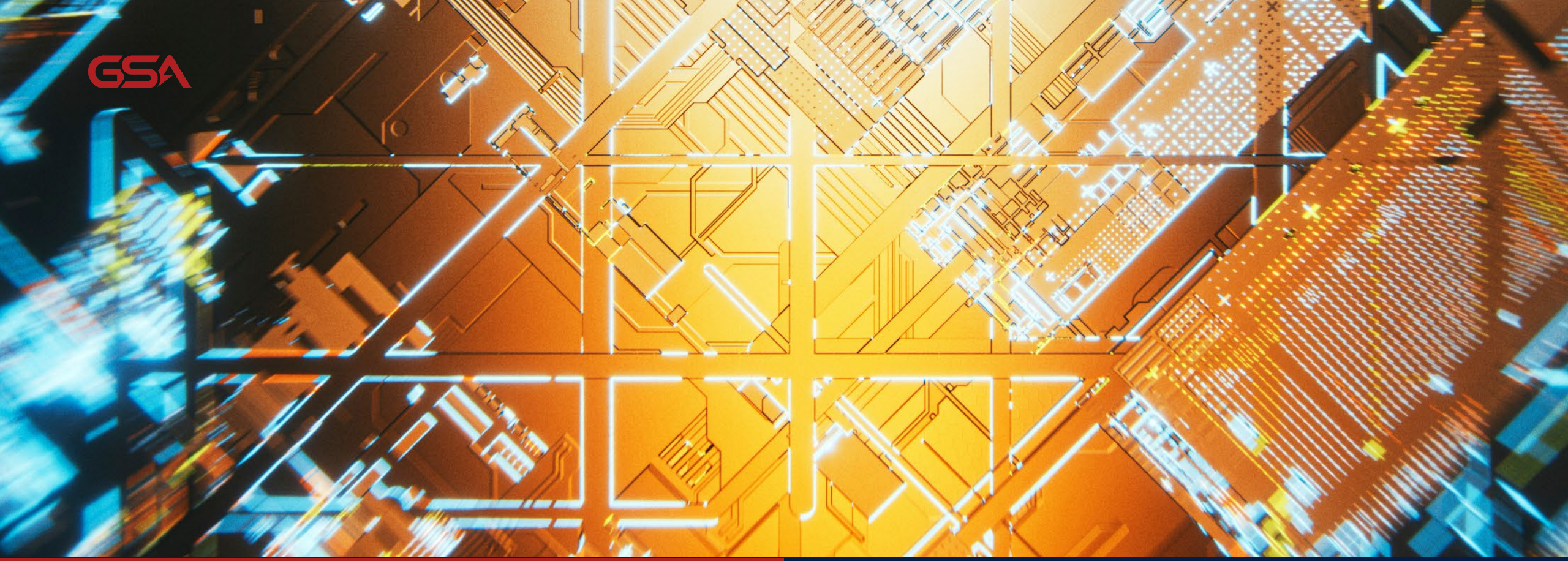


Transition Slide



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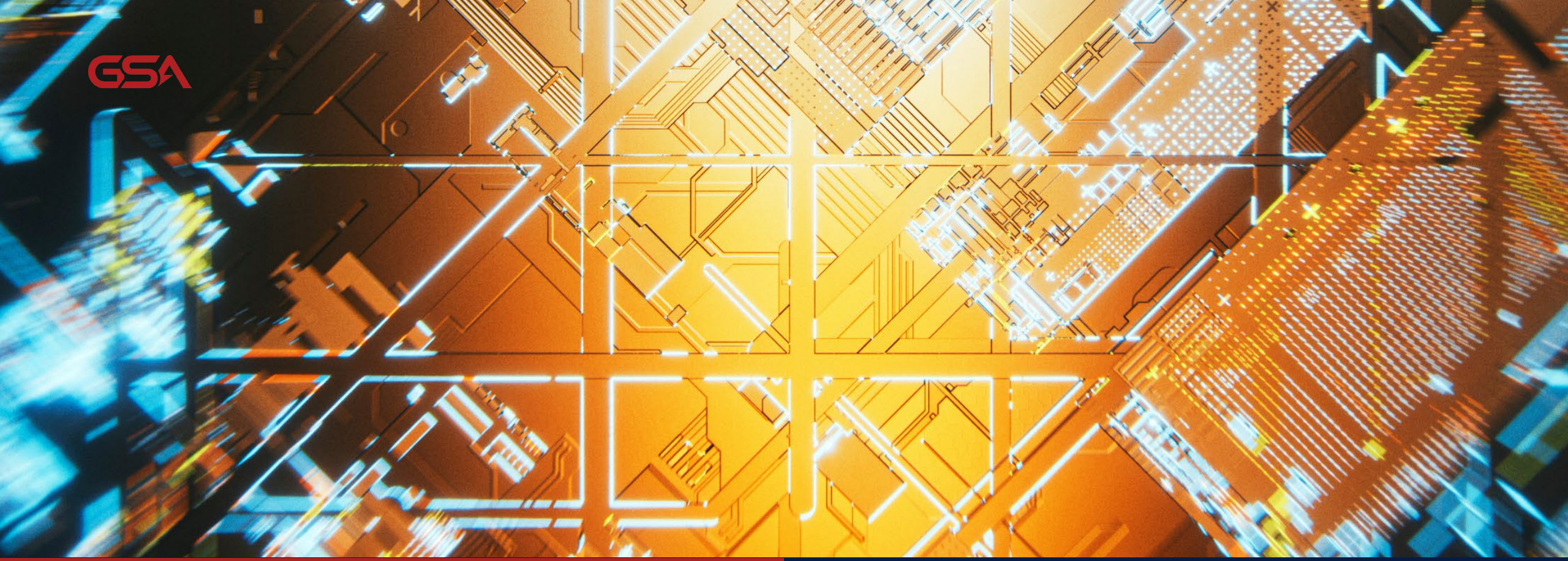

Transition Slide