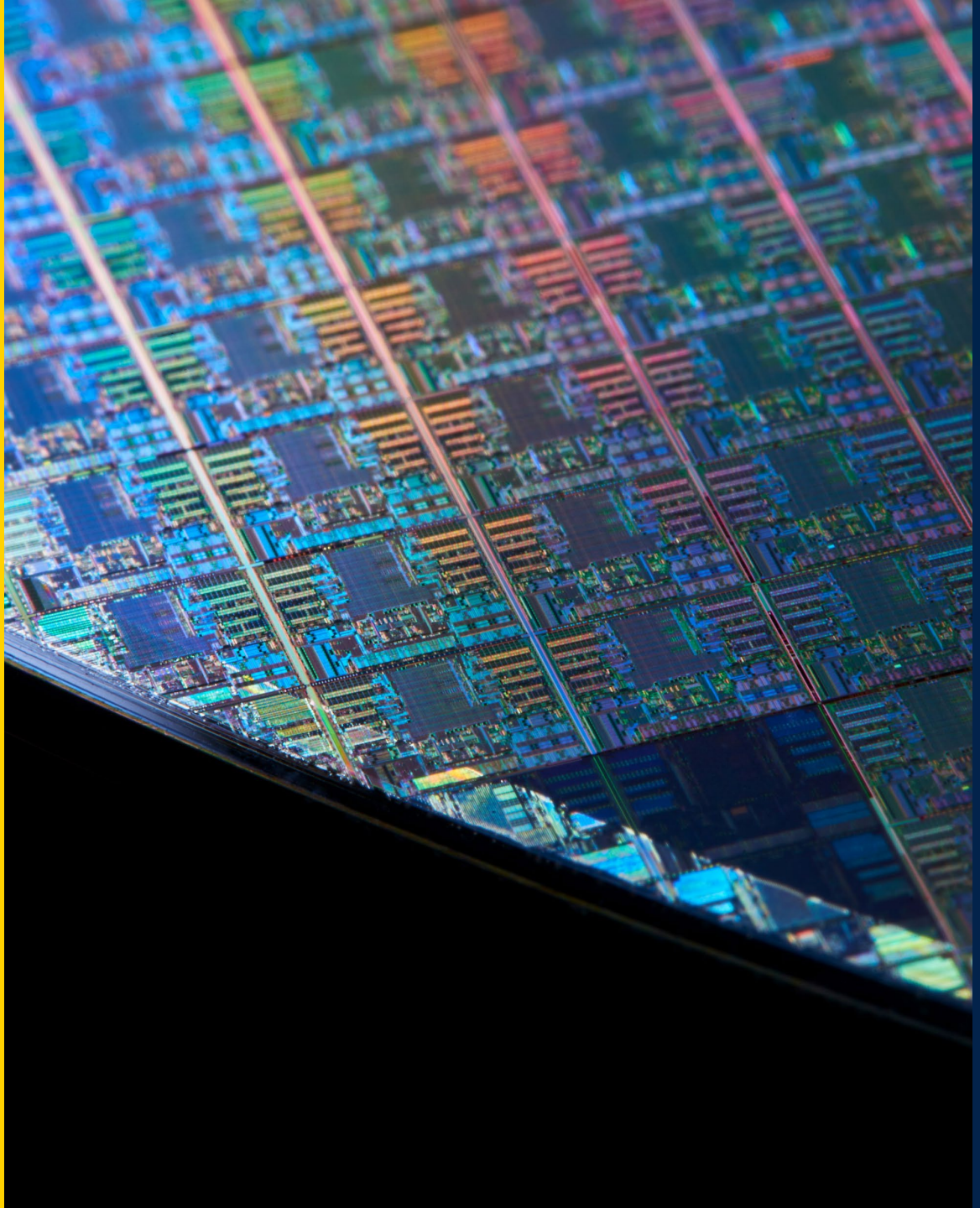

Optimizing ECO efficiency and precision:

An alternative approach for implementing digital-intensive RTL module restructuring through metal changes in IC design

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Agenda

1 Introduction

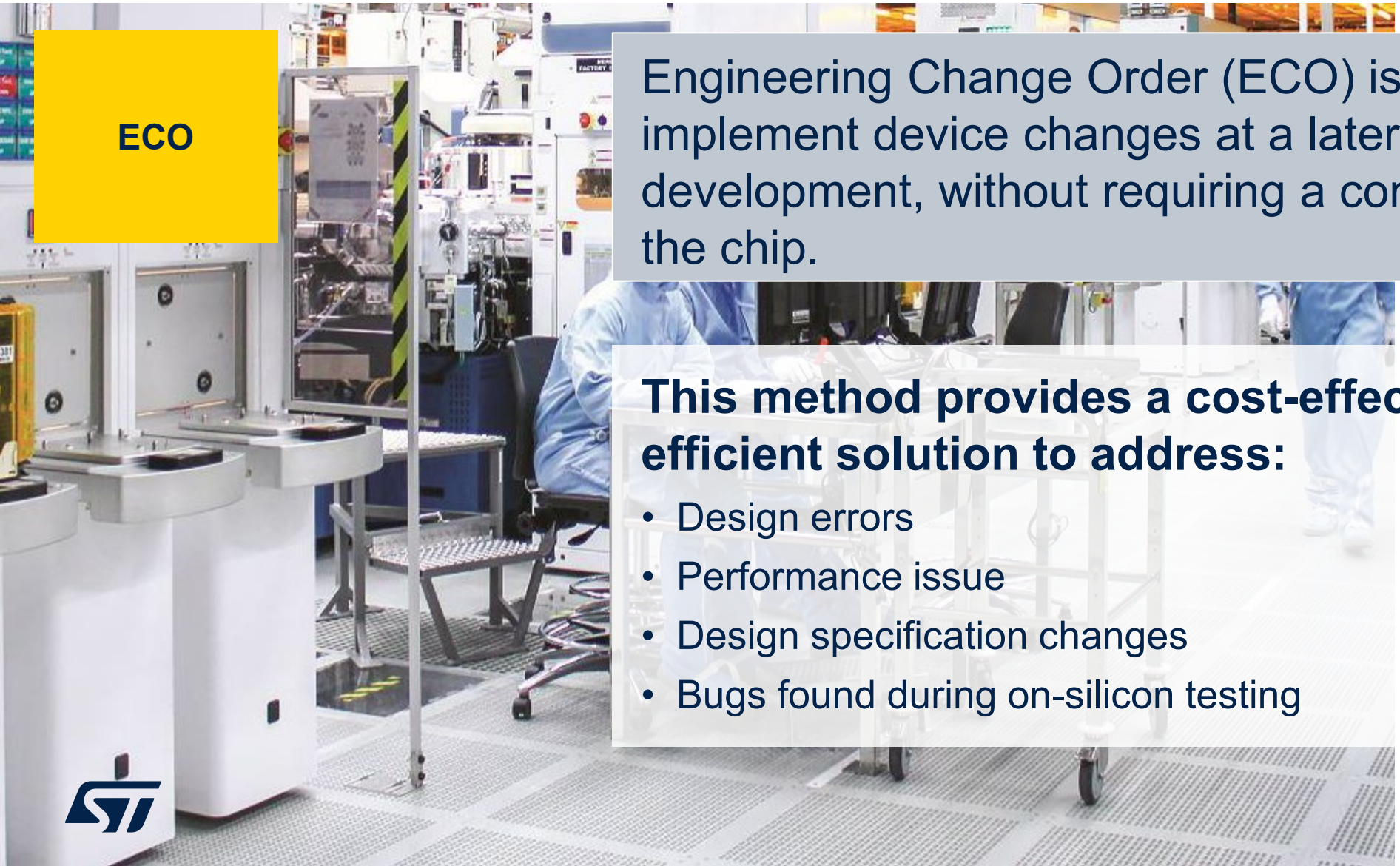
2 Standard ECO flow

3 Challenges

4 Proposed ECO flow

5 Conclusions

Engineering Change Order (ECO)



ECO

Engineering Change Order (ECO) is a process to implement device changes at a later stage of the development, without requiring a complete redesign of the chip.

This method provides a cost-effective and time-efficient solution to address:

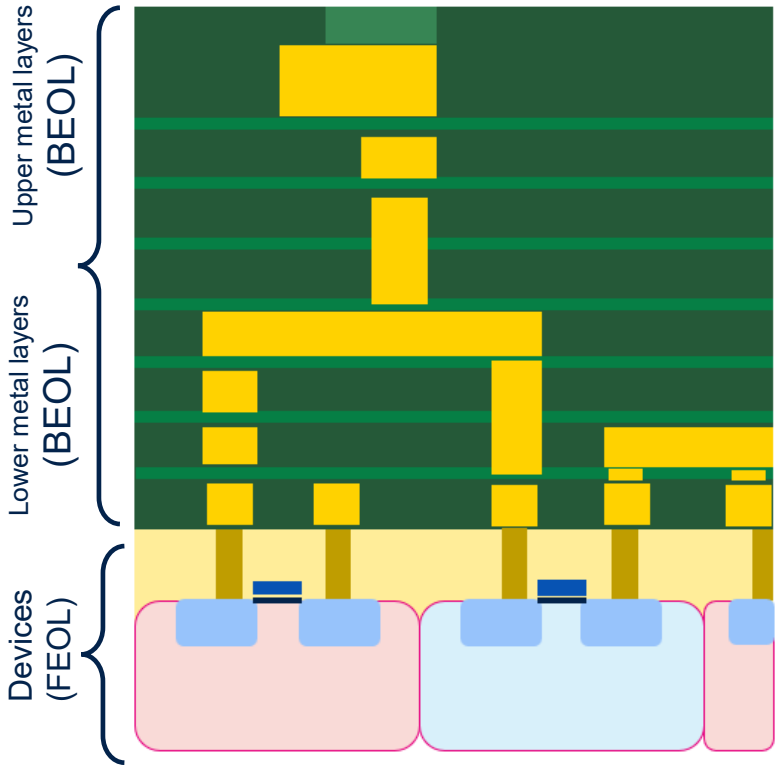
- Design errors
- Performance issue
- Design specification changes
- Bugs found during on-silicon testing

Types of ECOs

Full mask ECO
FEOL + BEOL

Needed for major design changes or partial redesigns requiring new logic gates.

- ☹ More expensive
- ☹ Higher time to market
- ☺ Suitable for complex changes
- ☺ New cells are added/deleted, no need for spare cells



Back end of line (BEOL)
Front end of line (FEOL)

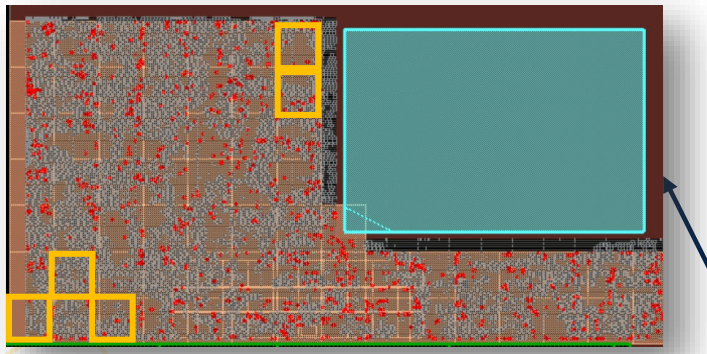
Metal mask ECO
BEOL only

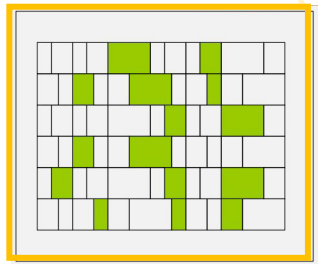
Ideal for minor fixes, reusing most existing design components and gates.

- ☺ Cost-effective
- ☺ Time saving
- ☹ Dependent on the complexity of design changes
- ☹ Limited by the availability of spare cells

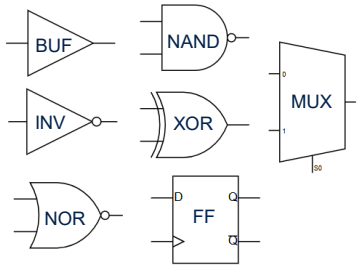
Metal mask ECO offers greater flexibility, reduces design and manufacturing timeline and cost and is the preferred choice, when feasible.

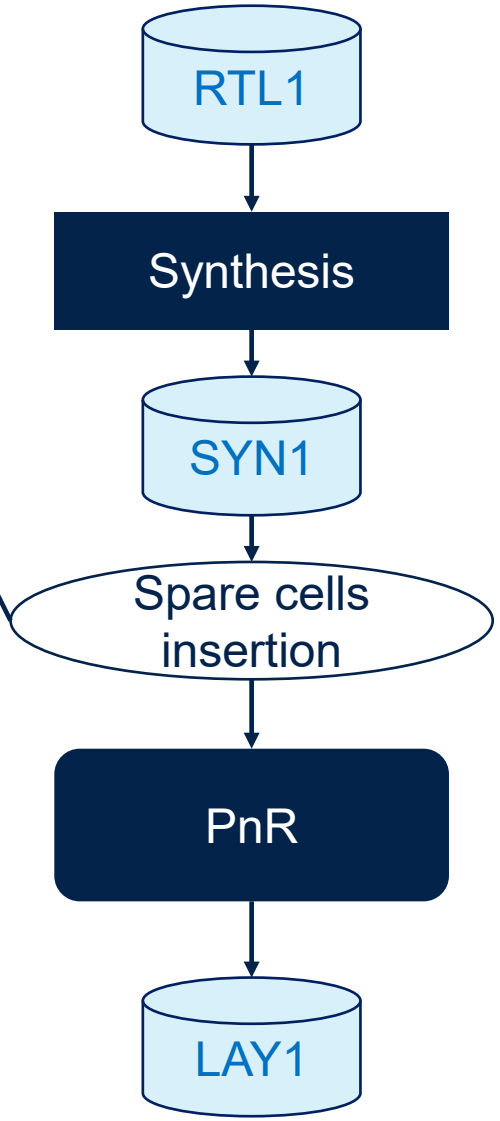
ECO flow – pre tape-out





Spare cell module



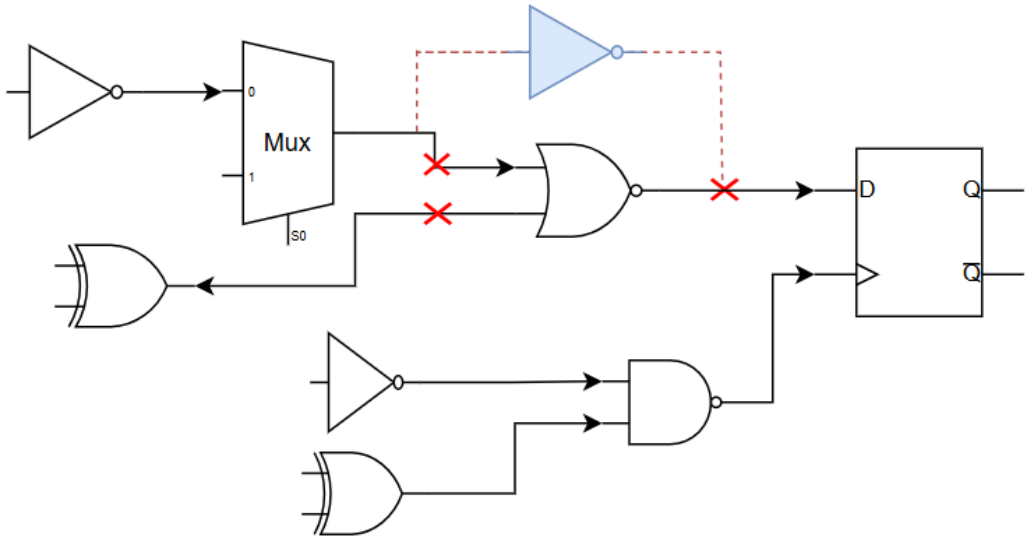


Spare cells are added during initial device implementation to support any future design changes after the tape-out.

- Topology is chosen between the most common cells of the design (NAND, NOR etc)
- Total number of spare is around 3-5% of total logic area
- Spare modules are evenly distributed inside the layout
- Inputs tied either VDD or VSS
- Outputs left floating

ECO flow – post tape-out (1/2)

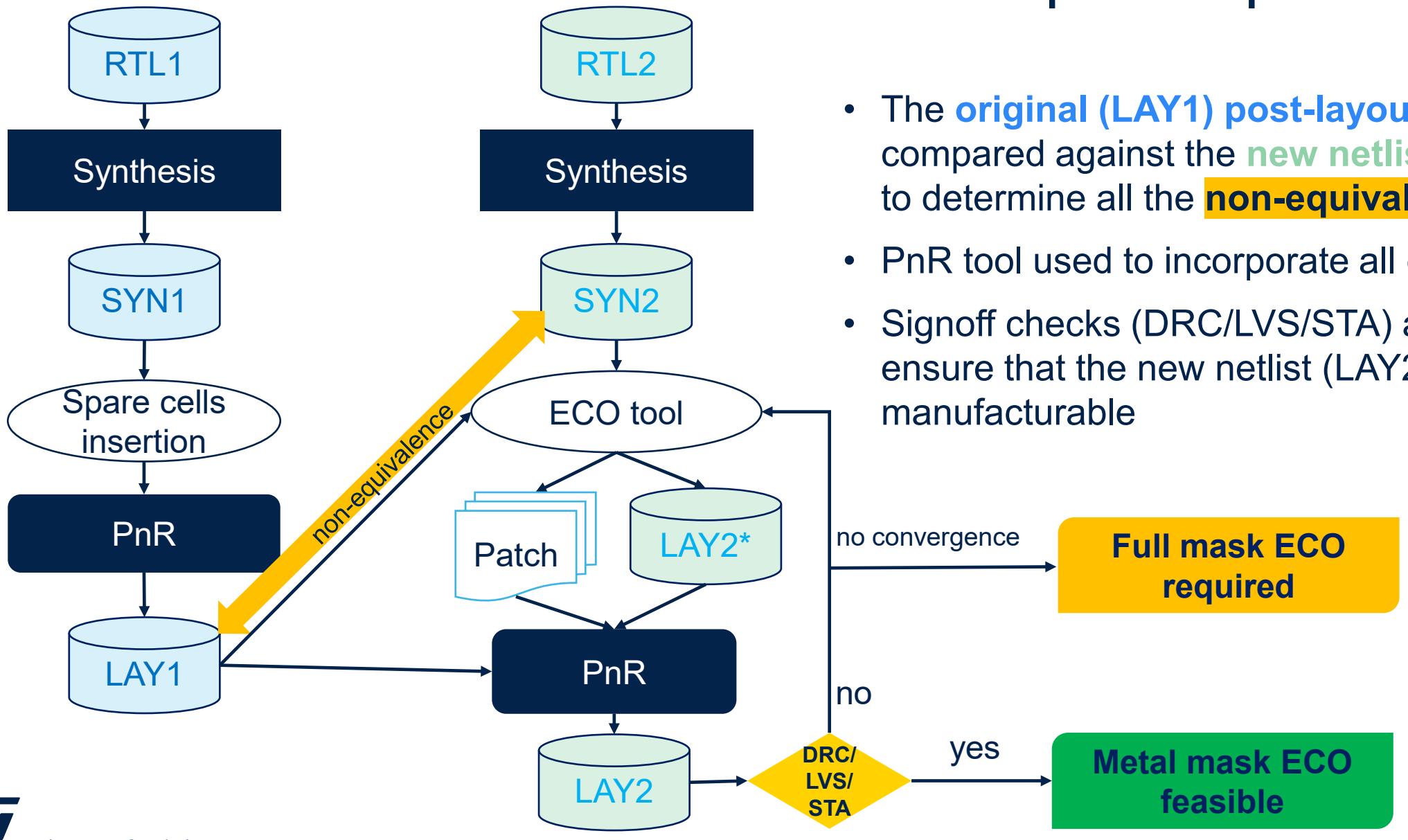
For **small changes** → manual fix is applied to post-layout netlist



For **bigger changes** → specialized EDA tool is adopted (next slide)

Question: is metal ECO fix feasible?

ECO flow – post tape-out (2/2)



- The **original (LAY1) post-layout netlist** is compared against the **new netlist (SYN2)** to determine all the **non-equivalences**
- PnR tool used to incorporate all changes
- Signoff checks (DRC/LVS/STA) are run to ensure that the new netlist (LAY2) is manufacturable

* layout file (.v) with added instances and connection

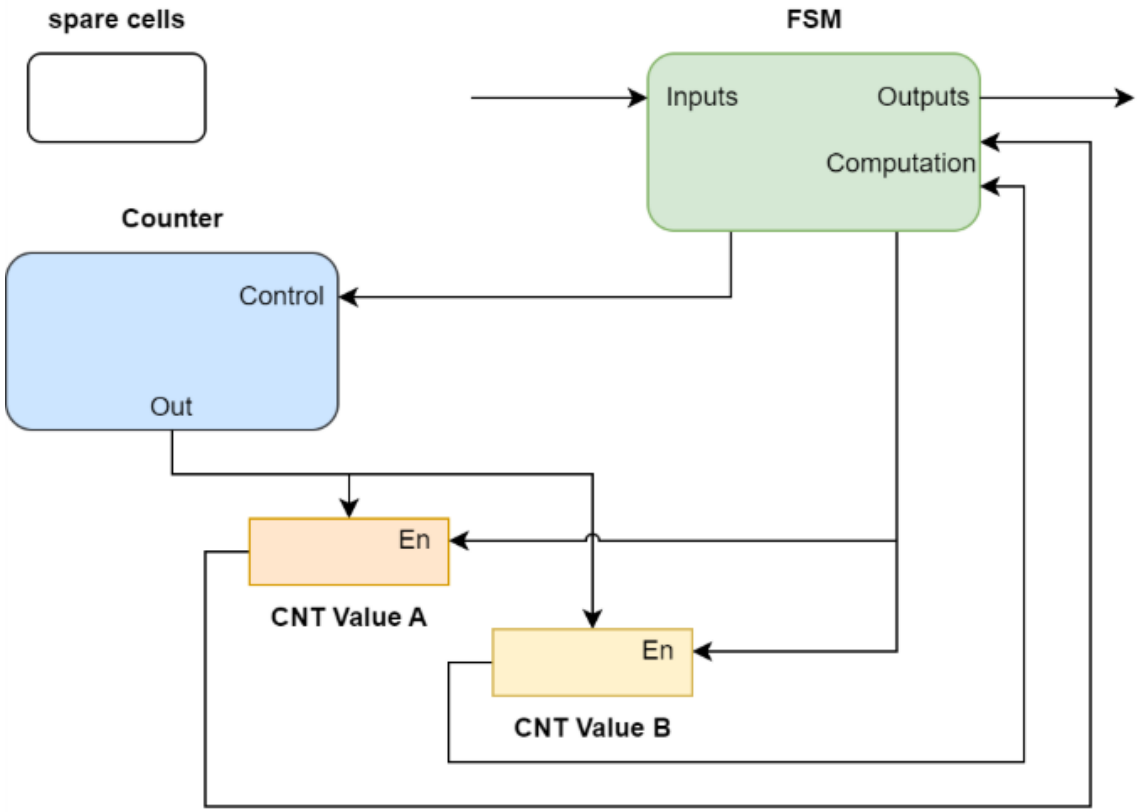
Test case description (1/2)

Original module architecture:

- Achieved area and performance trade-off using a single counter built from enlarged half-adder cells
- Control and sequencing managed by a Finite State Machine (FSM)

On-silicon testing revealed:

- Input signal dynamics were faster than anticipated
- FSM-based control introduced unacceptable computational latency



ORIGINAL ARCHITECTURE

Test case description (2/2)

Identified limitation

FSM delays incompatible with rapid input transitions

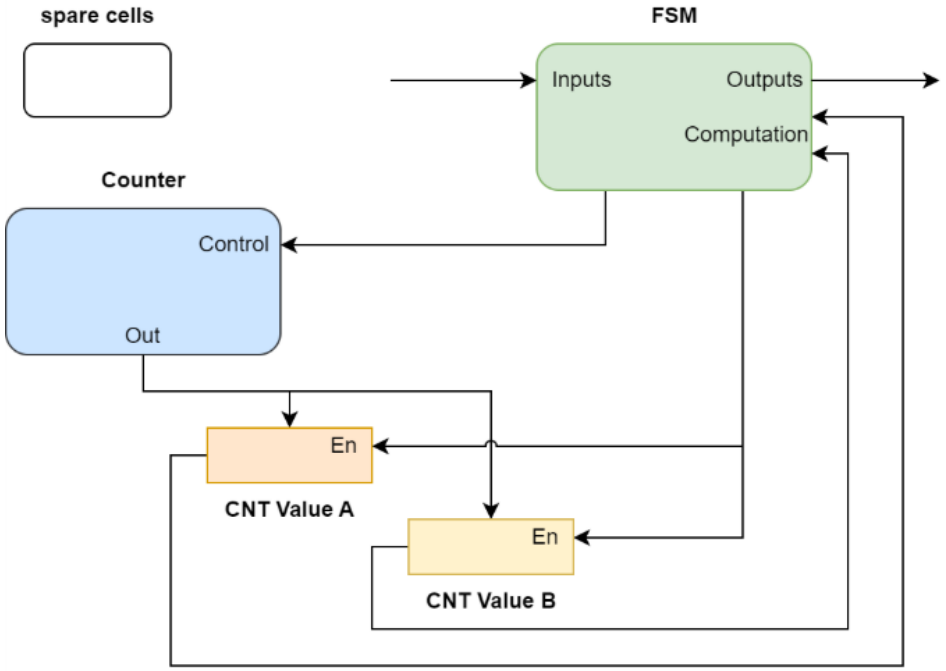
Solution implemented

➔ Eliminated FSM

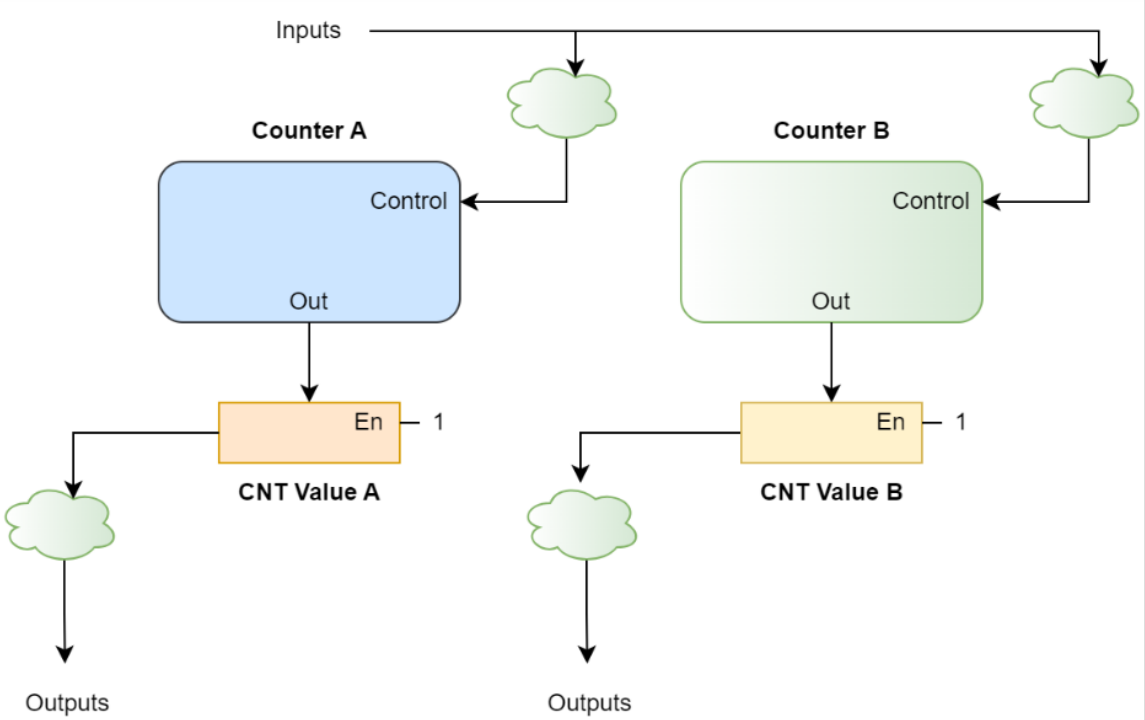
➔ Introduced a second counter

Outcome

- Overcame hardware bottlenecks
- Met stringent timing requirements imposed by accelerated input signals



ORIGINAL ARCHITECTURE



SOLUTION IMPLEMENTED

Standard ECO flow – Results

	Standard flow
Spare cells	149 logic instances 21 FF
Unused cone logic	Few existing cells (~10%) have been reused
CTS	Not balanced
DFT	Manual addition of new flops to existing scan chain
DRC	Long nets cause huge number of max cap/trans violations (>100)
DRV	Metal shorts and metal spacing violations (~250)

Key limitations

⚠ Extensive RTL-level modifications

⚠ Insufficient spare cells

⚠ Metal shorts & Timing violations

Conclusion:

🚫 Metal-only ECO not feasible with current implementation

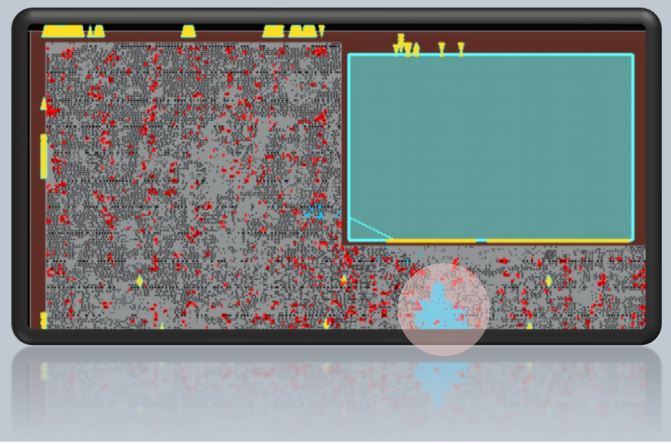
⚠ Full mask set ECO required to handle the scope of changes

Standard ECO flow – challenges (1/2)

1 Spare cells

- Not enough **spare cells** in the area of the **RTL module**
- Spare cells are too far apart

→ **Long nets/interconnections**

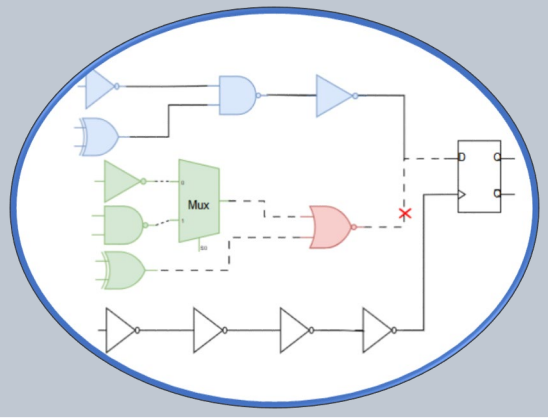


RTL module spare cells

2 Unused logic cone

- Logic beyond the old connection point **(red)** is not reutilized
- Old **(Green)** logic is not remapped to the new **(blue)**

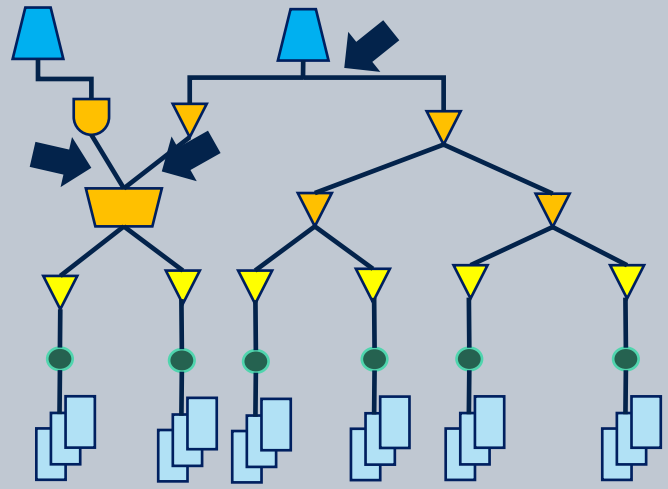
→ **Power Consumption**



3 CTS

- New flops added to trunk nets ( )
- No clock tree-balancing

→ **setup and hold violations**

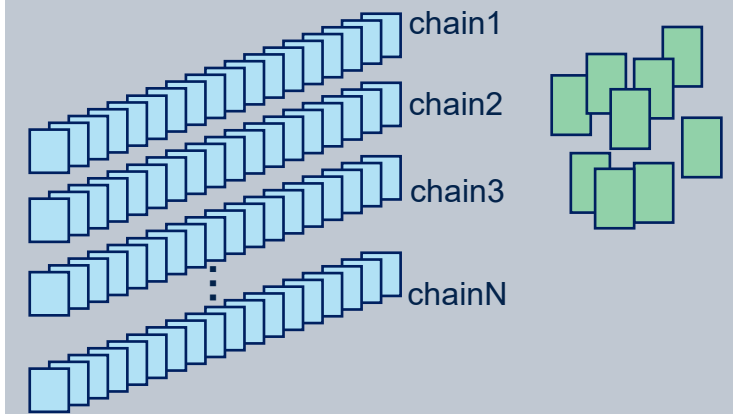


clock source clock leaf clock gates
clock trunk flip flops

Standard ECO flow – challenges (2/2)

4 DFT

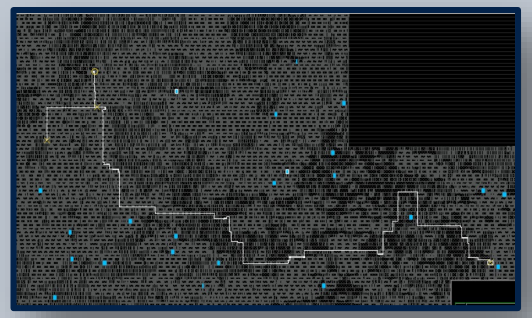
- New FFs are not connected to the existing scan chain
- Hand connection is necessary
- Impact on **DFT coverage**



existing scan chain new flops

5 DRV

- Distant spare cells → very long nets
- Max capacitance and max transition violations
- High number of buffers required



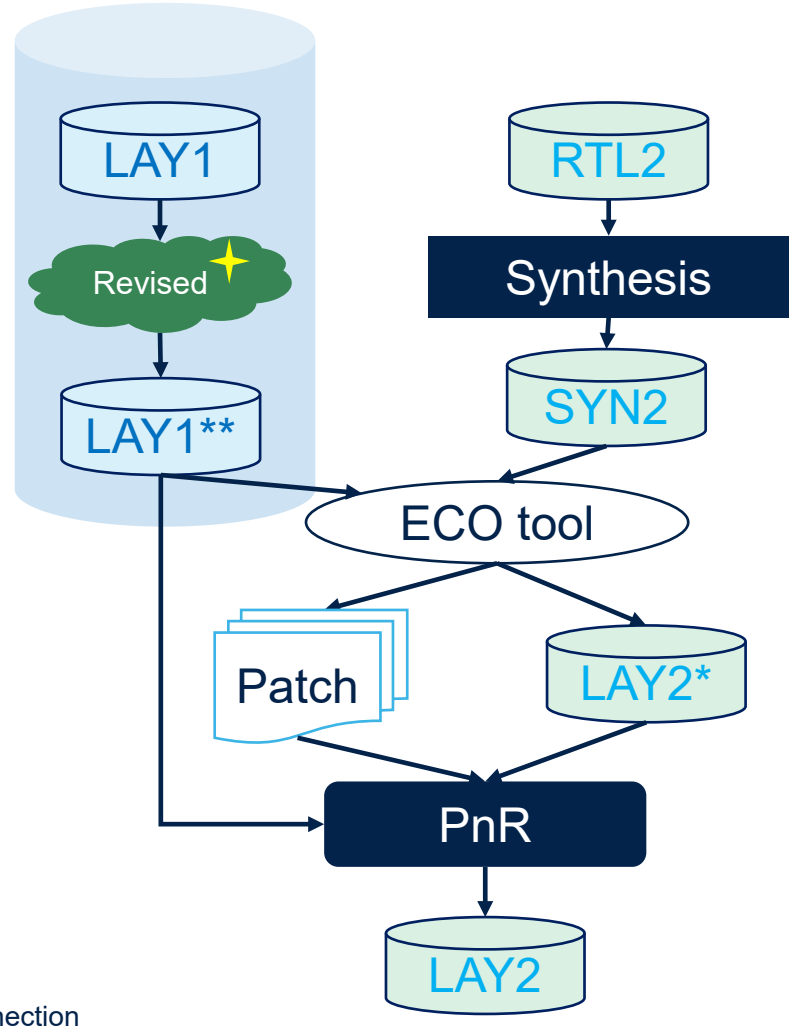
available buffers

6 DRC

- Routing congestions
- Metal shorts
- NDR (non-default-rule)

Proposed ECO flow (1/3)

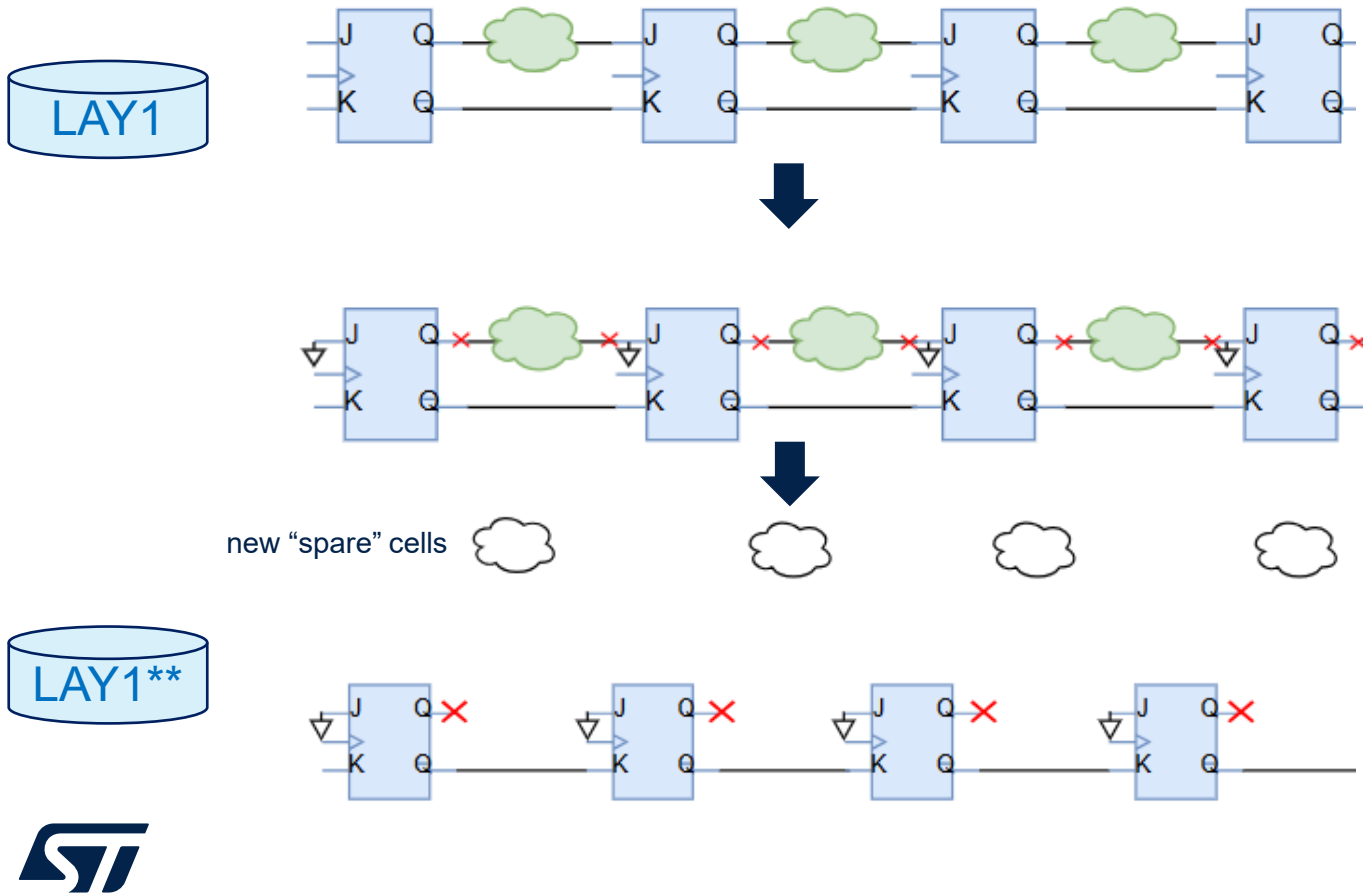
A **revised version** of the post-layout netlist is provided to the ECO tool. This netlist incorporates a series of **targeted modifications** aimed at **enhancing the tool's effectiveness** in resolving the issues encountered.



* netlist file (.v) with added instances and connection
** netlist file (.v) with targeted modifications

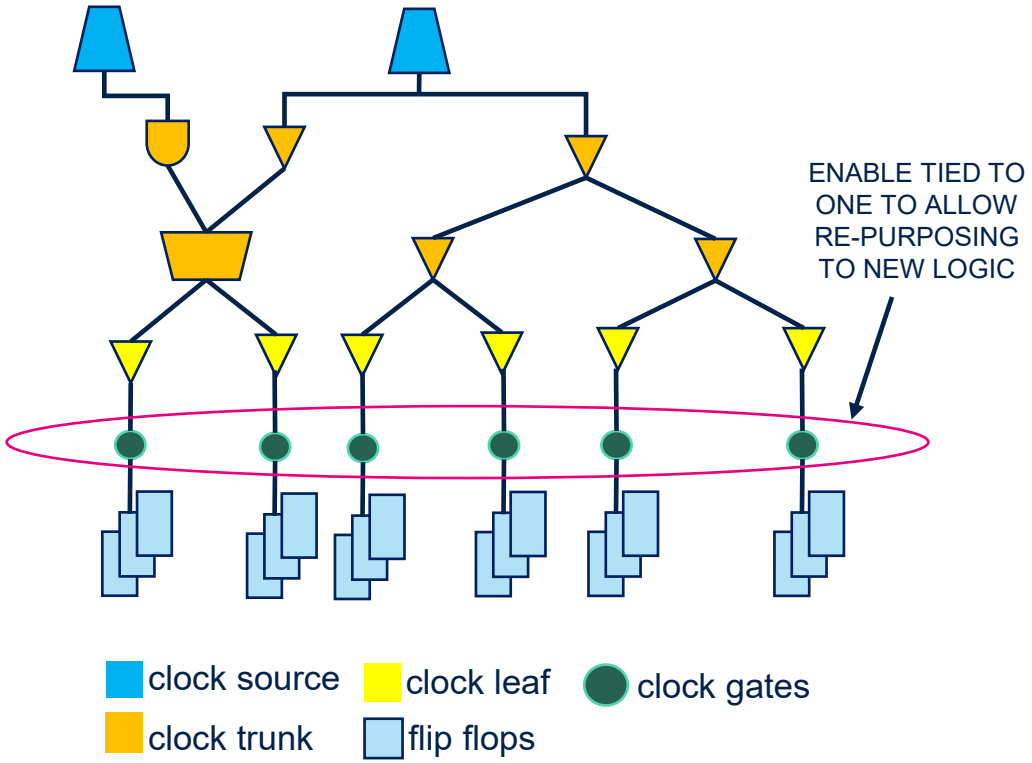
Proposed ECO flow (2/3)

Flip flop and DFT structure from original RTL module are **preserved** while all **combinational logic** gates are freed to become the new **“spare cells”**

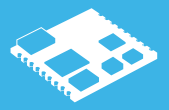


Clock tree structure is mostly preserved

Setup and hold timing ensured



Proposed ECO flow (3/3)



RTL + Verilog

- Retained flip-flops, clock tree, and DFT structure
- Allowed reuse of logic gates between flip-flops
- Kept original RTL register names unchanged
- Maintained verification tool compatibility

ECO tool

- Reused majority of FSM logic to map the new counter logic
- Limited number of spare cells
- New flip flops of Counter B remapped to old unused flop logic from FSM

Place and route tool

- Reused all cells located in the area of the module being rewritten
- DFT coverage and scan chain length not impacted
- Better routability
- No metal shorts
- Setup/Hold timing MET

STANDARD ECO FLOW		PROPOSED ECO FLOW
21 spare FF 149 spare logic cells	Spare cells	0 spare FF 22 spare cells instances
Limited logic reuse (~10%) unused logic disconnected	Unused logic cone	New logic remapped from previous FSM simplification (446 cells re-used/557)
Clock-tree structure needs manual intervention to fix setup and hold violations	CTS	Preserved synchronization between existing flops (setup/hold MET)
Manual addition of new Flip-Flops required Unbalanced scan chains	DFT	Original scan chain and DFT coverage preserved
Long nets High max cap/trans violations (>100)	DRV	Shorter nets Low of max cap/trans violations (~30)
Routability issues, DRC (~250) Metal shorts	DRC	No routability issues No metal shorts
⇩		⇩
Metal ECO is not feasible		**Metal ECO is feasible**

Summary and conclusion

- **RTL module redesign** was required to address hardware timing constraints identified during on-silicon validation.
- **Standard ECO flow** provides good automation and flexibility but exhibited limitations and challenges that initially made metal ECO implementation unfeasible.
- **Proposed ECO flow** maximizes reuse of existing standard cells, preserving flip-flops, clock tree, and scan chain connectivity of the original module design.
- Proposed ECO flow **overcomes the limitations of the standard approach** by improving efficiency and resolving routing and DRC issues.
- This approach **enabled metal ECO implementation** for extensive RTL restructuring, resulting in a significant **reduction in manufacturing costs**.

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