

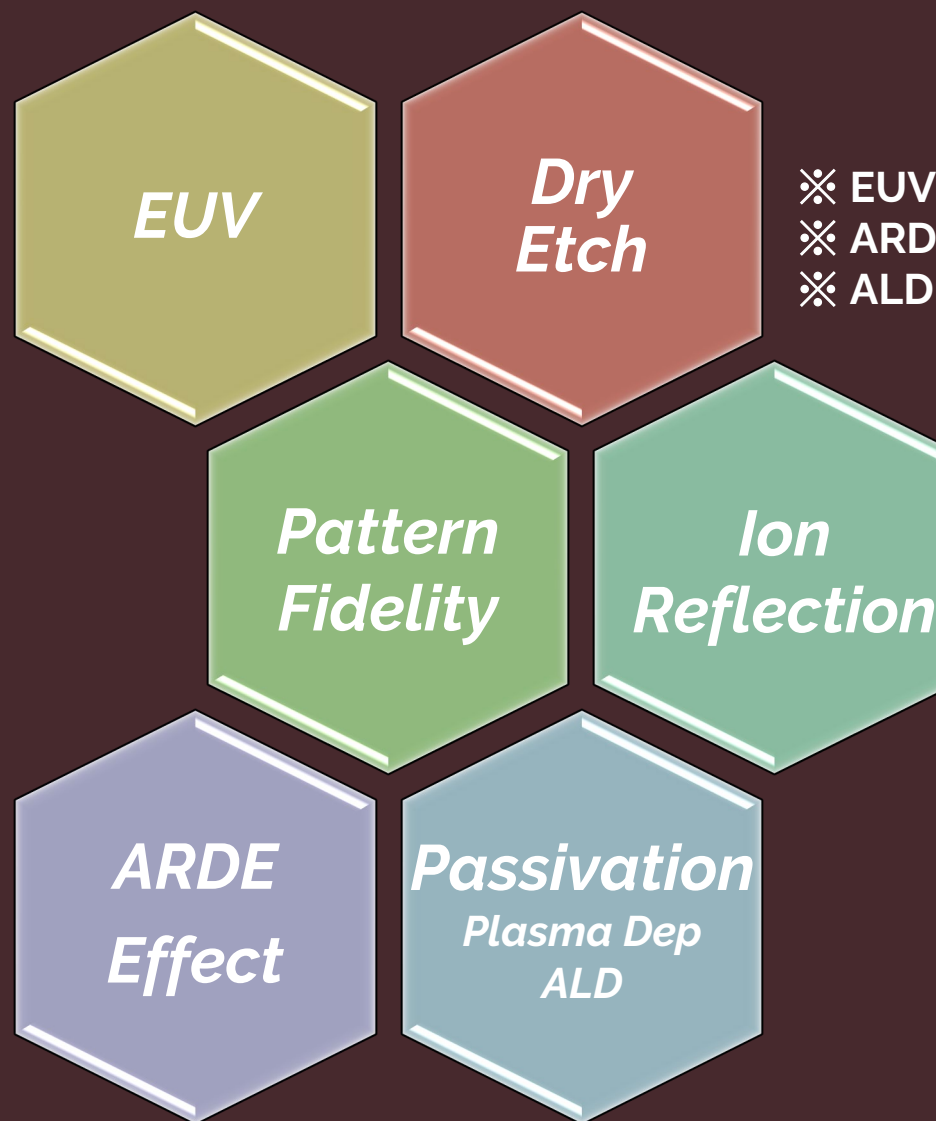
Novel Dry Etch Process Technology Enabling Precision at the Nanoscale: Pushing the Limits of Advanced EUV Patterning

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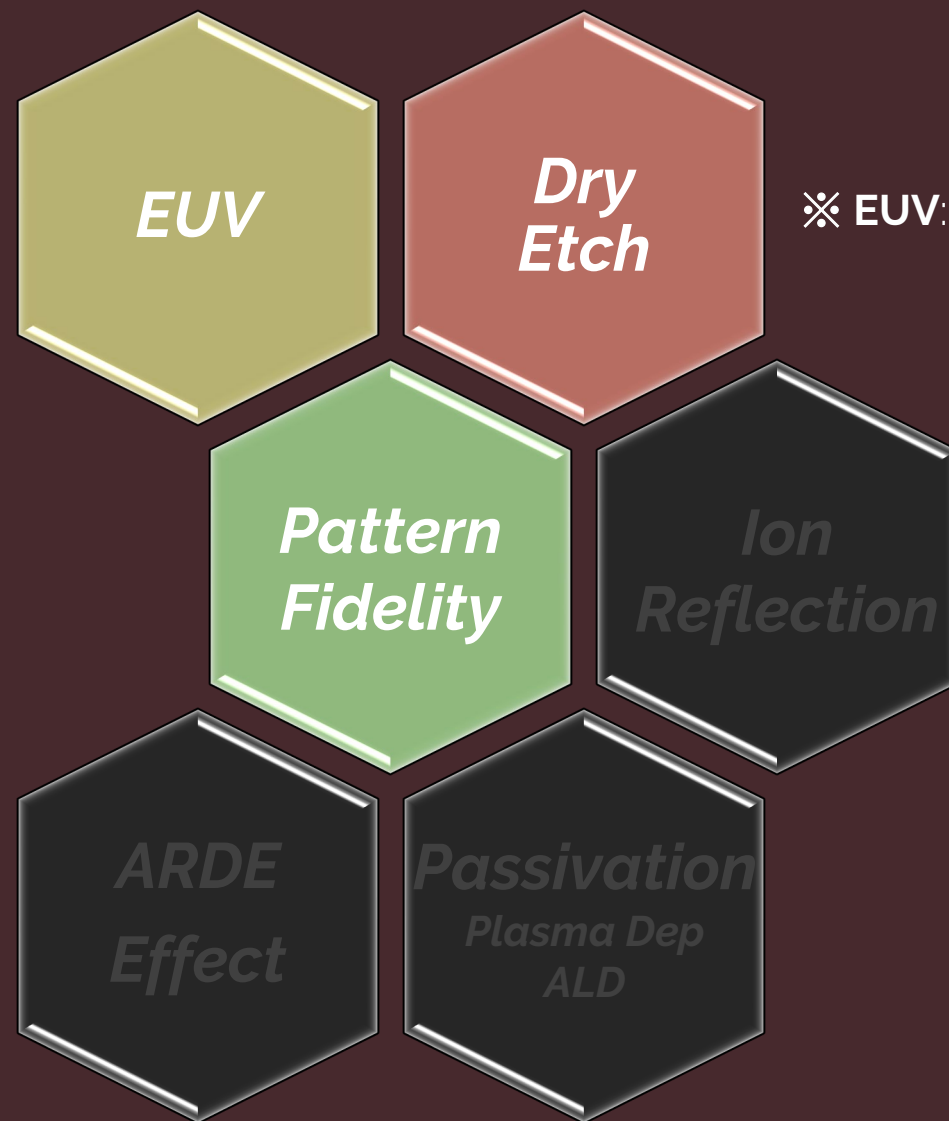


Author: Jasmine Chang
ADT PEE Dry Etch
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These Words Will Keep Coming Up

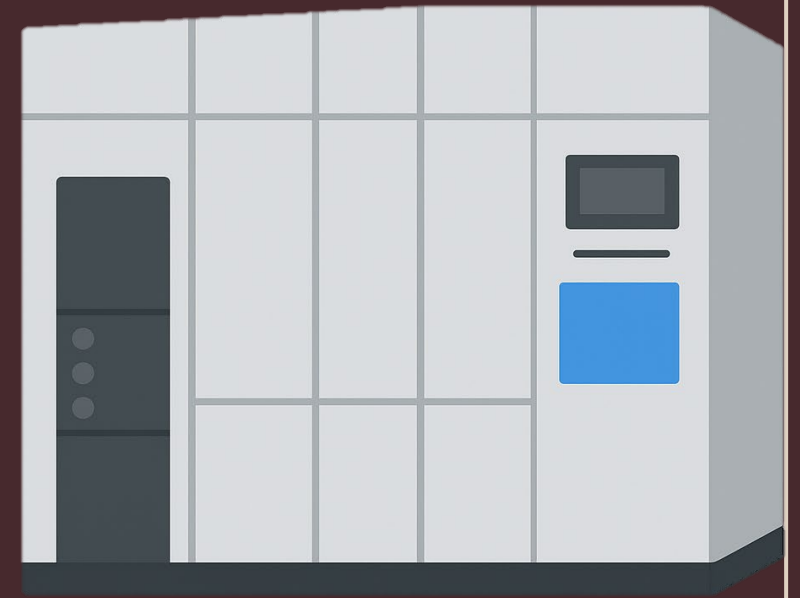


- ※ **EUV**: Extr^em^e Ultraviolet Lithography
- ※ **ARDE**: Aspect Ratio Dependent Etching
- ※ **ALD**: Atomⁱc Layer Deposition



Why EUV for DRAM?

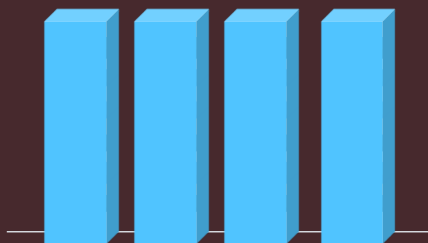
- DRAM scaling requires finer patterning beyond ArF immersion limits
- EUV enables single-patterning for critical layers, reducing process complexity
- Improves edge placement accuracy and CD uniformity
- Supports advanced DRAM nodes
- **Future trend:**
 - Hybrid lithography and multi-pattern EUV for sub-10nm features



What Are Dry Etch Challenges in EUV Patterning?

- Critical for accurate pattern transfer
- Enhances anisotropy and pattern fidelity
- **Challenges:**
 - Selectivity between EUV resist and film stack
 - Complex hybrid pattern
 - High-Aspect-Ratio Structures

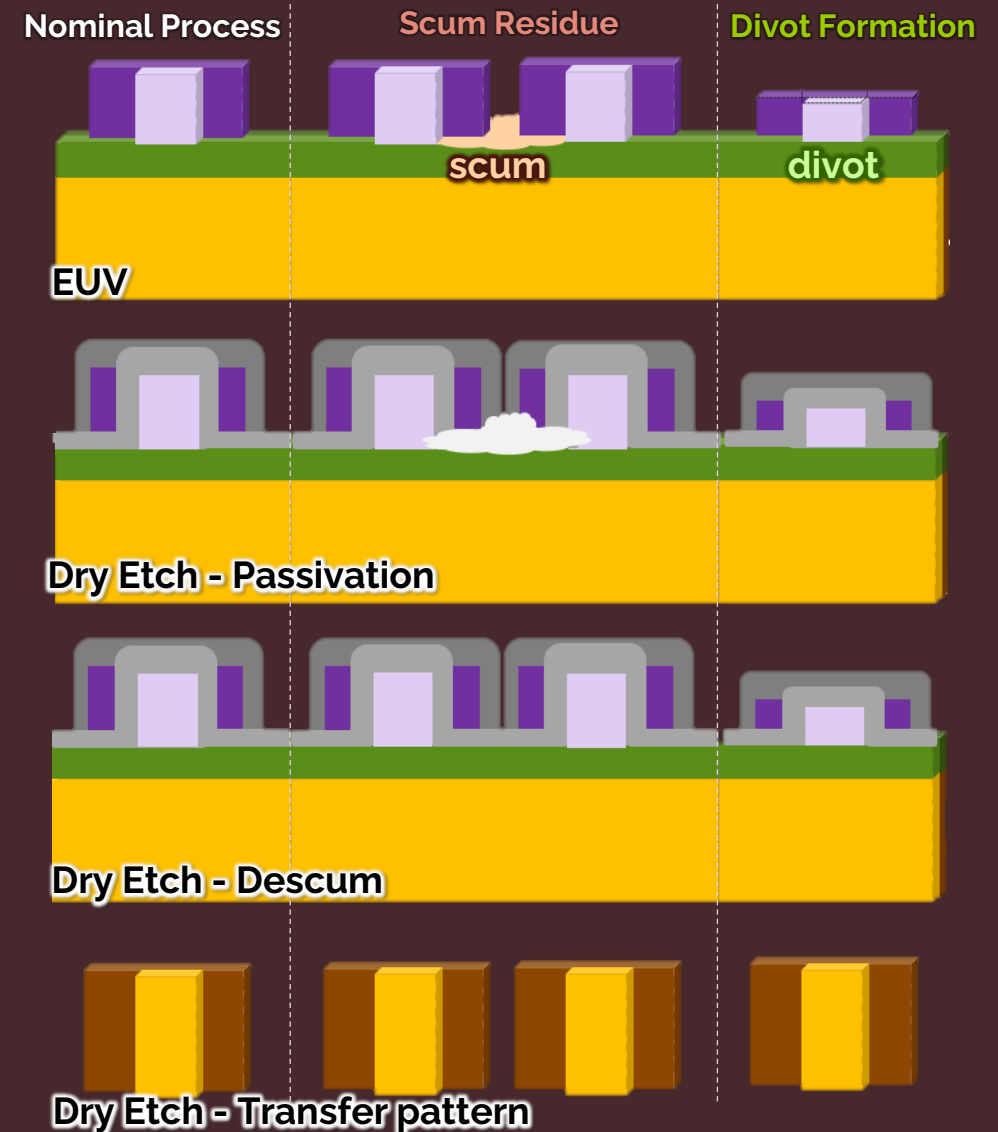
Single pattern

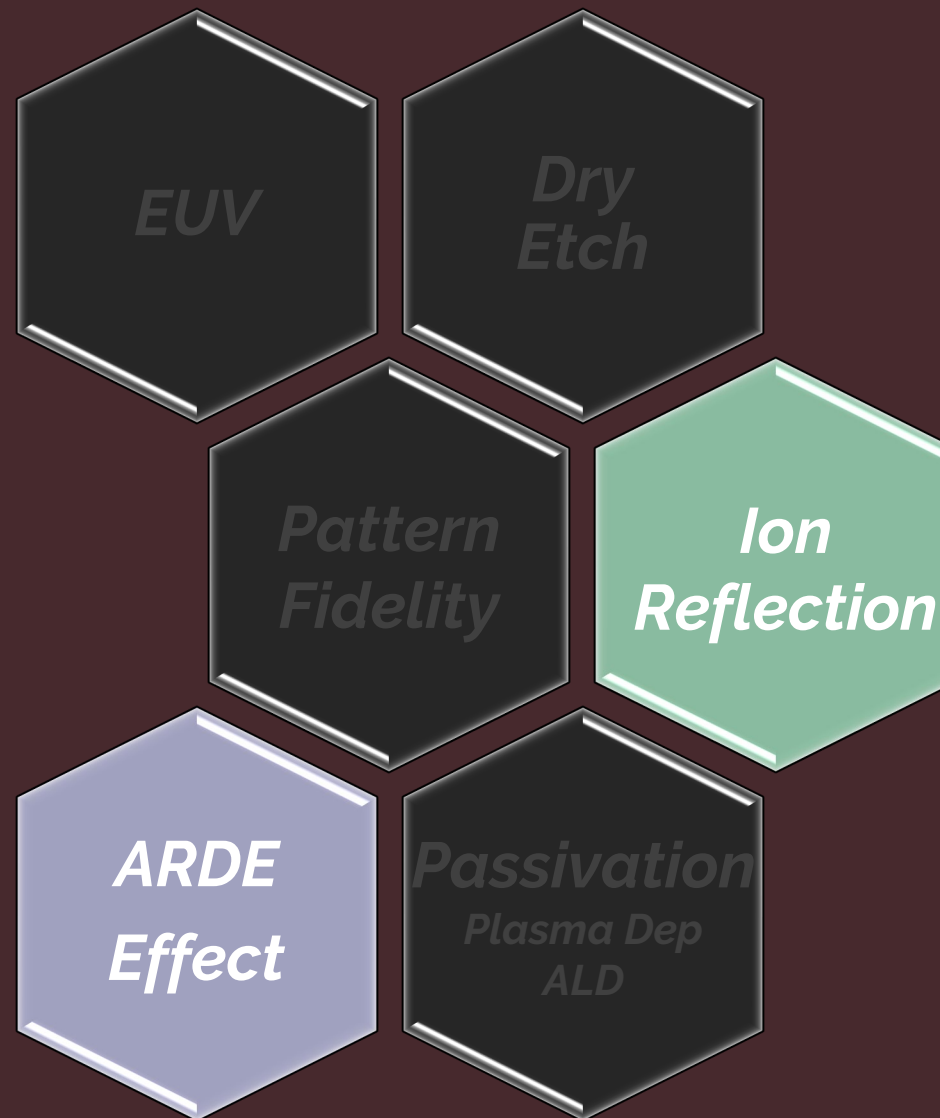


Complex hybrid pattern



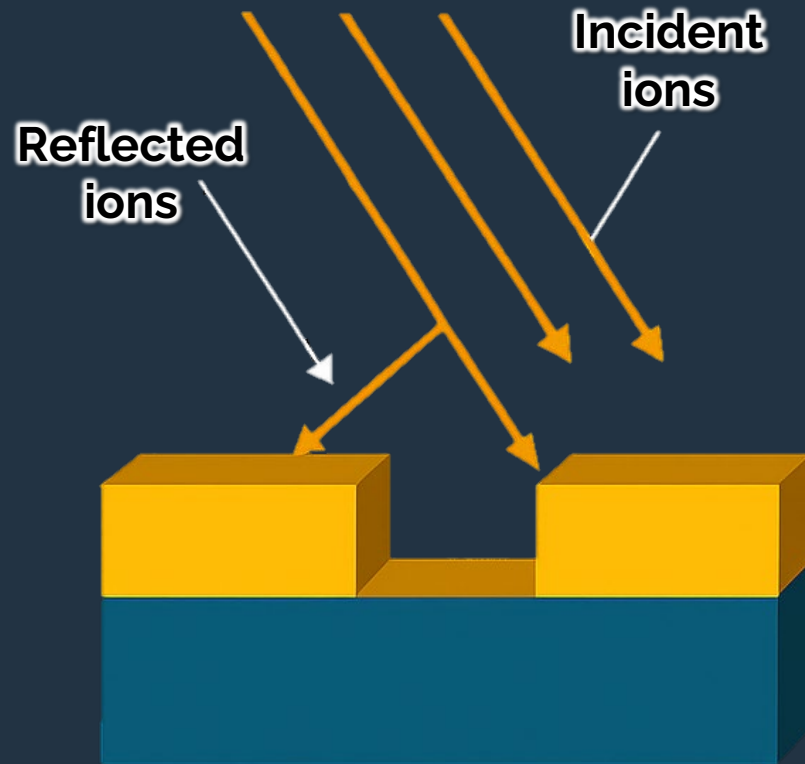
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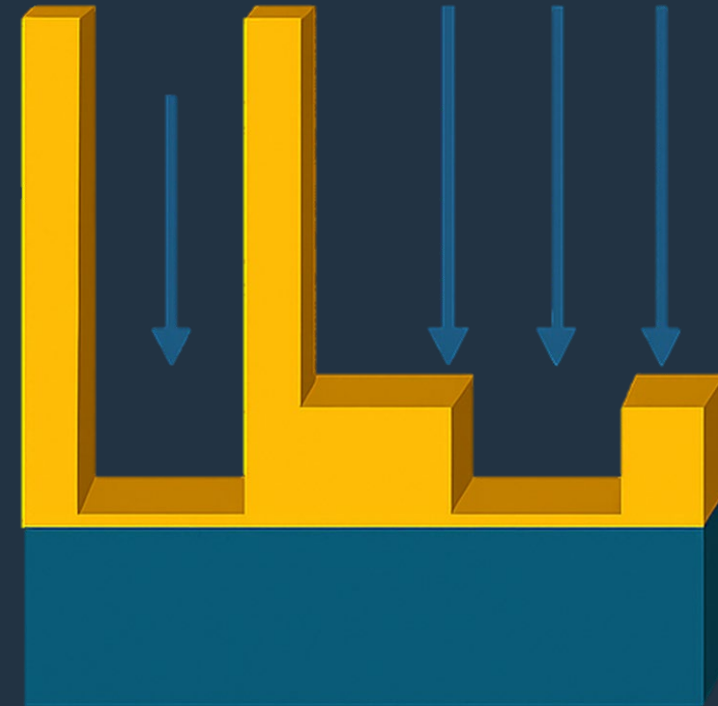


※ ARDE: Aspect Ratio Dependent Etching

Key Etch Effects in Ion-Based Processes



Ion Reflection effect



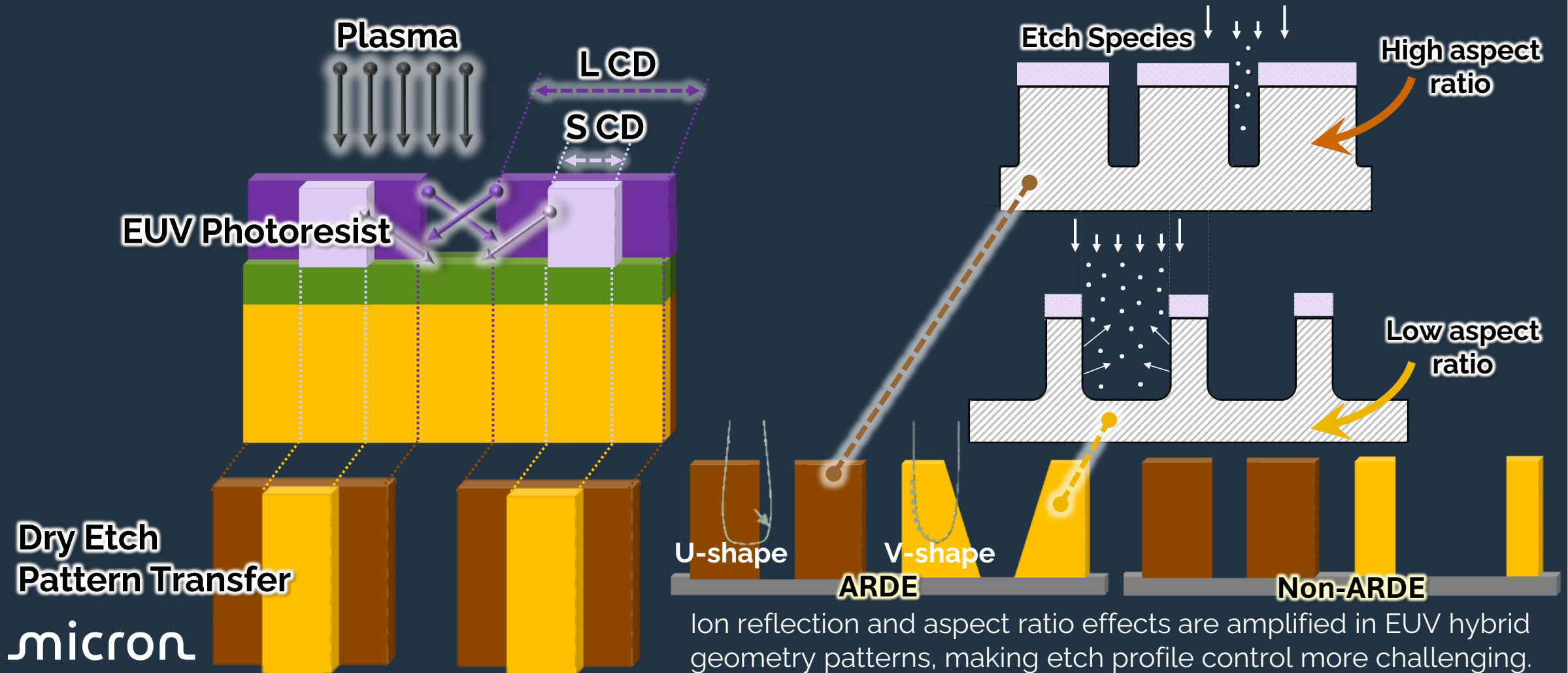
Aspect Ratio Dependent Eetch effect

Ion reflection and aspect ratio effects are critical factors influencing etch profile control in ion-based dry etch processes.

Key Etch Effects in Ion-Based Processes

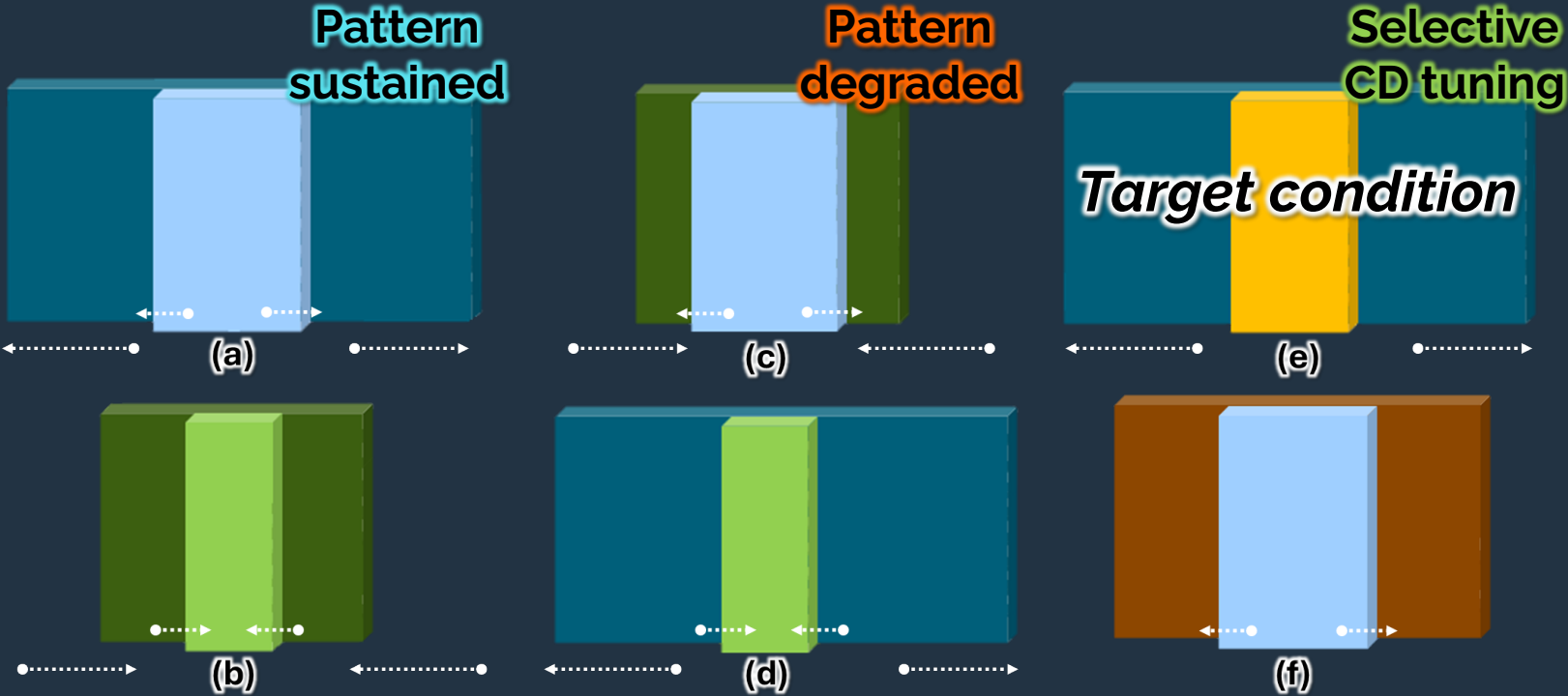
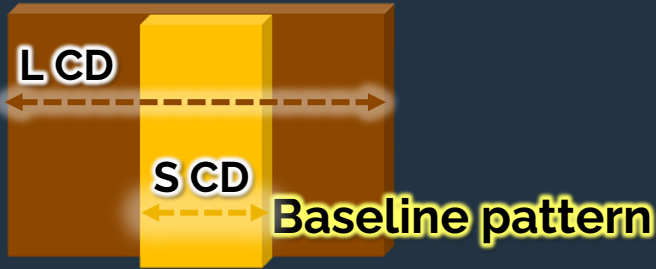
Ion Reflection effect

Aspect Ratio Dependent Etch effect



Selective CD Tuning for EUV Pattern Preservation

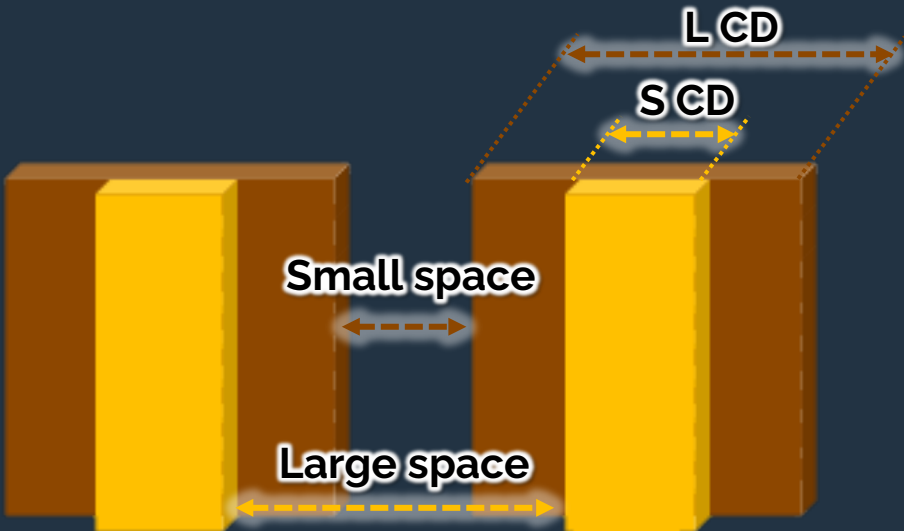
Case	L CD post Dry Etch	S CD post Dry Etch	L-S CD post Dry Etch	Sustain shape of EUV pattern
(a)	↑	↑	Keep	Yes
(b)	↓	↓	Keep	Yes
(c)	↓	↑	Decreases	No
(d)	↑	↓	Increases	No
(e)	↑	-	Increases	Proposed
(f)	-	↑	Decreases	No



In EUV-defined novel patterns, case (e) is targeting condition, the faster erosion of L CD poses a challenge for Dry Etch control.

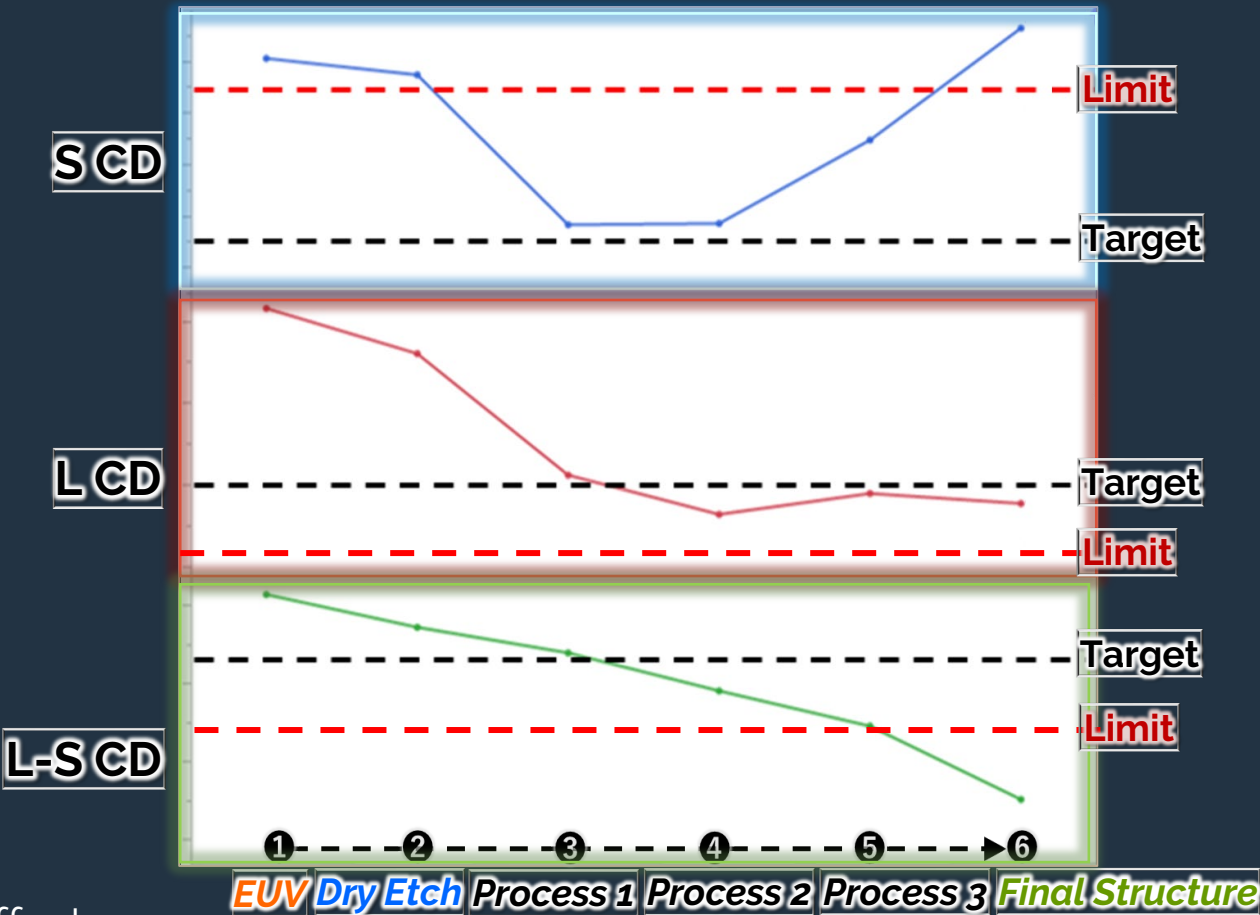


Progressive CD Loss

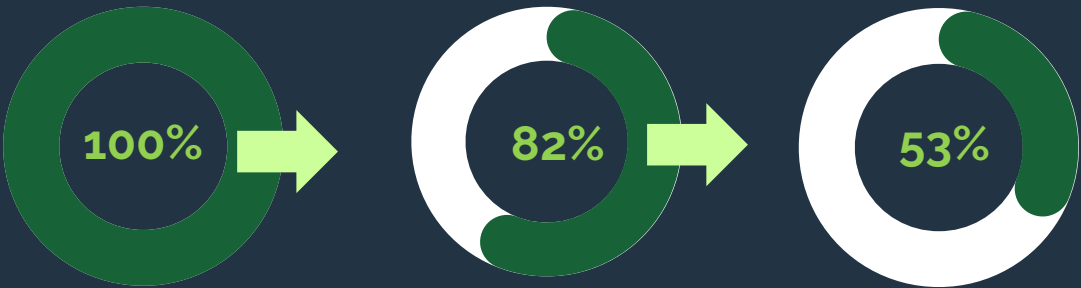


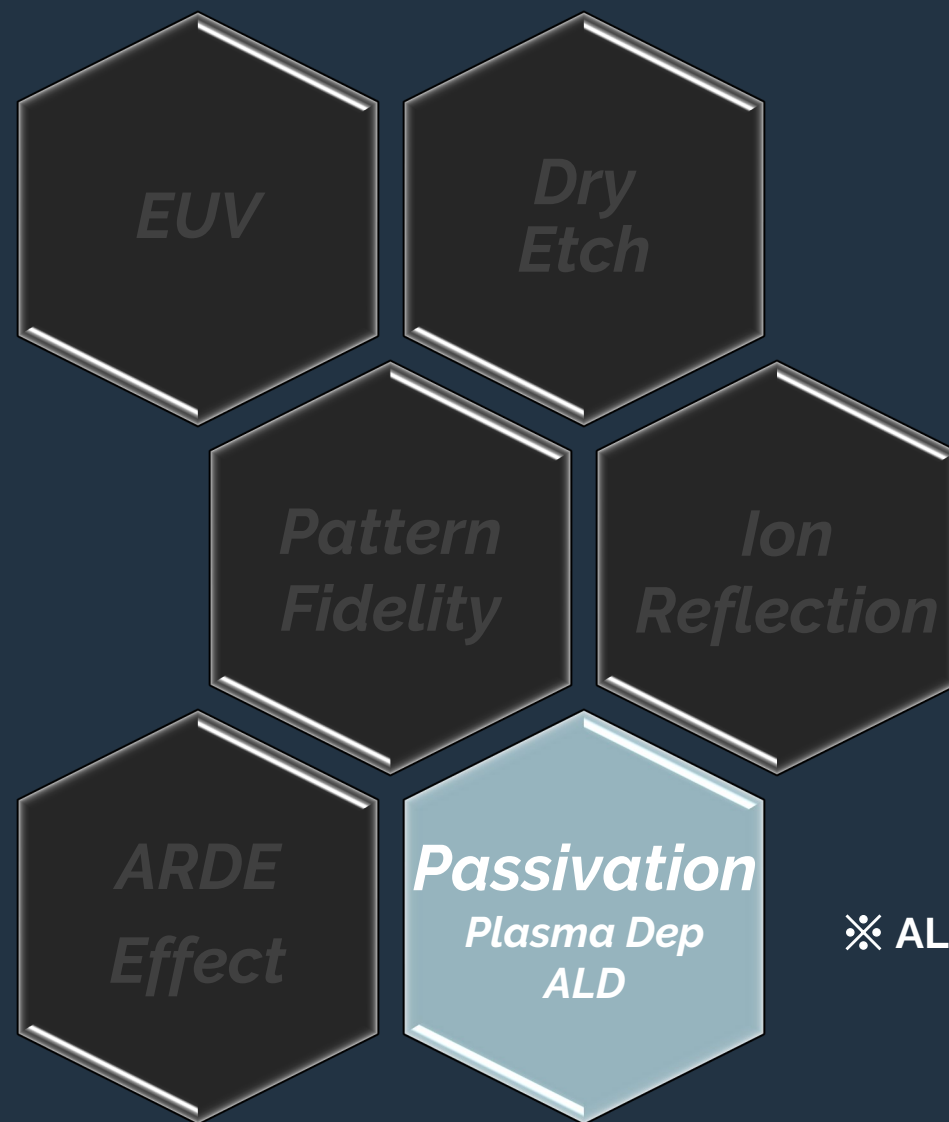
$\text{Pattern Ratio} = \text{L-SCD}$

Progressive L-S CD loss results from cumulative etch effects, such as ion reflection, ARDE, and space-dependent erosion. Effective dry etch tuning is essential to mitigate.



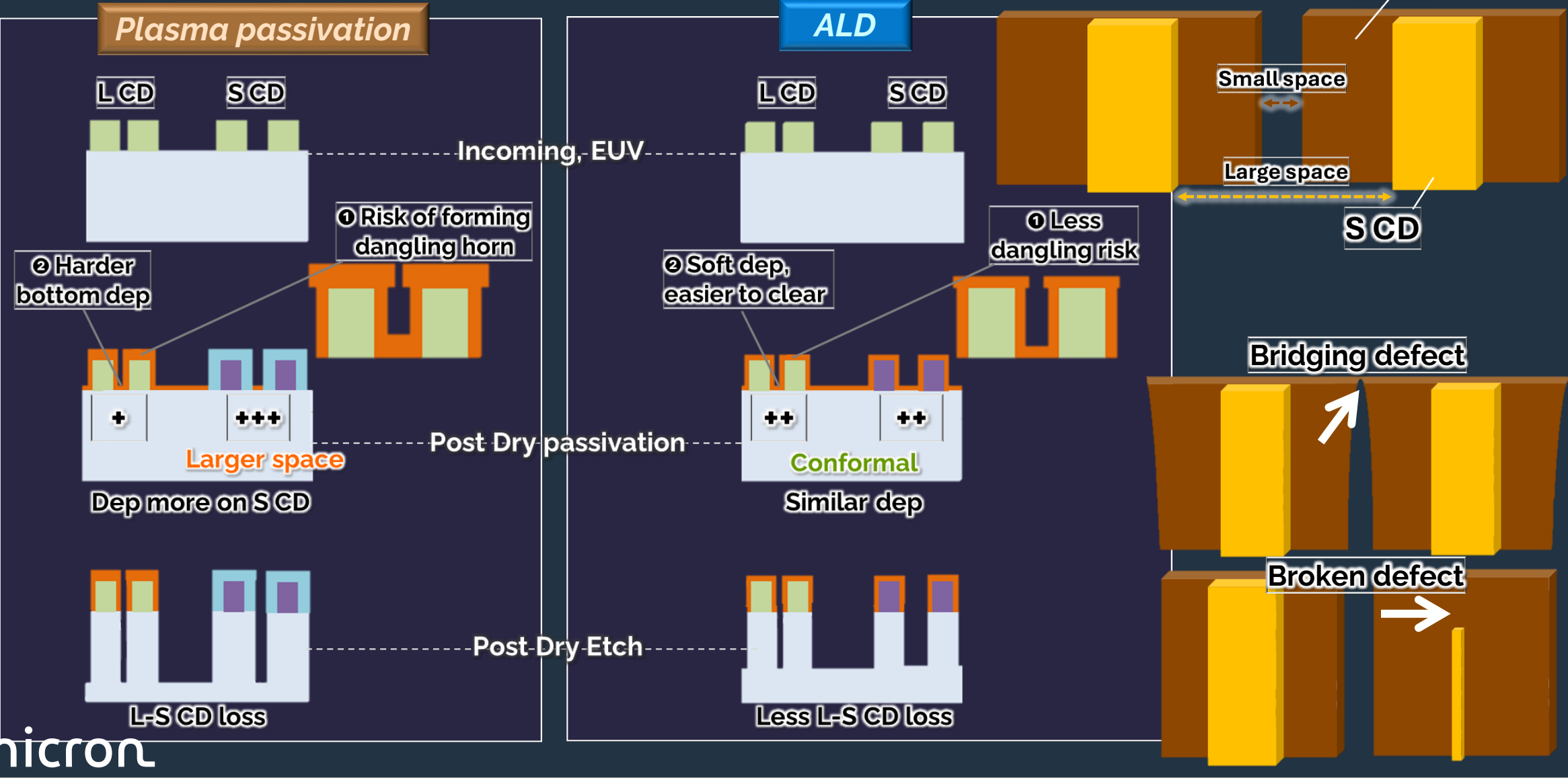
L-S CD loss



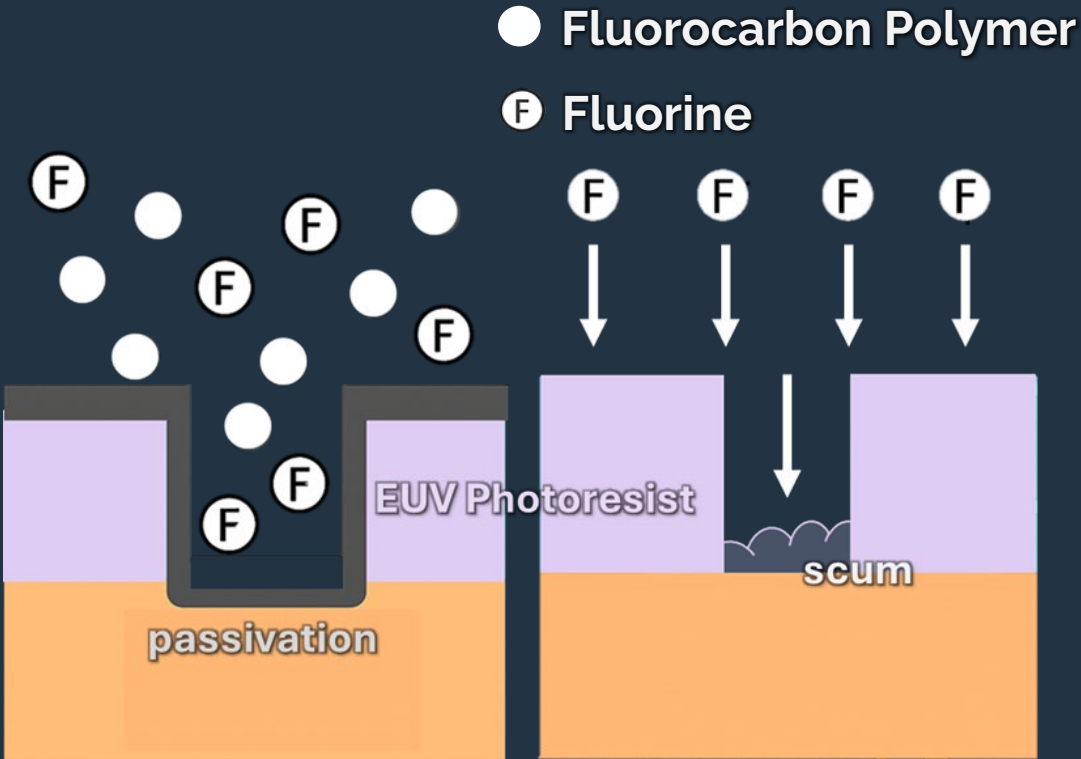


※ ALD: Atomical Layer Deposition

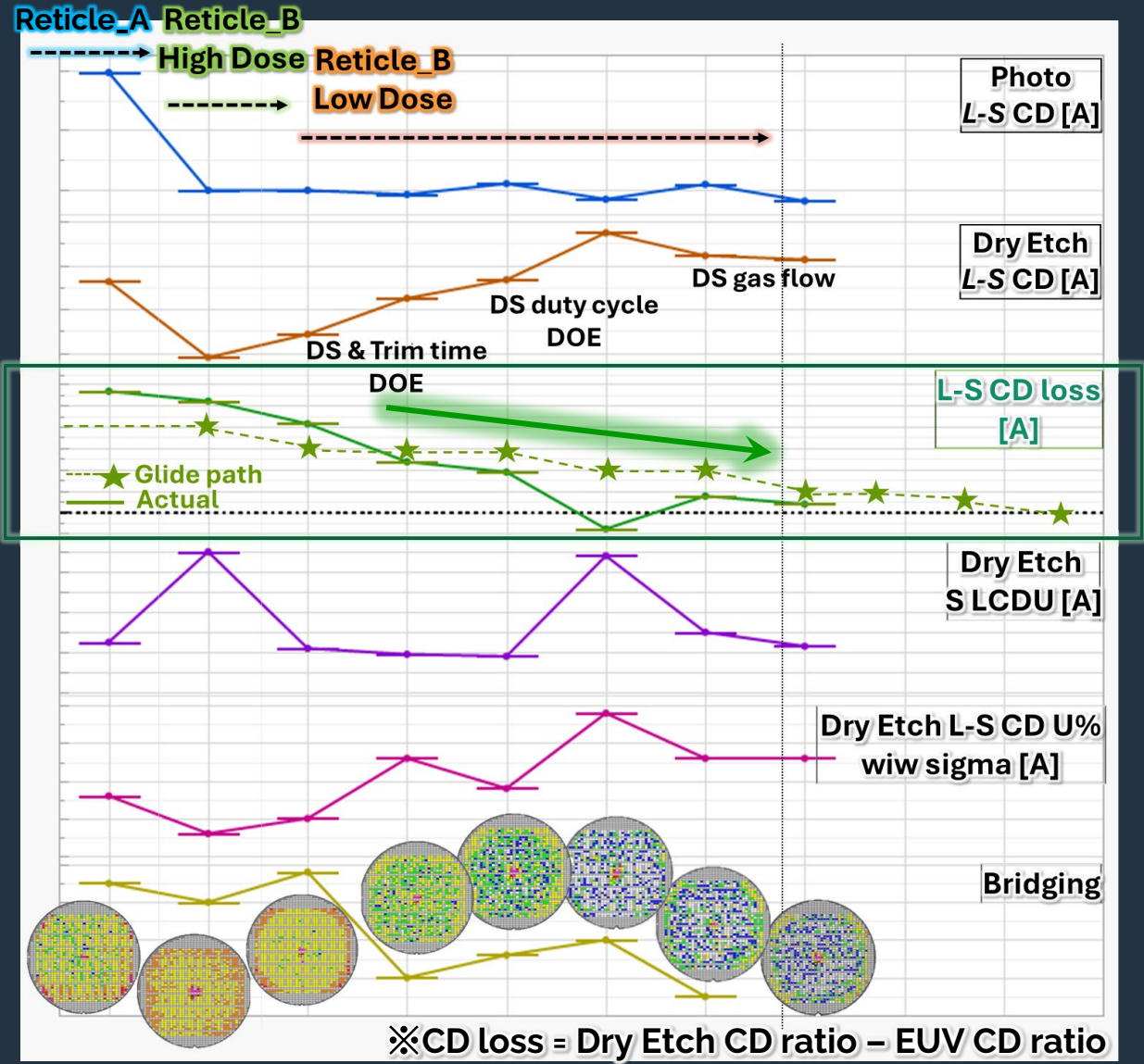
Dry Etch-Driven Passivation



Suppressing CD Loss through Dry Etch Engineering



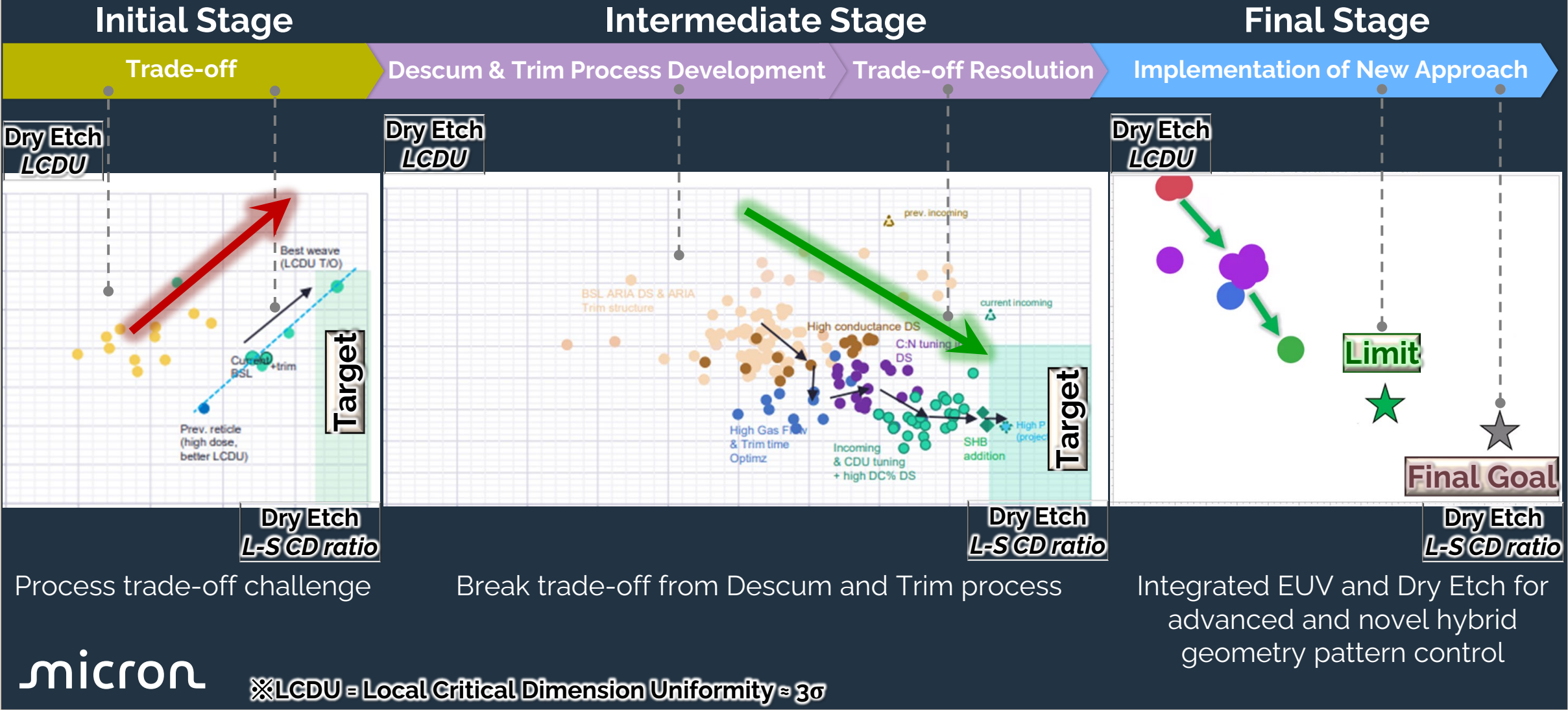
Effective suppression requires a balanced Etch approach, integrating **Descum** and **Trim** processes while carefully managing passivation and etching dynamics.



Dual Pattern Etch Roadmap - Let's Dive In



Dry Etch Key Stages to Expand EUV process Window

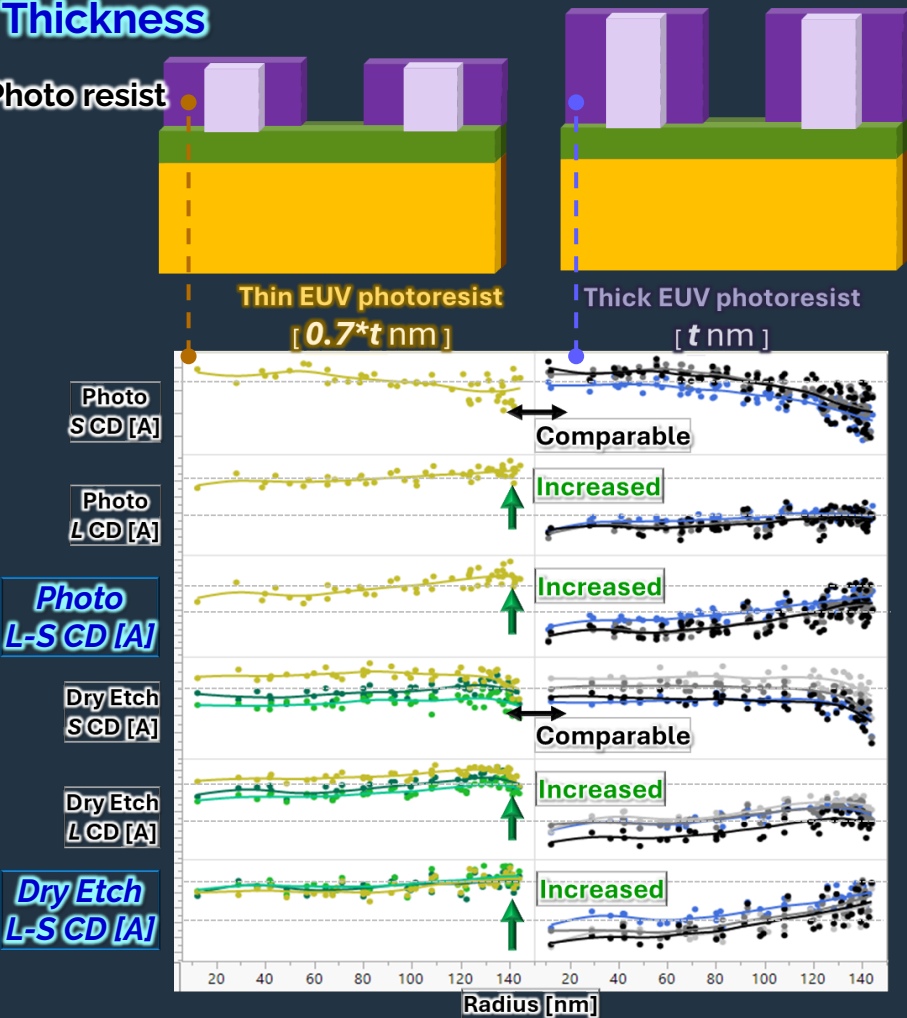


Beyond Etch: Where Else Can We Win?



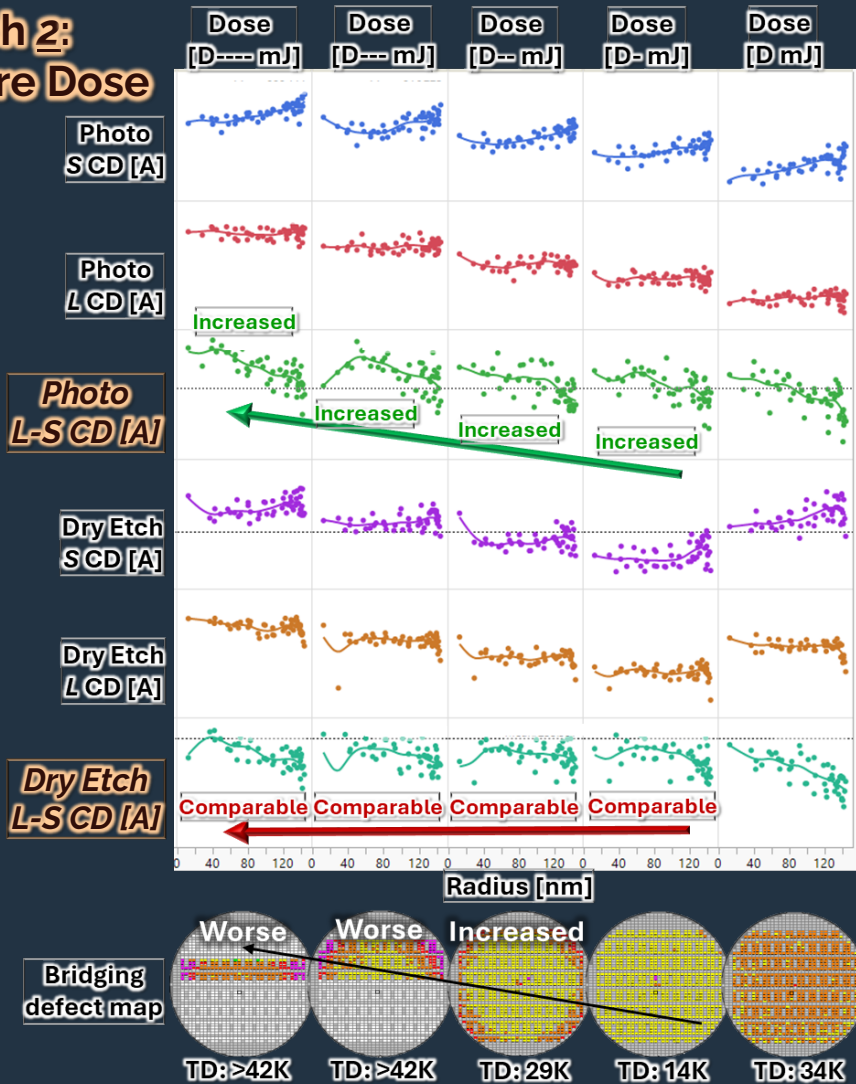
Opportunities in CD loss - EUV Lithography

Approach 1: EUV Resist Thickness



micron Thinner resist brings higher EUV CD ratio

Approach 2: EUV Exposure Dose



Trade-off between Dose, CD ratio & Bridging

Technical Highlights

EUV Lithography [13.5nm wavelength]

Key Features

- Enable scaling to advanced semiconductor nodes
- High resolution
- Process simplification

Challenges

- Mask defectivity
- Resist materials

Dry Etch [Hybrid patterns]

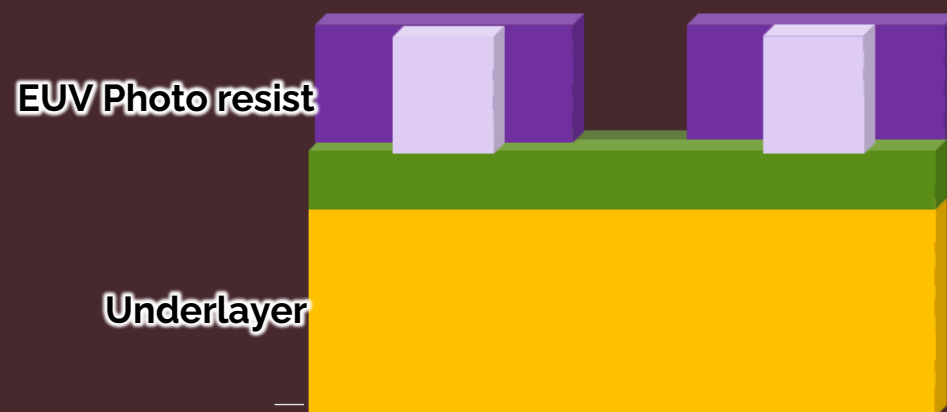
Challenges

- Ion reflection causing CD loss
- Aspect Ratio Dependent Etching effect
- Micro loading

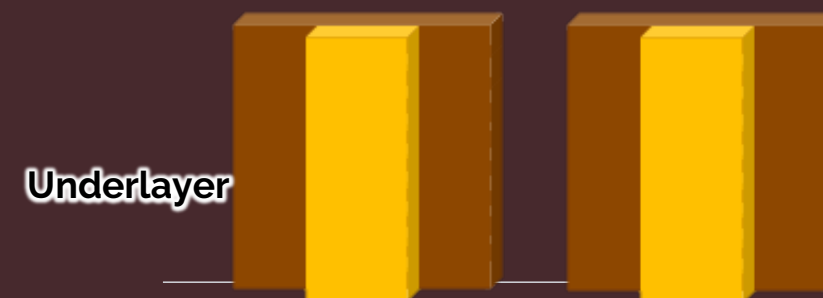
Mitigation

- Passivation techniques
- Gas chemistry selection

Hybrid pattern definition



Pattern transfer to underlayer



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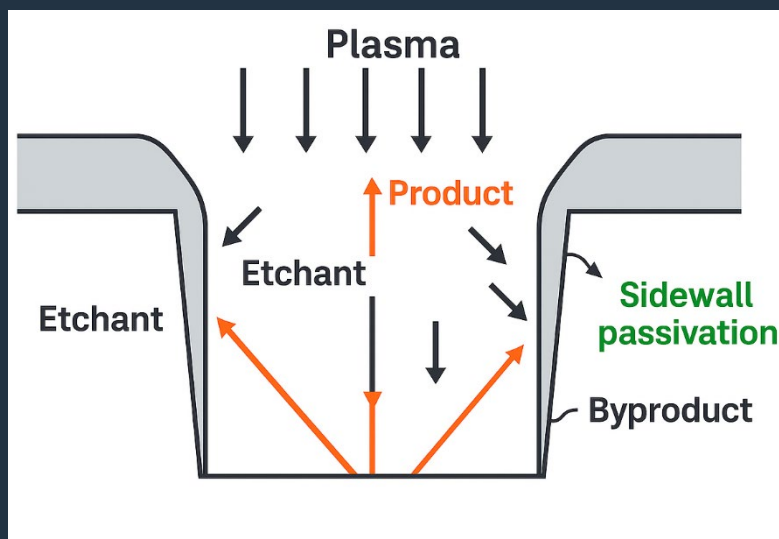


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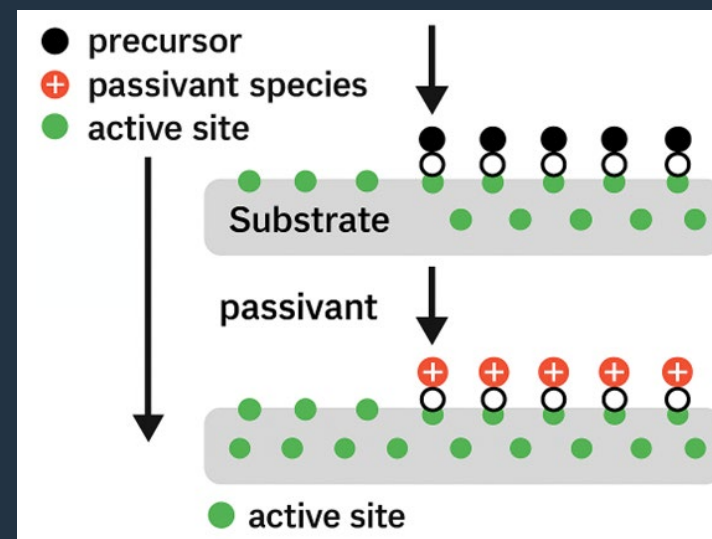
Strategies to Mitigate CD Loss: Dry Etch Passivation

Strategy ①: Plasma passivation



G. S. Oehrlein et al., *Sidewall surface chemistry in directional etching processes*, Materials Science and Engineering: R: Reports, Volume 24, Issue 4, 15 December 1998, Pages 153-183.

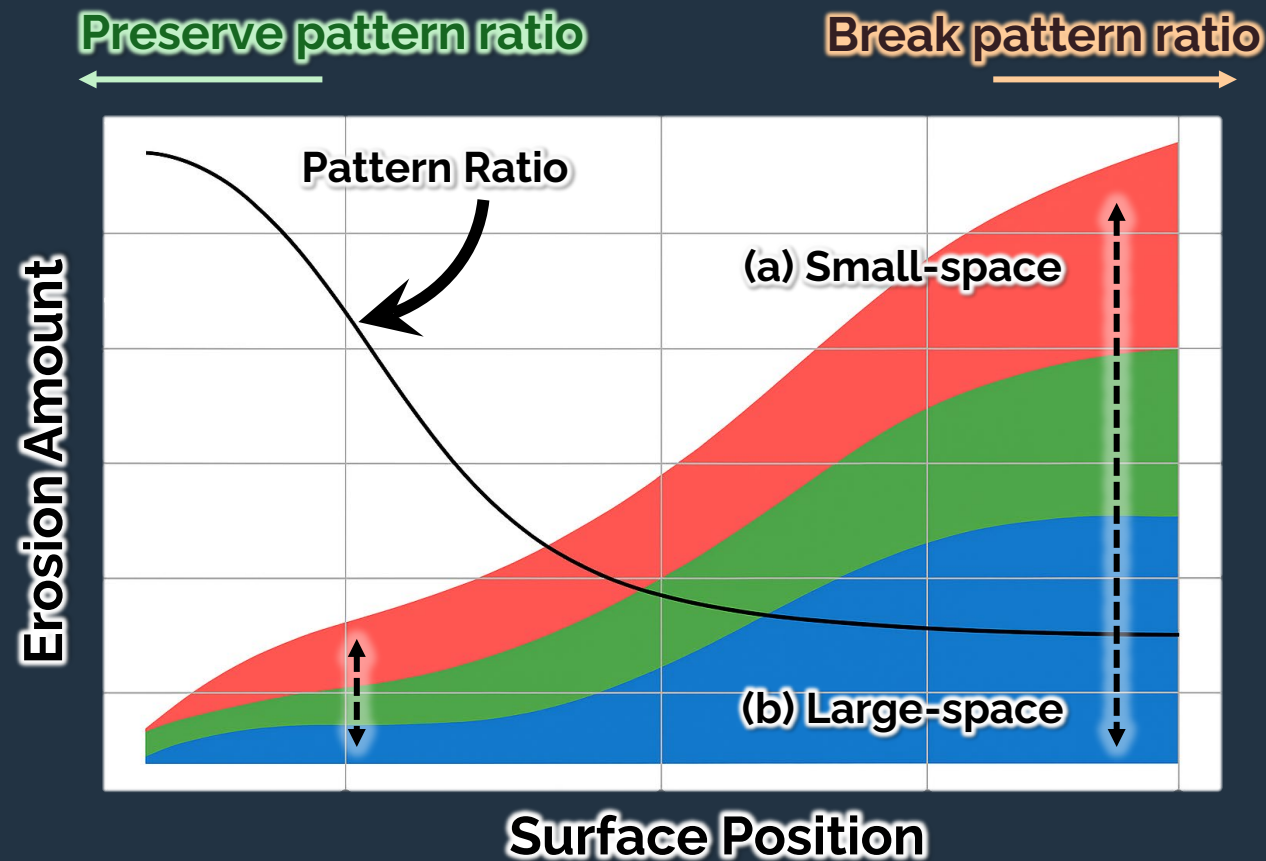
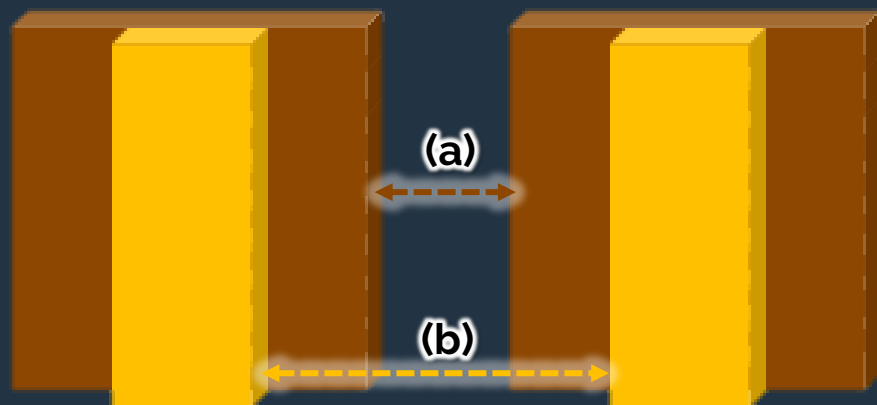
Strategy ②: ALD passivation



Nanomanufacturing: ALD Fundamentals, Eindhoven University of Technology.

Both plasma and ALD passivation offer viable dry etch strategies to mitigate CD loss, with distinct mechanisms suited for different pattern geometries and process requirements.

How Space Size Affects Pattern Integrity?



Smaller space features exhibit faster erosion rates, leading to pattern ratio distortion and increased risk of profile degradation.

Achievement

- **CD:** Achieved **L-S CD loss <5Å**
- **Methodology:** Identify optimal balance between **Descum** & **Trim** steps through DOE
- **Defectivity:** Determine **gas flow** is key factor of **L-S CD** & **defectivity** trade-off
- **Forward looking:** Good methodology for future planar DRAM scaling - How to **etch EUV-defined complex patterns**

