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Marvell Semiconductor Inc.

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Agenda

- **Introduction to 3DIC Physical Verification**
- **Challenges in 3DIC Physical Verification**
- **Unified 3DIC Physical Verification Flow**
- **Case Insights and Pilot Implementation**
- **Conclusion**

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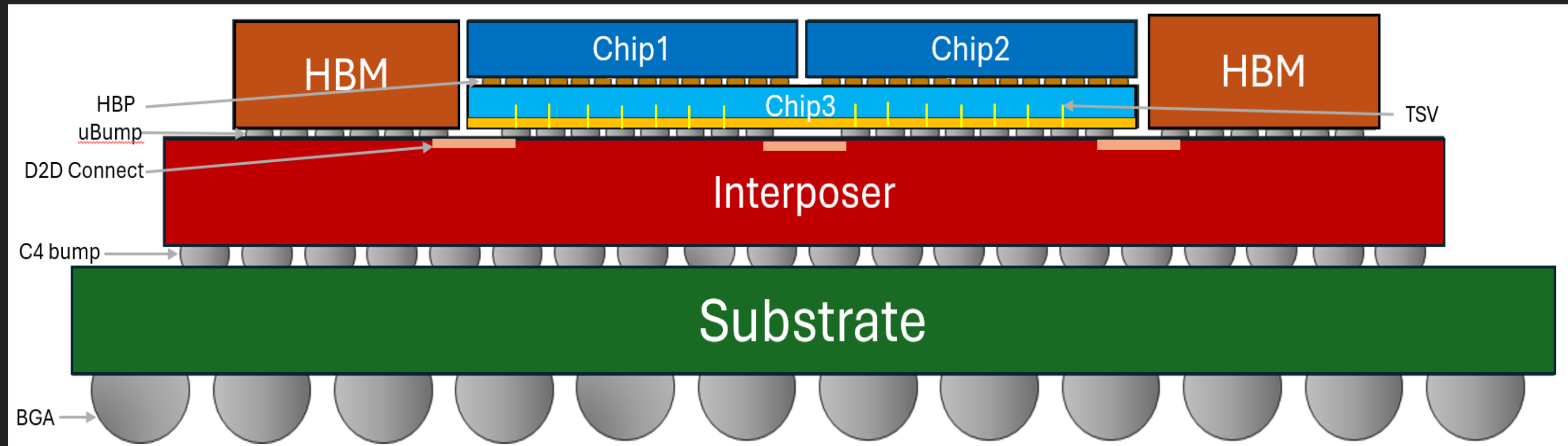
What is 3DIC

3DIC: Three-Dimensional Integrated

Key Components: SoC Chips, High Bandwidth Memory (HBM), Through-Silicon Vias (TSV), advance packaging

Key Benefits: Increased performance, improved power efficiency, heterogeneous integration, enhanced bandwidth

Applications: High-performance and compact designs



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Challenges in 3DIC Physical Verification

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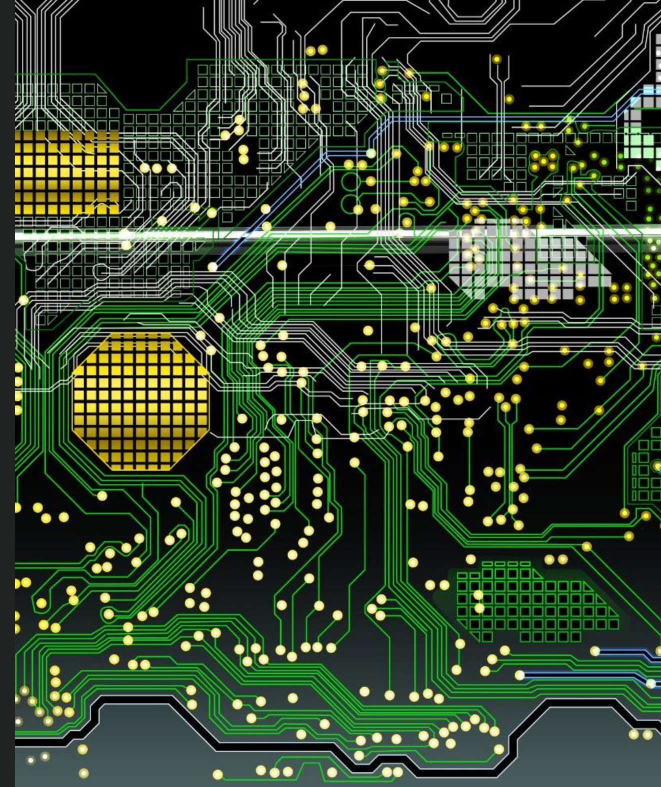
Why 2D Signoff Fails in 3DICs

Limitations of 2D Physical Verification

Complex Vertical Interactions

Undetected Failures in 3D Stacks

Need for New PV Methodologies



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Why 2D PV Breaks in 3D

CHALLENGE	DESCRIPTION
Heterogeneous Die Stacking	Different process nodes and foundries rule compliance
TSV and Micro-Bump Connectivity	Cross-die alignment and electrical consistency checks
Antenna Effect Analysis	New conductive elements, complex electrical paths
Seal Ring Insertion	Post-assembly insertion affects dummy pad visibility
Die Alignment Checks	Ensures hybrid bond pads are correctly aligned

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Build Unique and Unified Flow

Multi-Die Verification	Integrate multi-level checks DRC, LVS, antenna, and ESD checks.
Vendor-Neutral Verification	Ensure compatibility across different platforms and technologies
Automated Verification	Streamline verification and reduce manual errors.
Early Issue Detection	Reduce late-stage failures and improve reliability

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Unified 3DIC Physical Verification Flow

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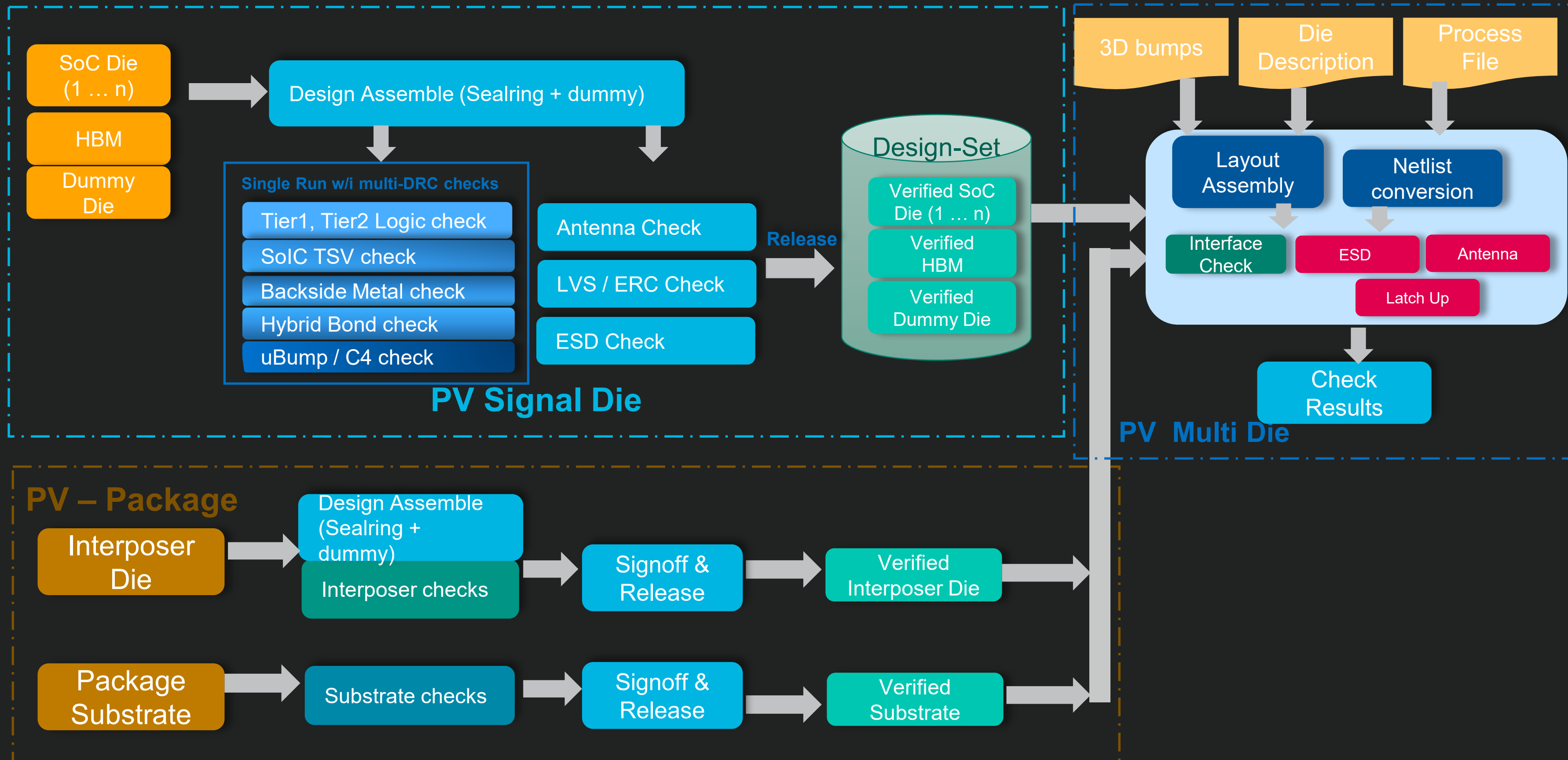
Unified Physical Verification Flow



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Seal Ring and Dummy Pad Strategy

- **Seal Ring Importance**

Provide the crucial mechanical protection and environmental isolation.

- **Dummy Pad Challenges**

Complicate post-assembly assignment due to invisibility in P&R.

- **Automated Dummy Pad Generation**

Auto-generate DRC-compliant dummy HBPs, enable early interface alignment checks.

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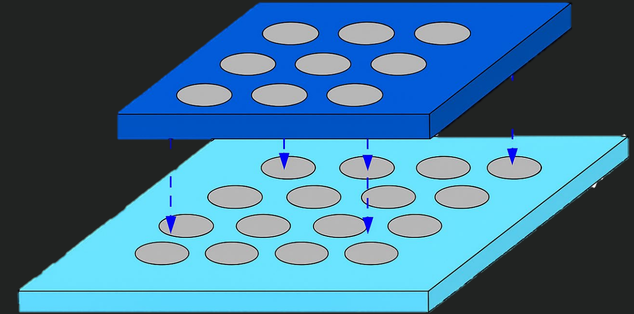
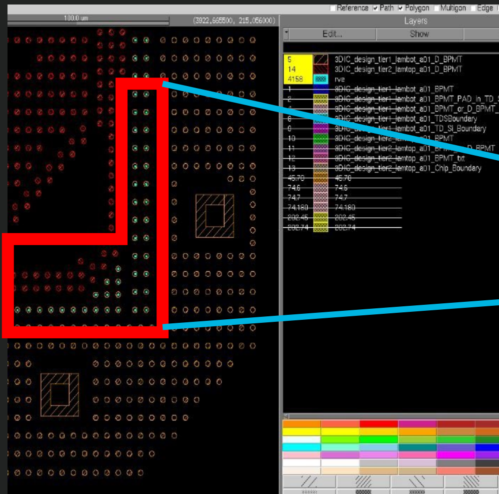
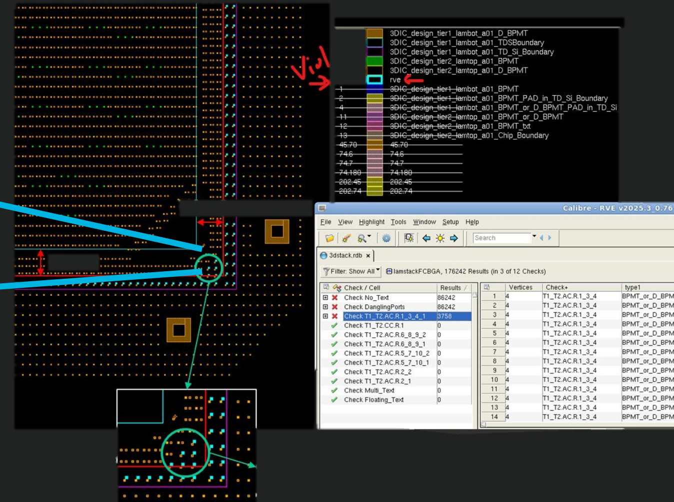
3D Connectivity flow

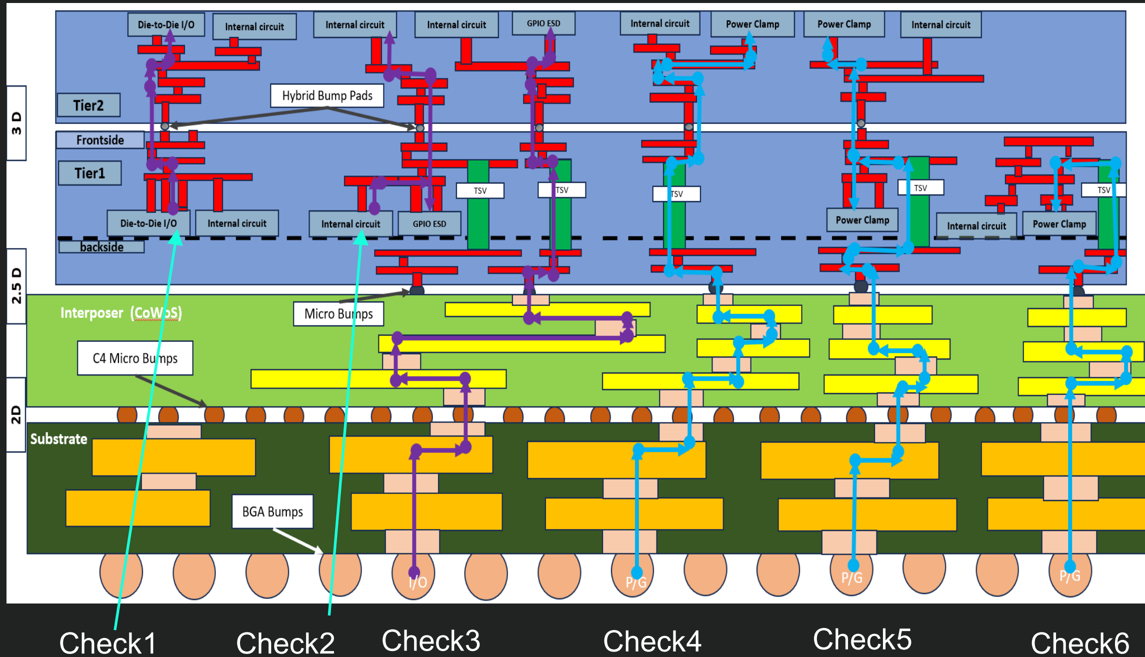
- Validate bump alignment between stacked dies
- Ensure TDS boundary layer alignment
- Verify bump connectivity and perform LVS







Electrical 3D ESD Verification



Check1 Check2 Check3 Check4 Check5 Check6

Overall Goal : Check all the possible ESD Paths from the substrate to all the ESD Cells inside dies

- **Check1**: Connectivity from on hybrid bond to its facing counterparts
- **Check2**: Micro-bump die-to-die signal pad
- **Check3**: IO signal bump to GPIO ESD
- **Check4**: Power / Ground bump to Tier2 power clamp cells
- **Check5**: Power / Ground bump to both Tier1 and Tier2 power clamps
- **Check6**: Power / Ground bump to both Tier1 power clamps

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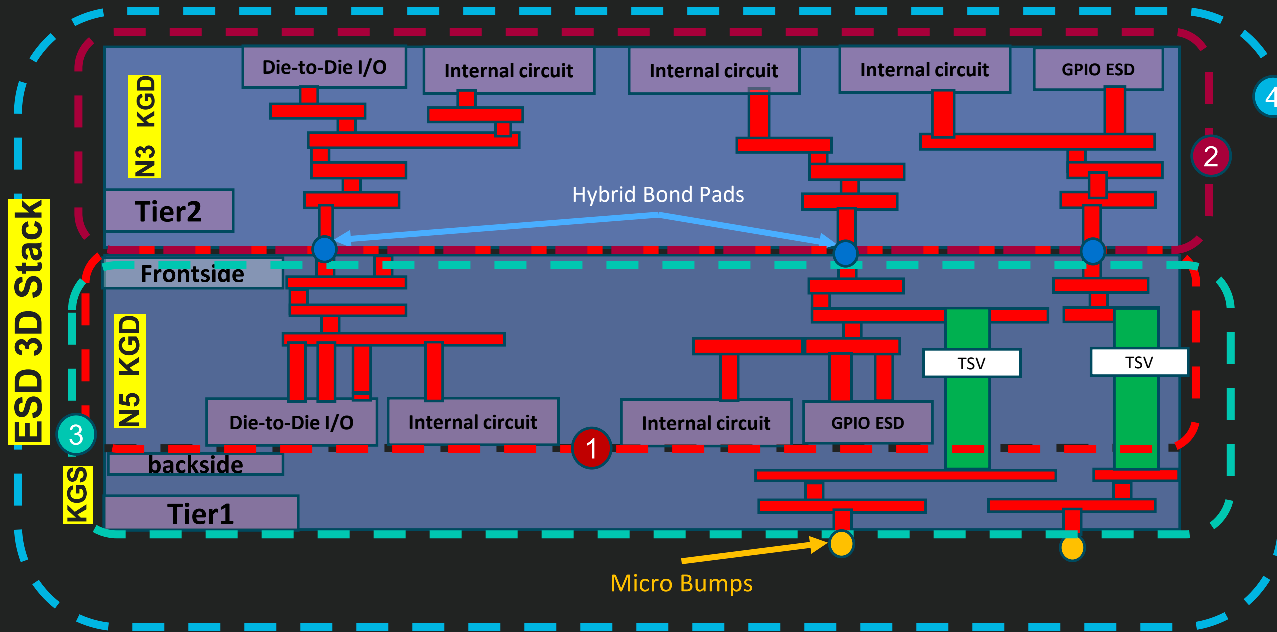
ESD Challenges



- **Tool Performance Challenges**
- **SoIC™ Bottom Die Dual-mode Verification**
- **ESD Check Job Overhead**

Die-to-Die I/O: Input/Output interface for high performance, low-power D2D communication

KGD (**K**nown **G**ood **D**ie) : Check ESD w/o backside metal

KGS (Known **G**ood **S**tack**) :** Check full GPIO and ESD clamp w/I backside metal

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Generalized Runtime Performance

Full Chip- SOIC Tier1	**Runtime (KGD)**	**Runtime (KGS)**	**RESOURCES**
Topology (*TOPO*) Check	3 hours	2.9 hours	48 cores
Logic Driven Layout (*LDL*) Check	2.5 hours	2.5 hours	48 cores
Current Density (*CD*) Check	6.2 hours	6.2 hours	16 cores
Point to Point (*P2P*) Check	**39 hours**	6.5 hours	**240 cores**

SoIC Tier1 Bottom Die:
9 Power Domains
1 Ground
\> 24000 D2D Signal nets
\> 100 I/O Signal nets

Full Chip- SOIC Tier2	**Runtime**	**RESOURCES**
Topology (*TOPO*) Check	1.5 hours	48 cores
Logic Driven Layout (*LDL*) Check	1.6 hours	48 cores
Current Density (*CD*) Check	1.8 hours	48 cores
Point to Point (*P2P*) Check	**41 hours**	**240 cores**

SoIC Tier2 Top Die:
9 Power Domains
1 Ground
\> 24000 D2D Signal nets

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3D PERC ESD Result

ESD Power Clamp Cell

ESD Power Clamp Cell

BGA Ball

Hybrid Bond

Results for SoIC™ Standalone

Results for SoIC™ + Substrate

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Conclusion

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Conclusion

- Adopt new PV strategies to manage 3DIC complexity
- Build a unified framework for die, package, and stack verification
- Shift verification left with standards-driven practices
- Align signoff across all integration layers
- Advance modeling for 3D antenna and ESD effects
- Collaborate across design, packaging, and verification teams

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Thank You

3DIC is the future of semiconductor innovation

Together, we can make something amazing happen!

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