



Strategic Shifts in Semiconductor System Design

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Agenda

- The Chiplet Revolution from vision to today
- Industry Case Studies
- Silicon and Package Technologies
- “One More Thing”

The Chiplet Revolution

Moore's Predicted "Day of Reckoning"

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected¹."

-Gordon E. Moore

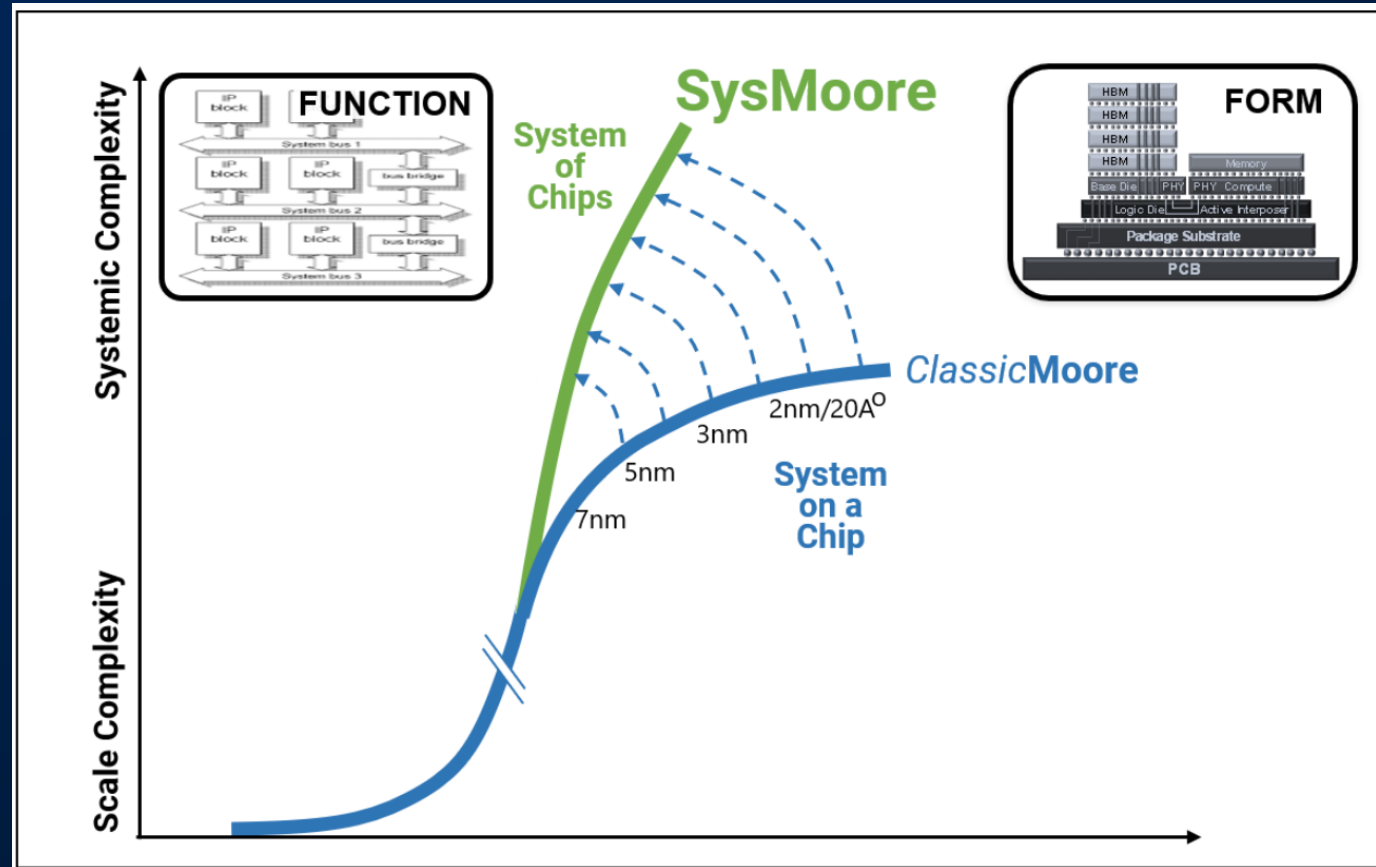


Image: Intel®

¹: "Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965

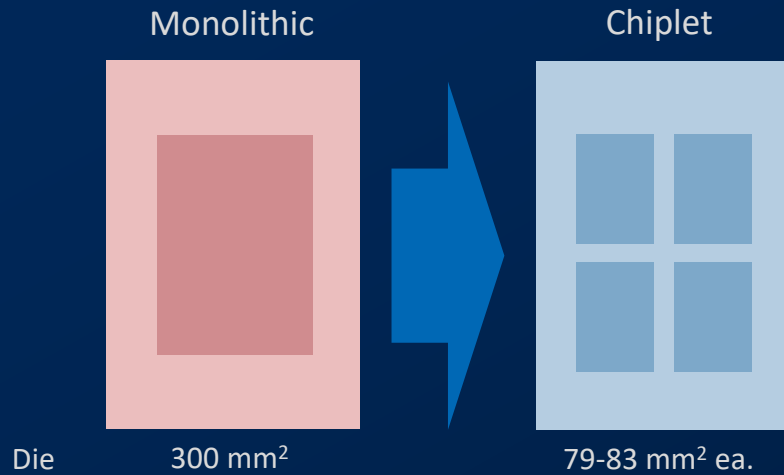
System on Chip -> System of Chips

“Catalyzing the Impossible: Silicon, Software, and Smarts for the SysMoore Era” – Dr. Aart de Geus



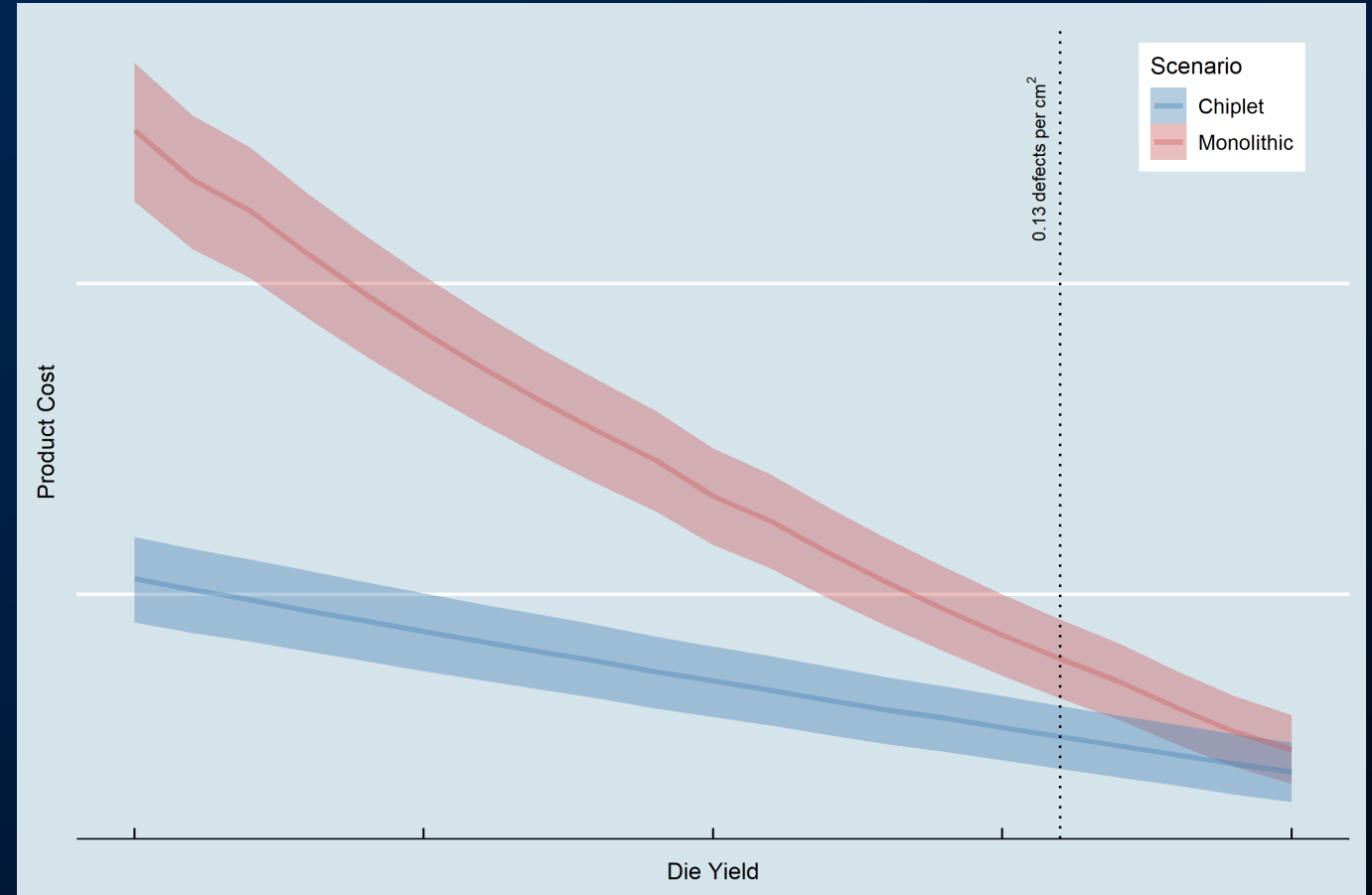
Source: Synopsys, <https://www.synopsys.com/glossary/what-is-sysmoore.html>

Motivation : Cost & Manufacturing Optimization



Input Variables:

- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead

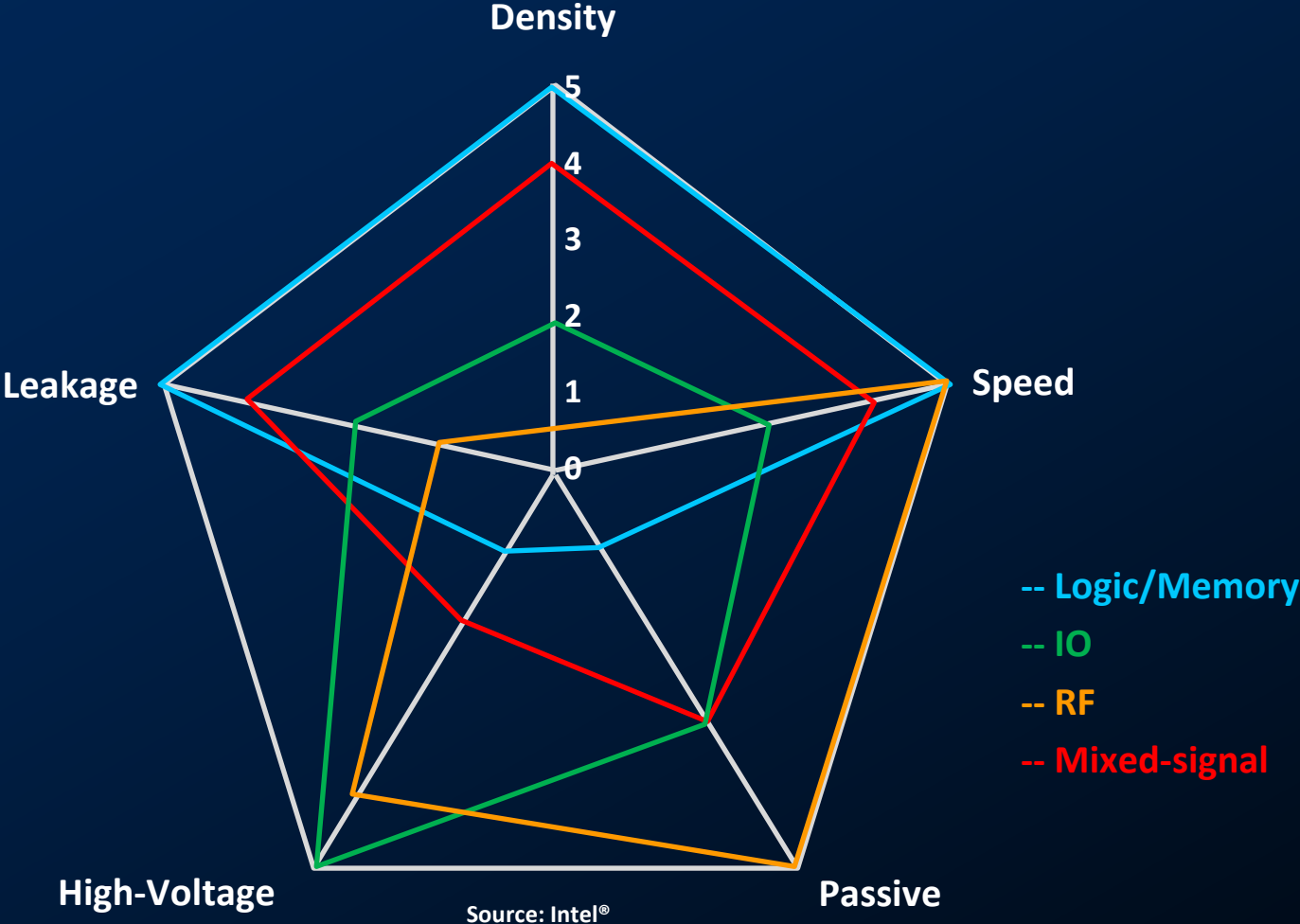


*Probabilistic trend by 1std dev

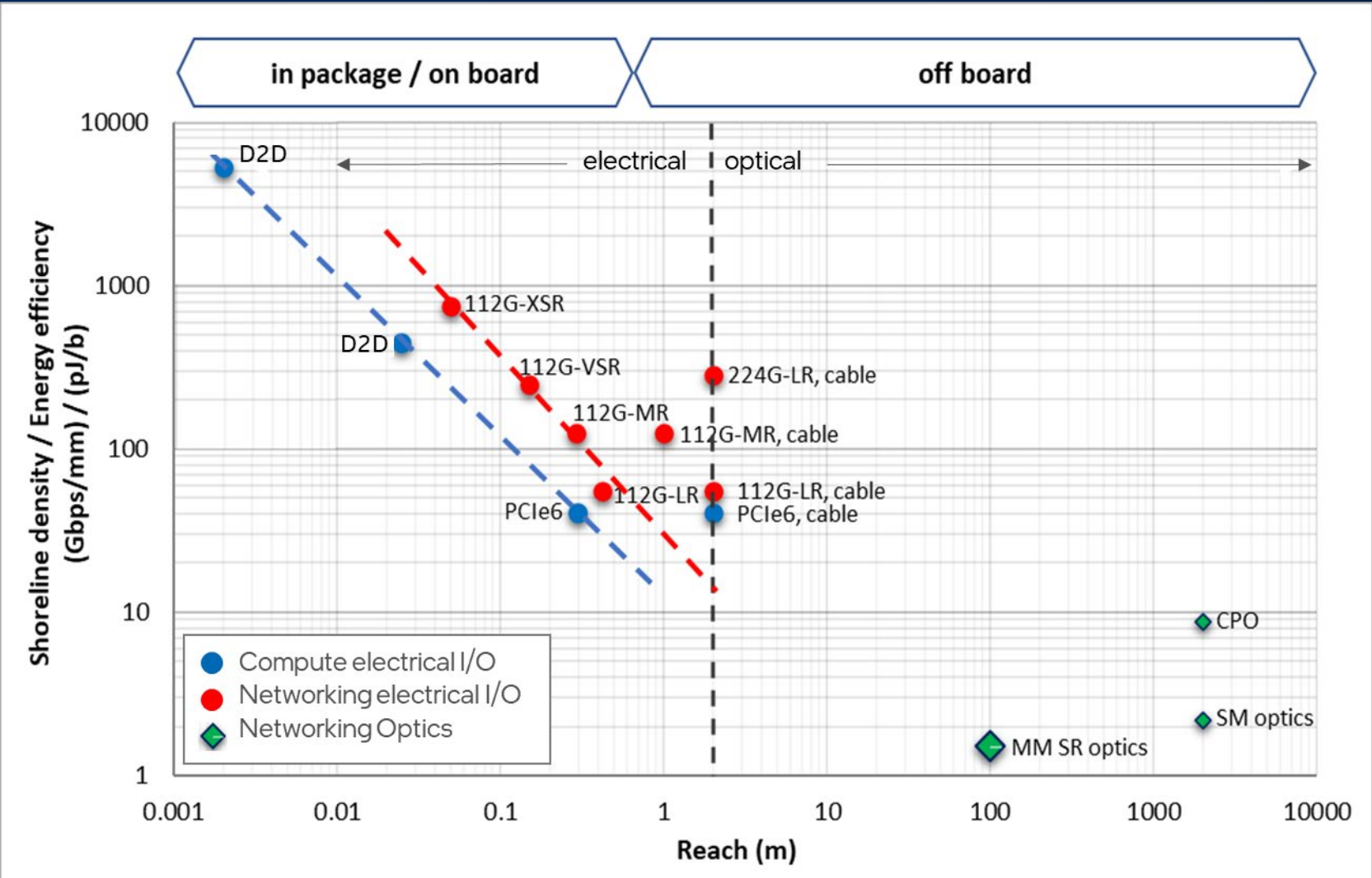
Source: Intel® Model

Reference: <https://ieeexplore.ieee.org/document/9758914>
"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

Motivation : Process Technology Optimization

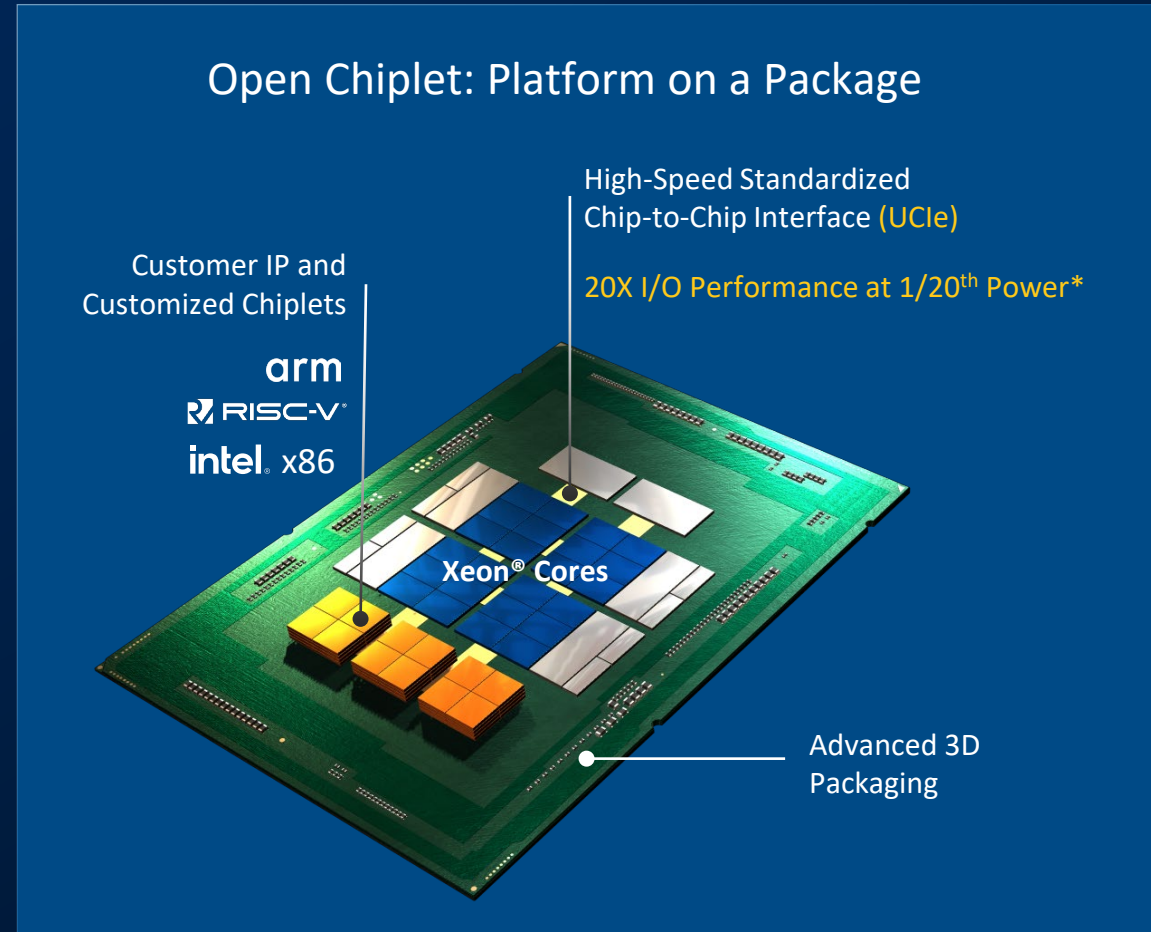


Motivation: Optimize System Level High Speed IO



Source: Intel®

Intel® Vision 2022 : The “Chiplet Revolution”

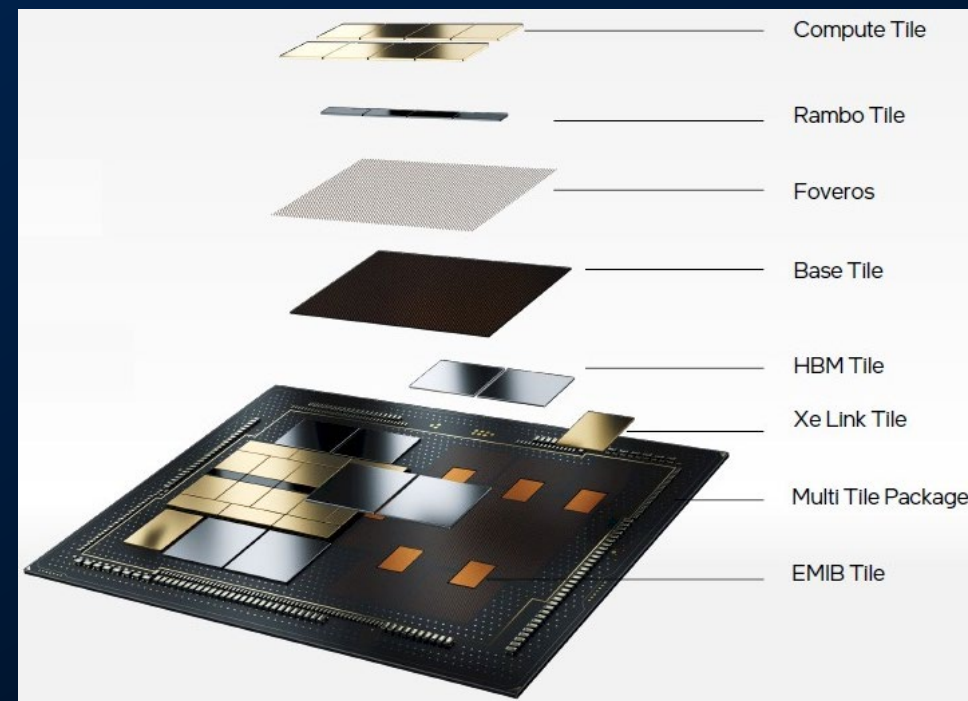
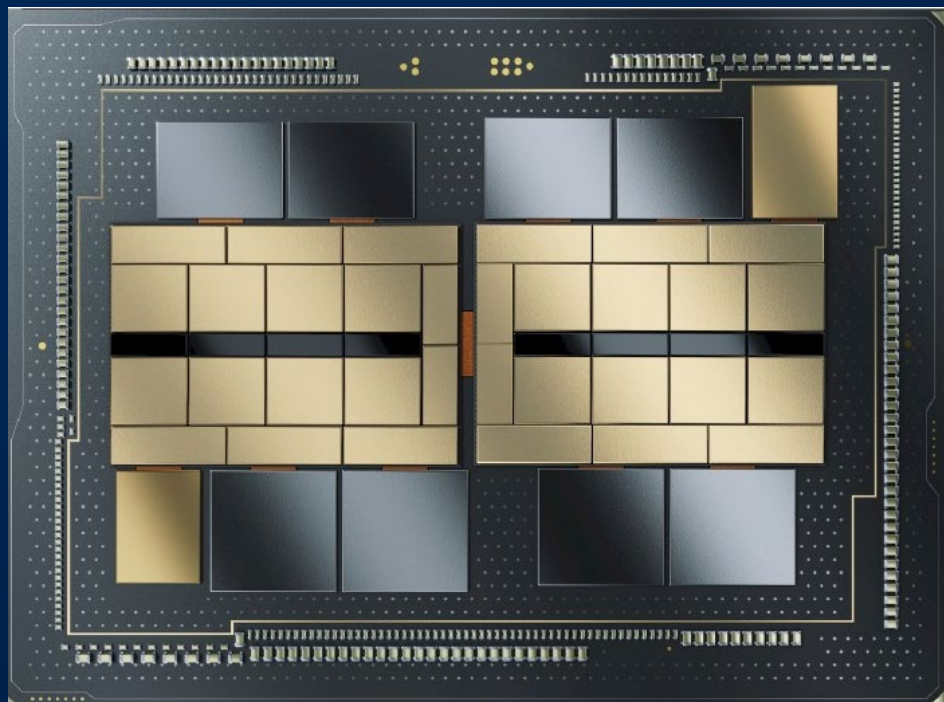


*relative to PCIe G5 x16

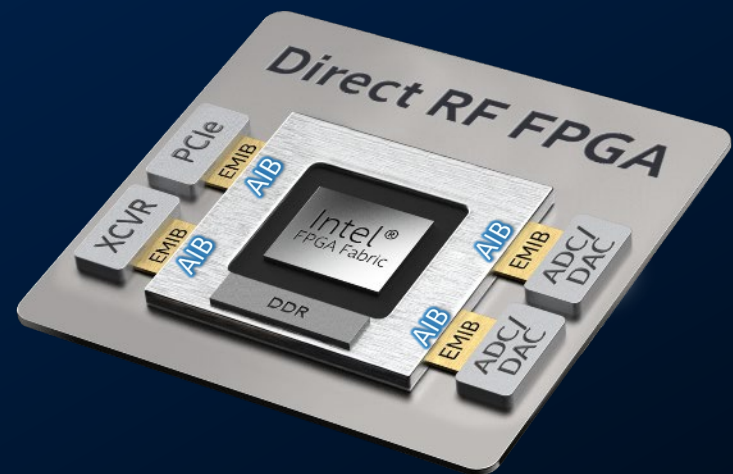
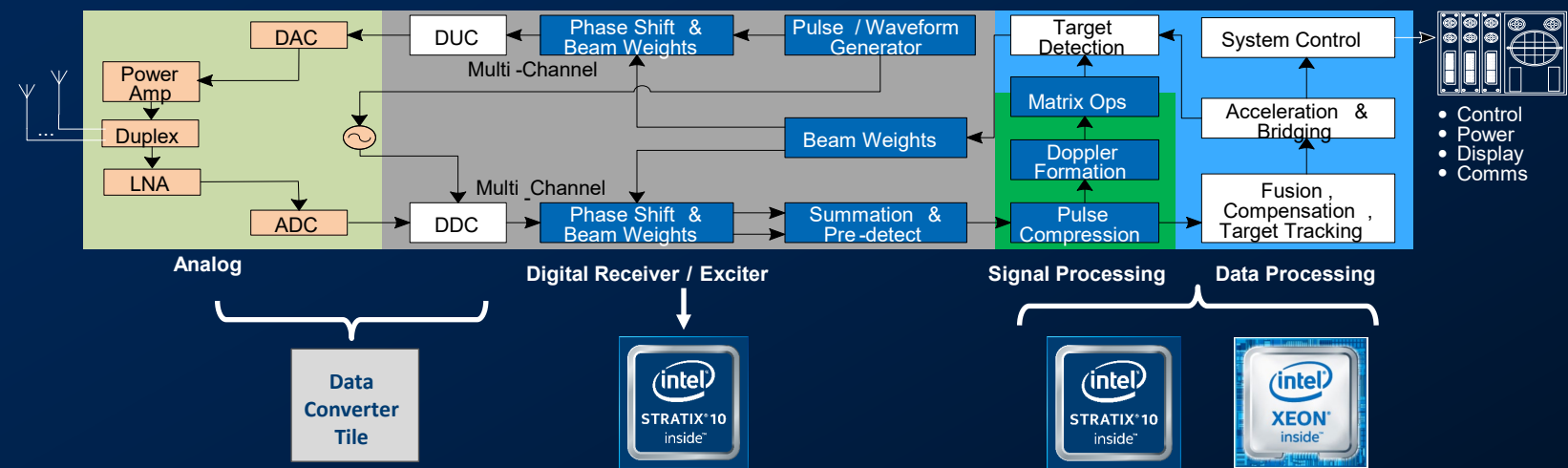
Industry Case Studies

Case Study : Intel® HPC - Ponte Vecchio

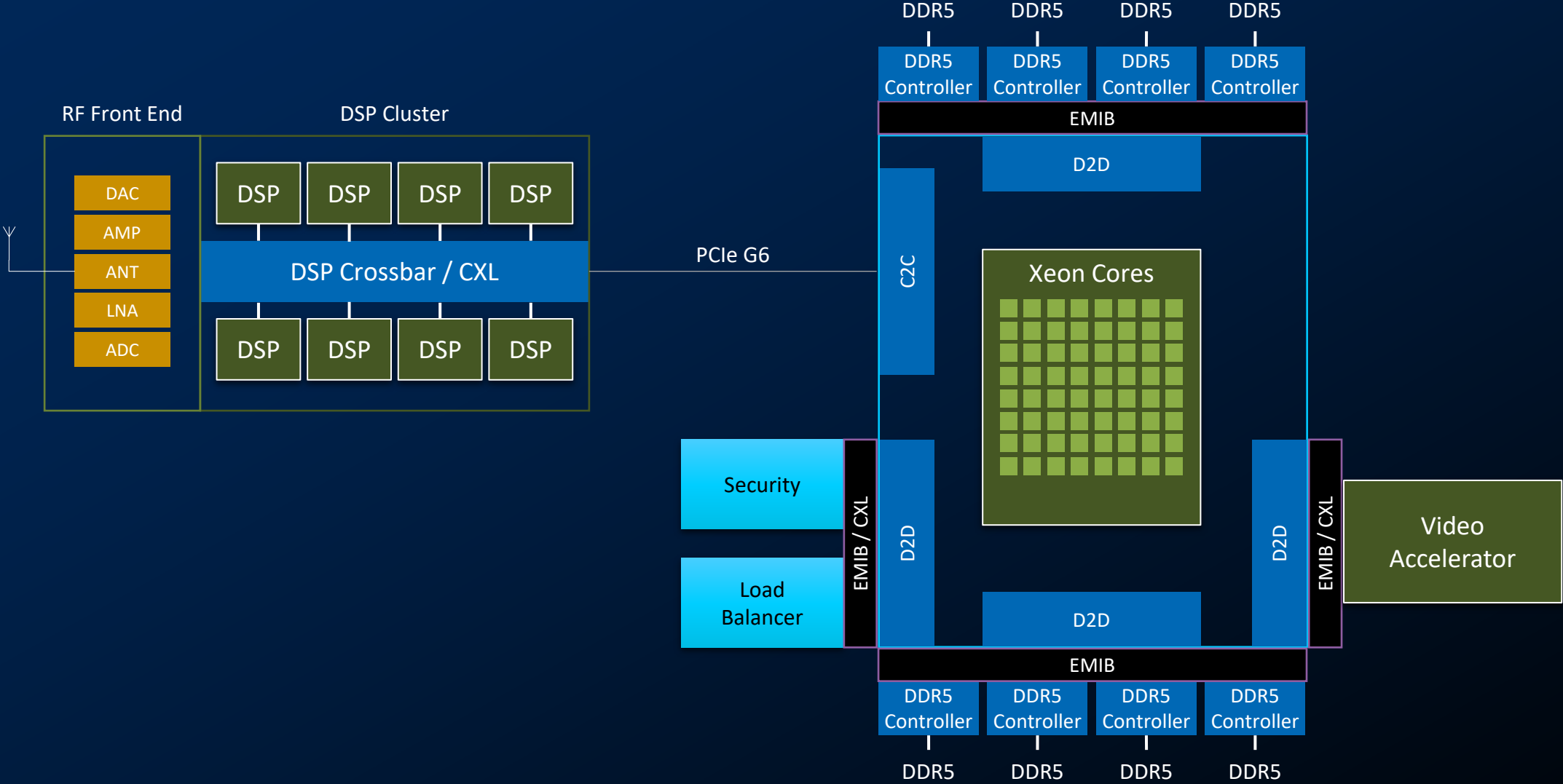
Ex. Complexity Management, Process Optimization



Sensor Case Study: Radar Beamforming Application

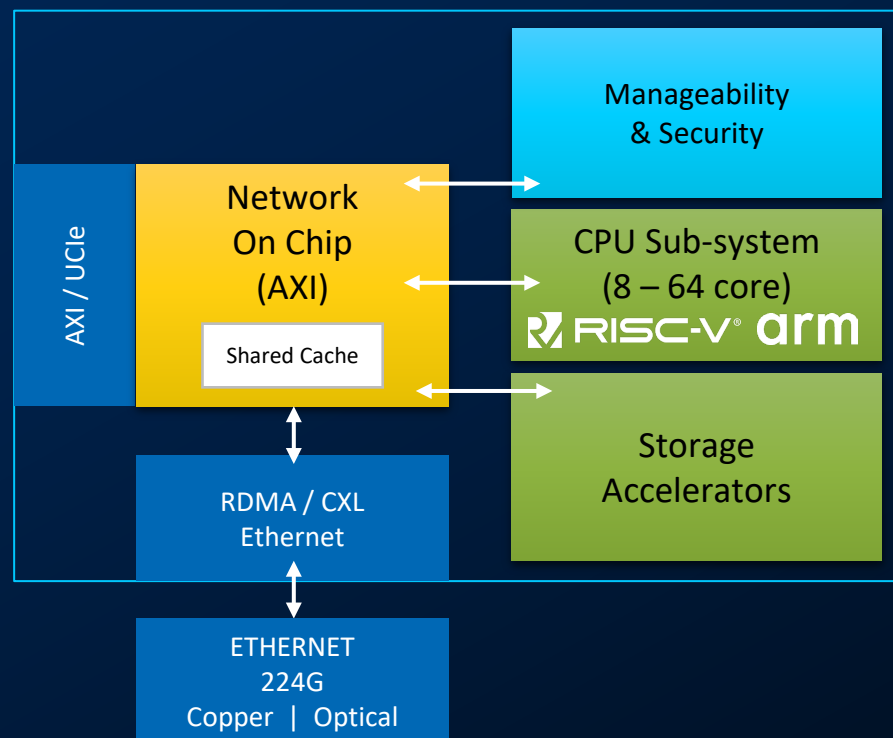


Telco Repartitioning (5G, 6G)



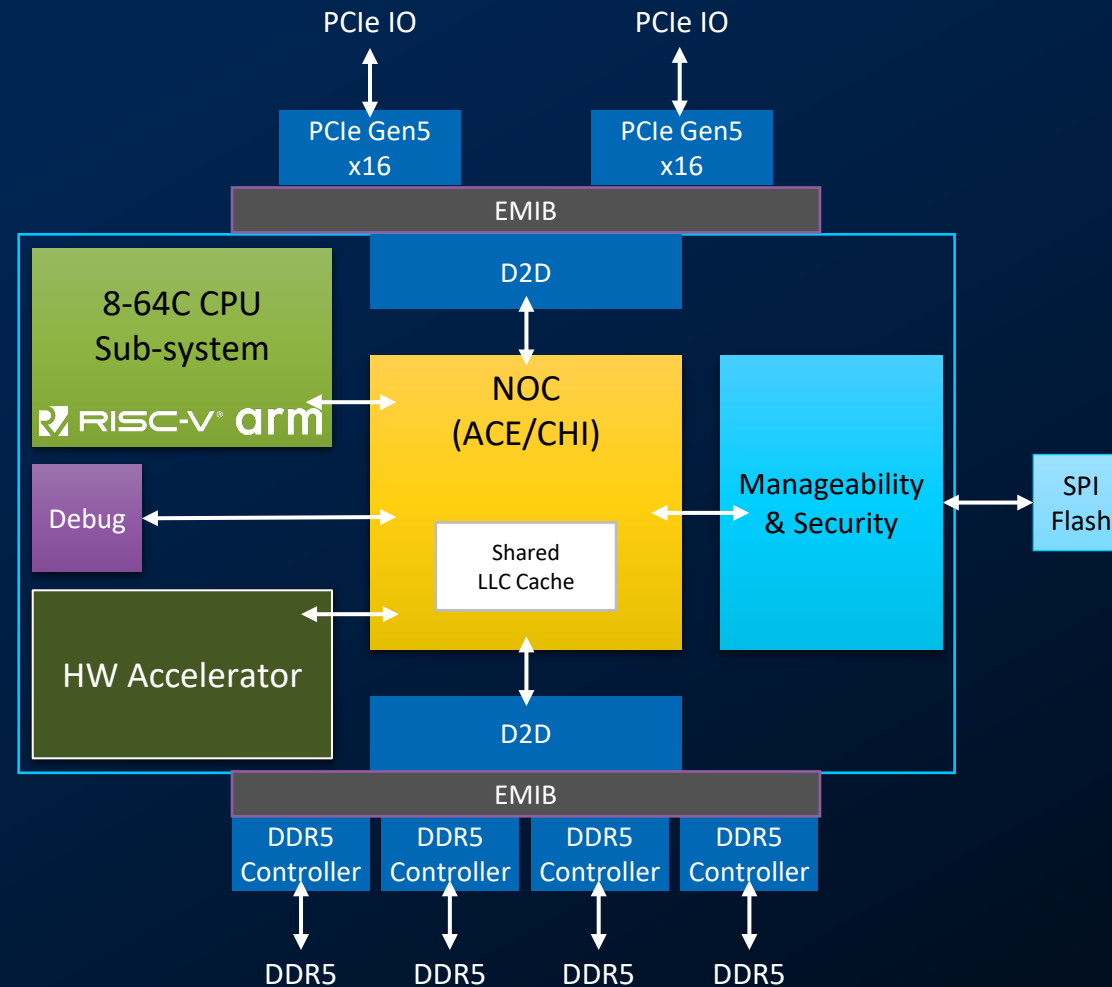
Networking/Storage Case Study: IPU/DPU

Ex. Multi-Protocol Architecture : AXI/UCle ; Networking Modularity

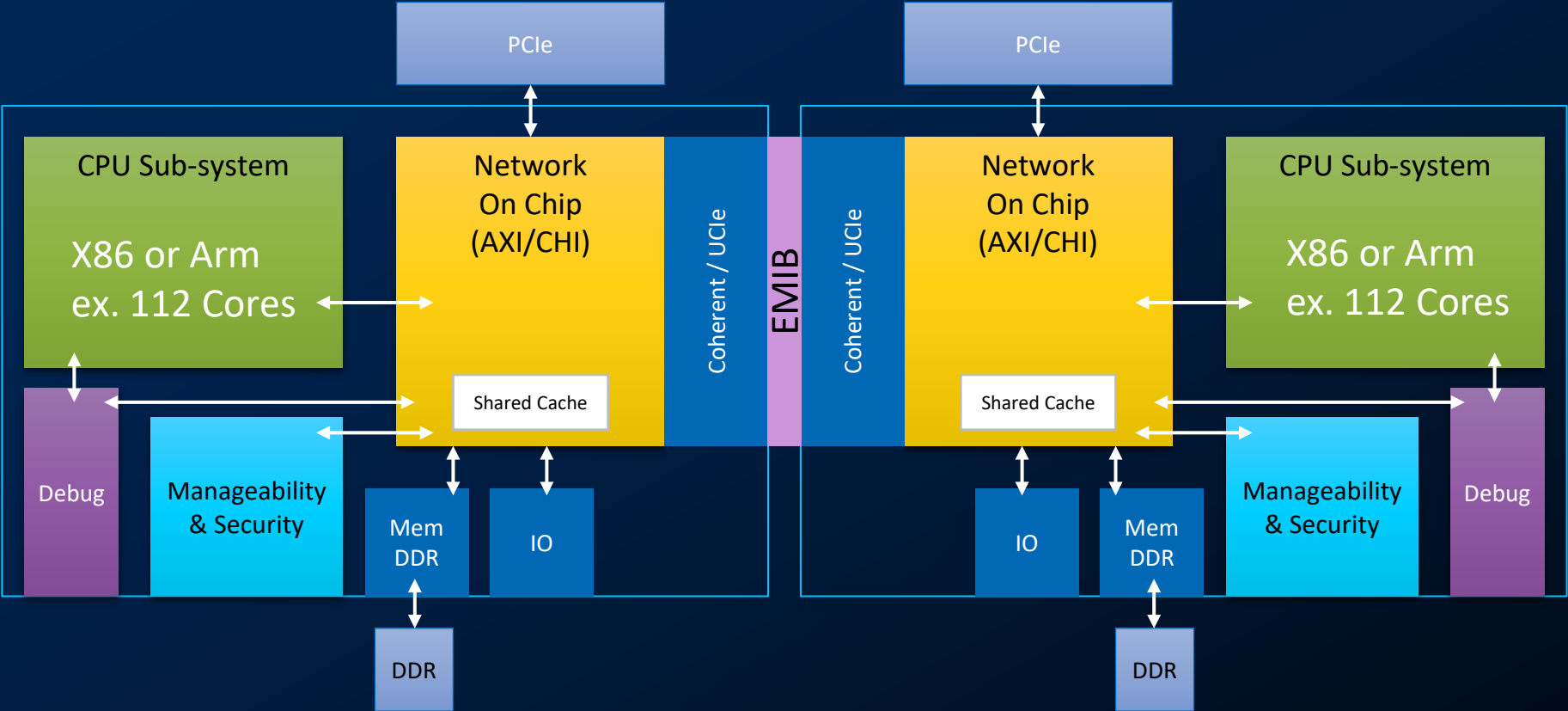


IO Case Study: Disaggregated PCIe & Memory

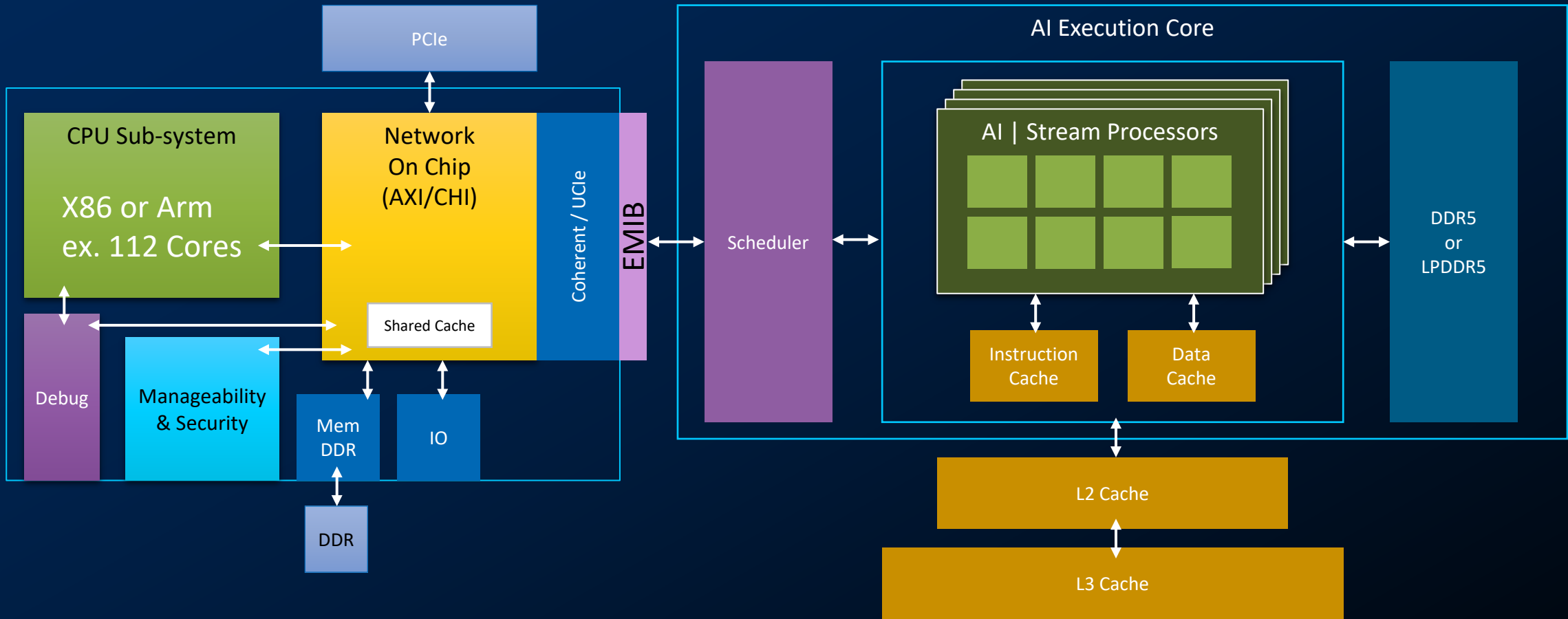
Ex. Optimization of Process (ex. Analog), Supply Chain



Server –Server Chiplet Architecture Example



Server – AI Inference Example

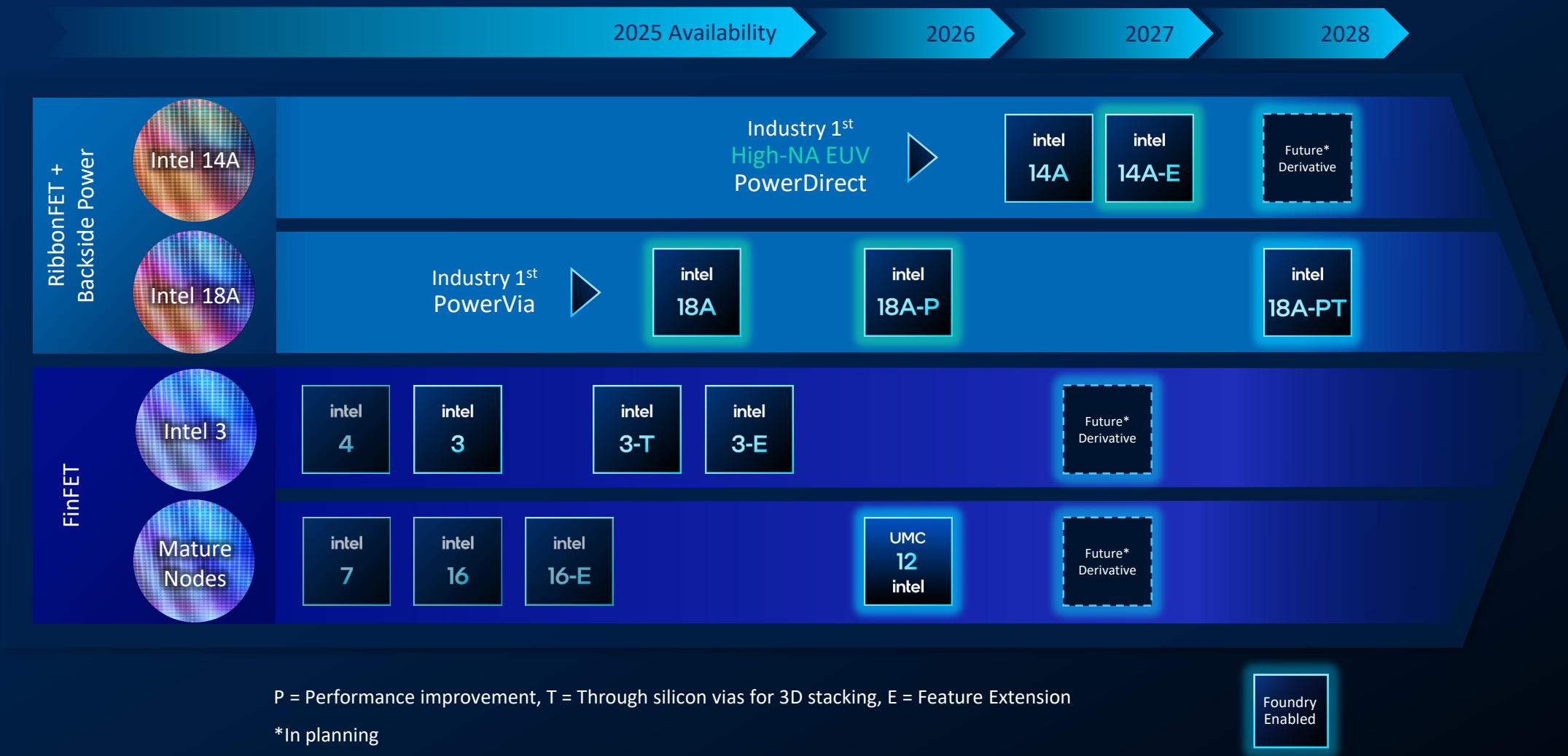


Silicon and Package Technology Needed

Systems Foundry for the AI Era



System of Chips Starts with Leadership Silicon



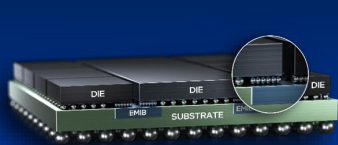
All product and service plans, roadmaps, and performance estimates are subject to change without notice.

Brought together by Advanced Packaging

EMIB

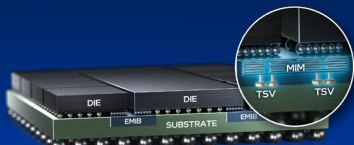
EMIB-M 2.5D

Provides highest density of compute with a lower cost



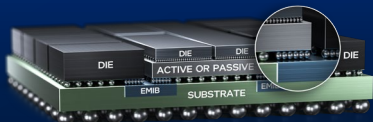
EMIB-T 2.5D

Addition of TSVs for die to HBM4 stitching



EMIB 3.5D

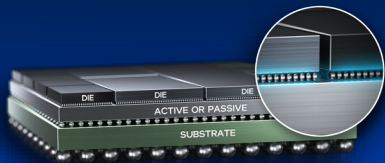
Enables flexible heterogeneous systems for complex products



FOVEROS

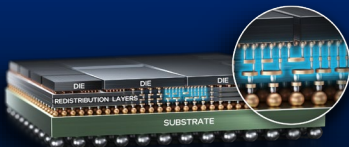
Foveros-S 2.5D

Disaggregation supporting high speed I/O with a smaller die complex



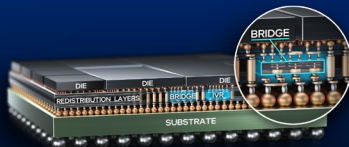
Foveros-R 2.5D

RDL based interposer for reduced cost



Foveros-B 2.5D

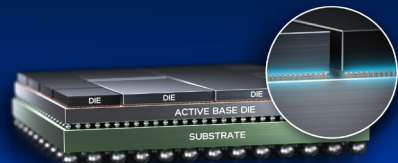
Si bridge interconnect for design flexibility & IVR /MIM integration



FOVEROS DIRECT

Foveros Direct 3D

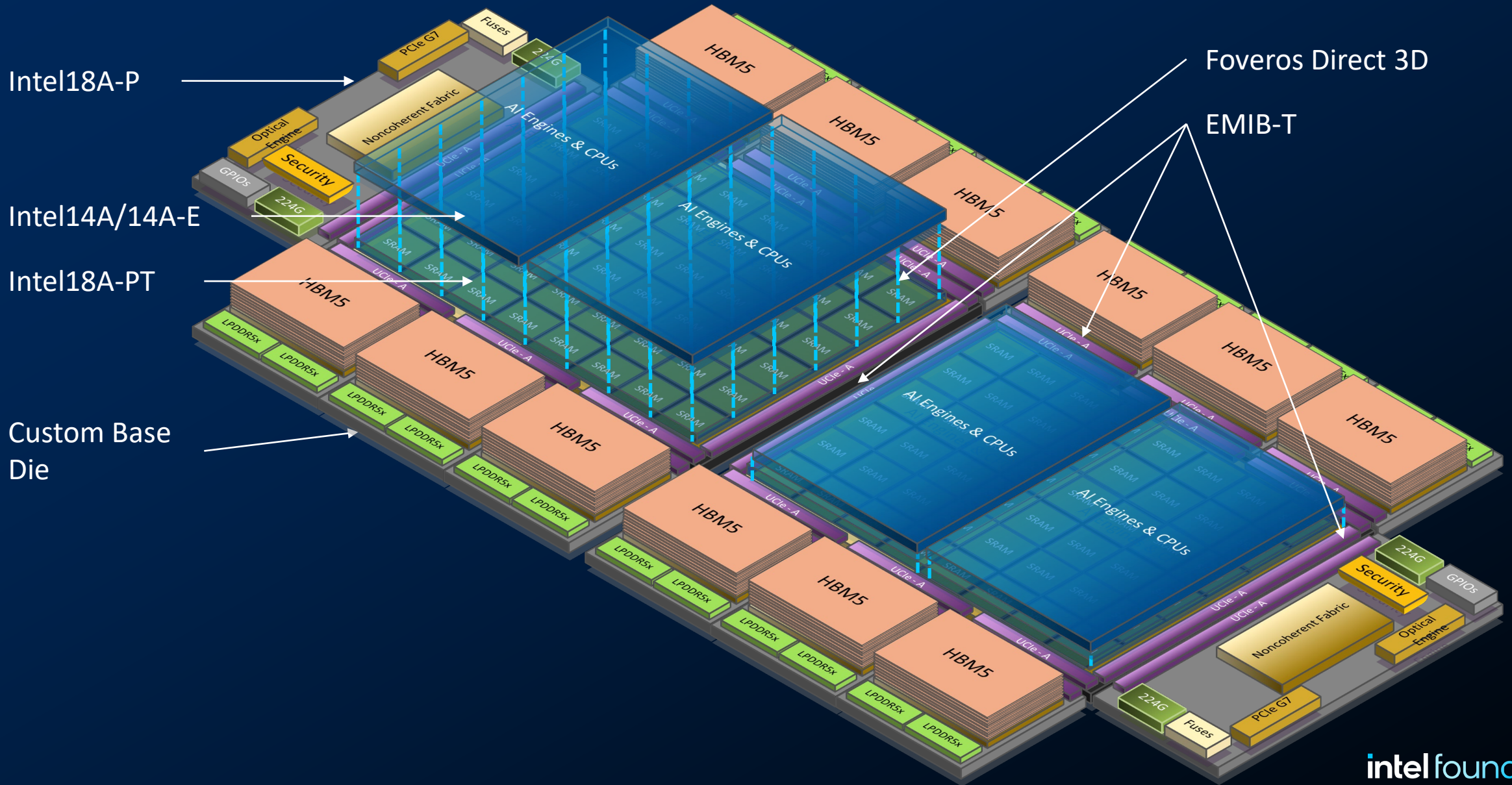
Ultra-high bandwidth and low power interconnect for superior performance



One more thing...

Pulling it all together

AI System of Chips



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