Propelling AI forward through Advanced Packaging Creativity

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AI IS HERE

HEALTHCARE

TELECOMMUNICATIONS

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FINANCIAL SERVICES

- AI applications permeating global life, creating new efficiencies and new markets, from data center to edge devices.
- AI economy projected to soar from $189 billion in 2023 to $4.8 trillion by 2033 – a 25-fold increase in just a decade
- AI adoption could boost global GDP by 15% by 2035, based on game-changing capabilities and safe deployment.
- Unprecedented data generation is driving global datasphere trajectory towards 200ZB by 2030

Source: UN Trade and Development (UNCTAD), PwC, IDC 2025

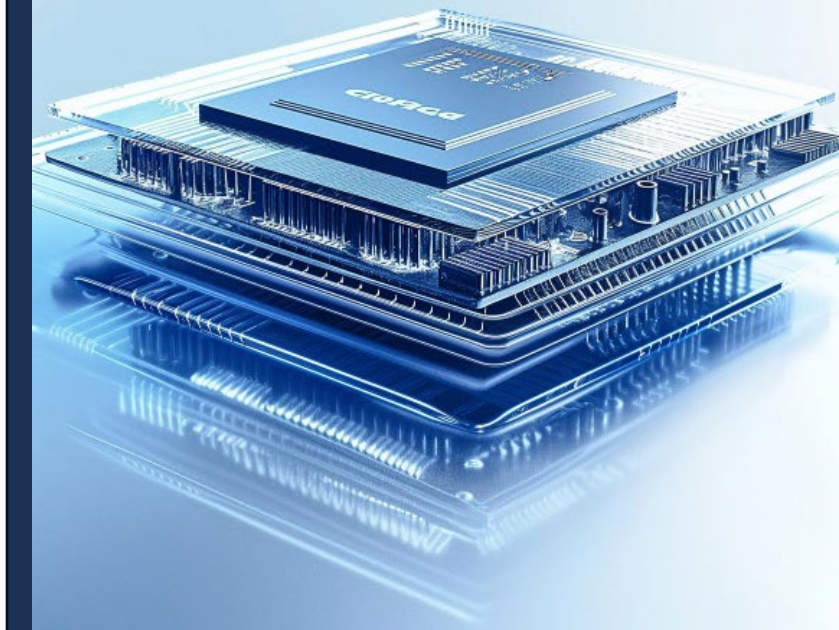
Semiconductor industry scaling

The AI innovation ecosystem is driving the global semiconductor market with demand for:

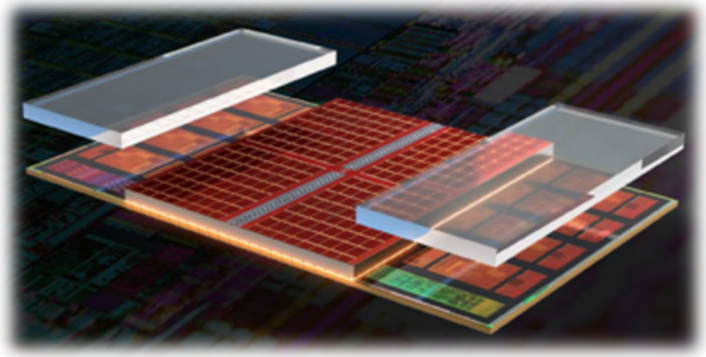
- New equipment
- New materials
- New architecture

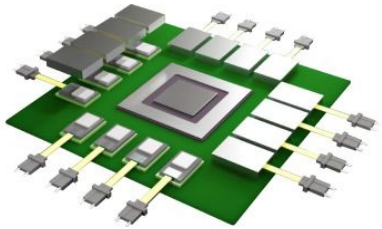
Advanced Packaging is bringing transformative innovation to address critical thermal and electrical challenges

- Heterogenous integrated solutions
- Power management devices
- Co-Packaged Optics



Advanced Packaging Delivers Holistic System Level Efficiency





Silicon and Si Stacking

Application

Packaging

Optical Interconnect

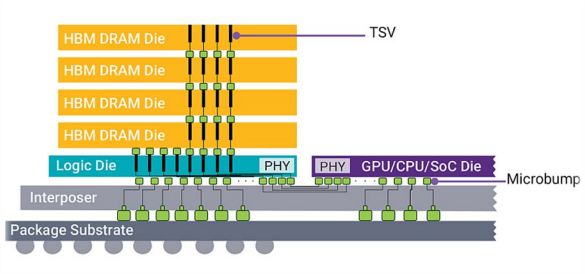
Energy efficiency through holistic design

Compute

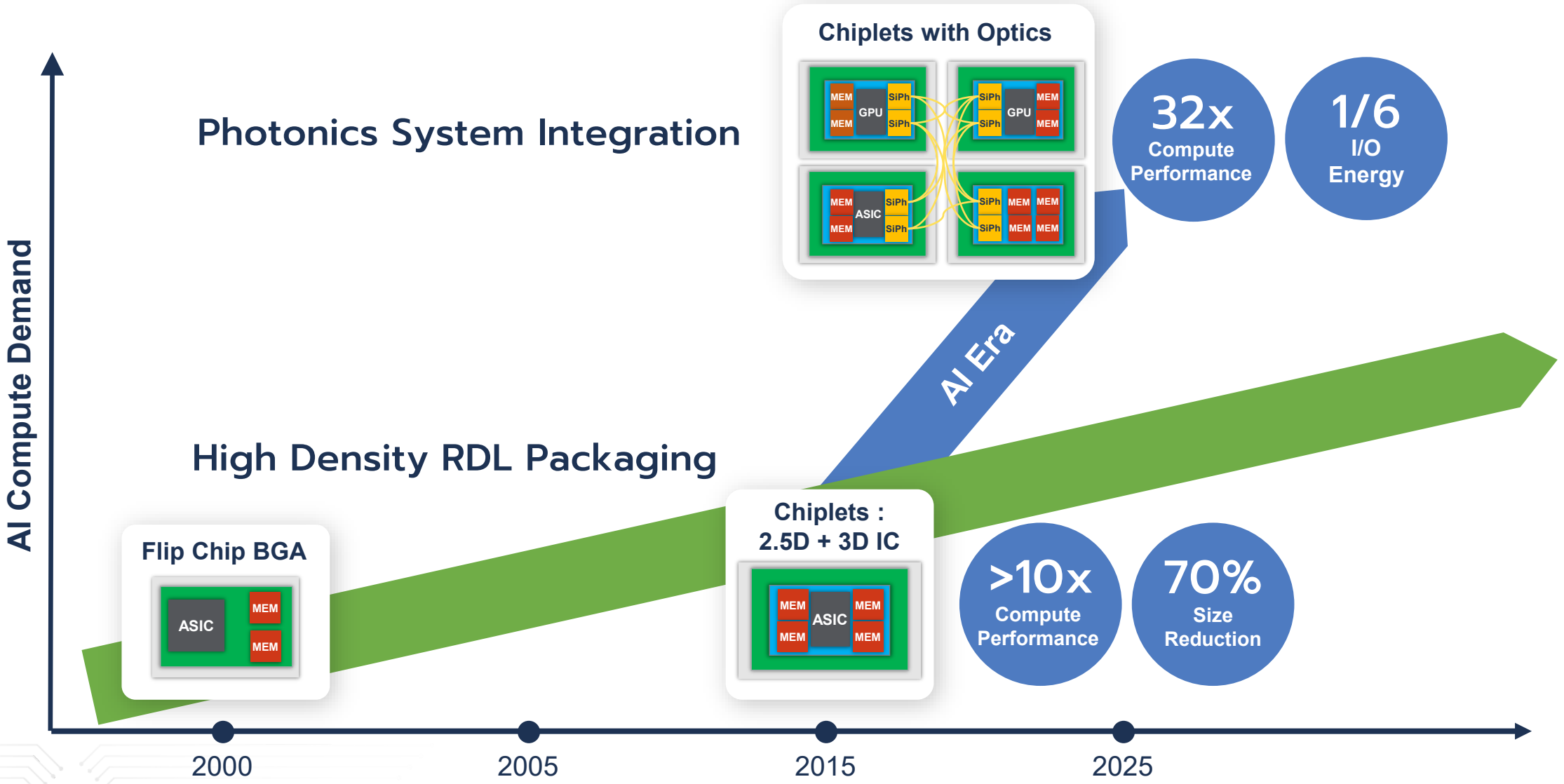
Software Stack

Memory

Accelerators



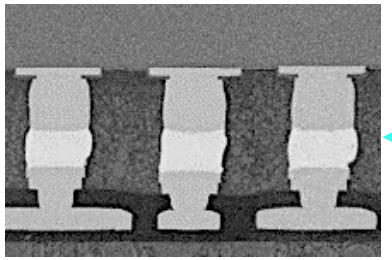
Packaging evolution for AI systems



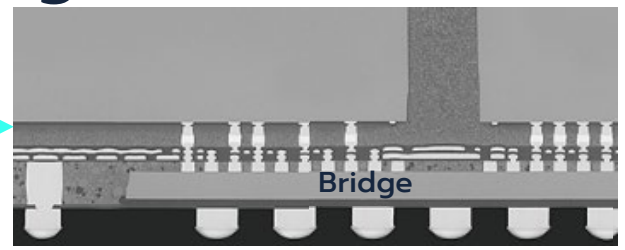
Exploring FOCoS & FOCoS-Bridge

FOCoS

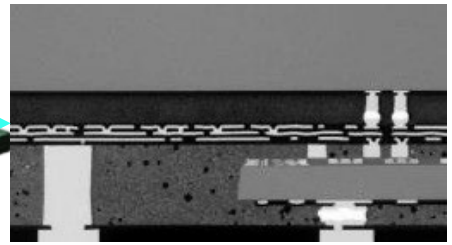
FOCoS-Bridge

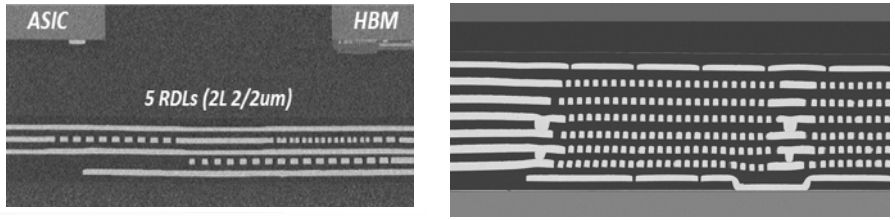


CoW uBump



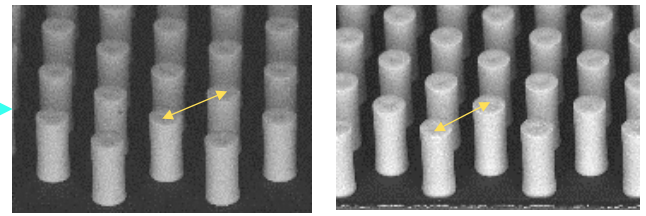
RDL Interposer with Embedded Bridge





RDL Interposer

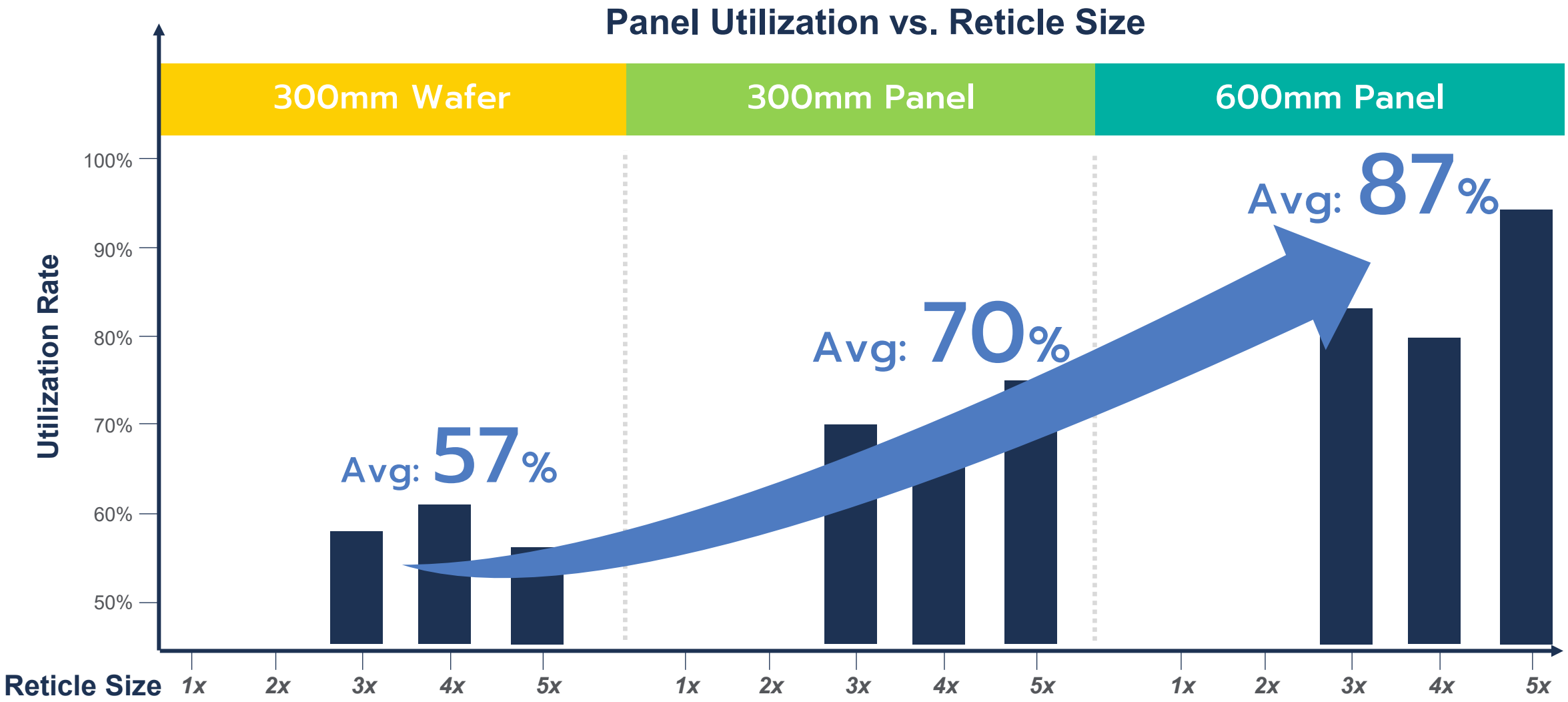
C4 bump pitch



150um

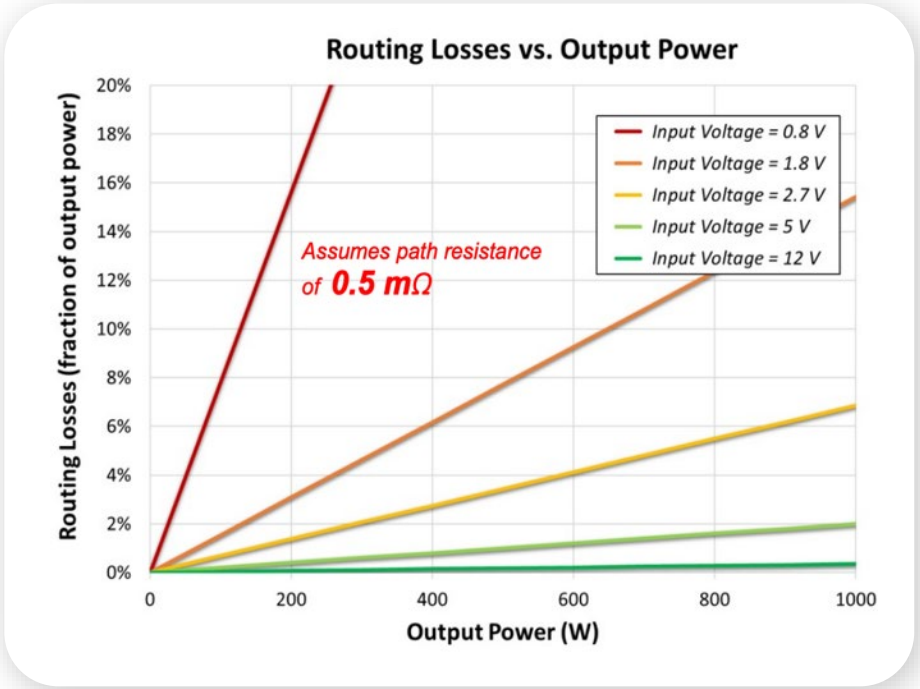
130um

Panel utilization



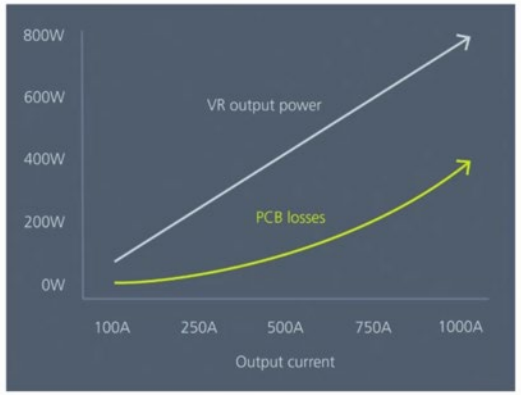
The need for IVR/VRM

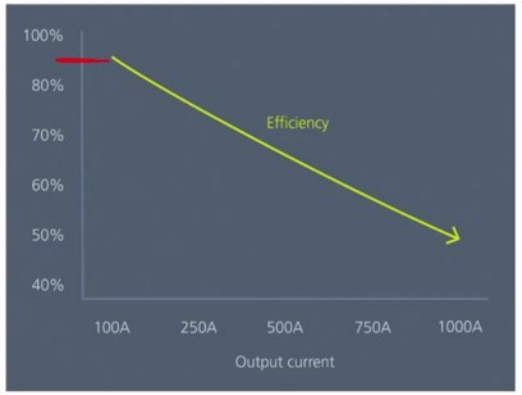
High power at lower voltages requires high current and causes high power delivery loss (I^2R) – Power delivery needs to be in short distance = vertical power delivery



Source: 2024 IEEE VLSI Symposium on Technology & Circuit

Escalating need to integrate power conversion from high voltage at point of load (PoL)
– integrate new power delivery architectures = Vertical power delivery





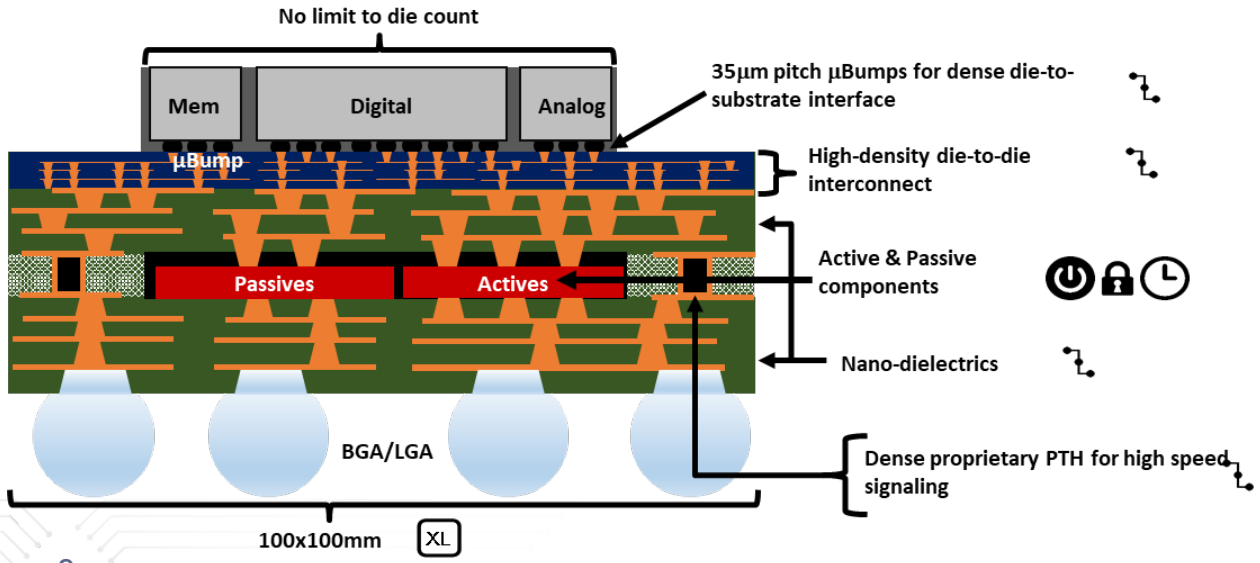
Example with PCB resistance of 400µΩ (VR at $0.8V_{OUT}$)

	Vicor Lateral	Conventional
PDN resistance	50µΩ	400µΩ
PDN loss @ 500 Amps	12.5W loss 96.8% efficiency	100W 75% efficiency
PDN loss @ 1000 Amps	50W loss 93.75% efficiency	400W 50% efficiency

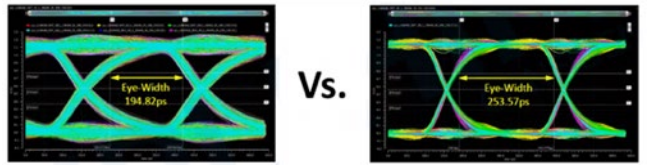
PDN Power Loss, due to circuit board copper resistance = I^2R

Power delivery innovation: Voltage Regulator Module

- PIM's cost & performance are better than after 7nm advanced node develop
- Decoupling frequency 100MHz ➔ 200MHz:
  - Clock & PHY VDD I/O 32% noise reduction
  - Driver VDD 78% noise reduction
- Voltage drop 179mV ➔ 119mV, 60mV improve could increase ~40% frequency
- Fast die-to-die interconnect and lower power via 30% wider eye

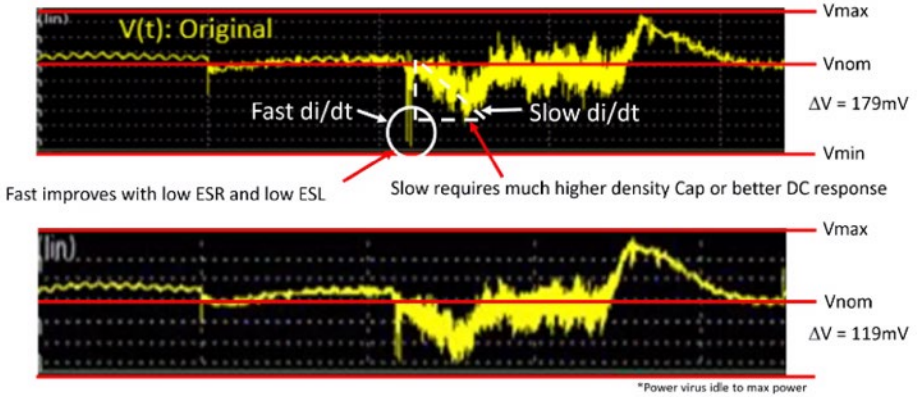


Better HBM Signaling

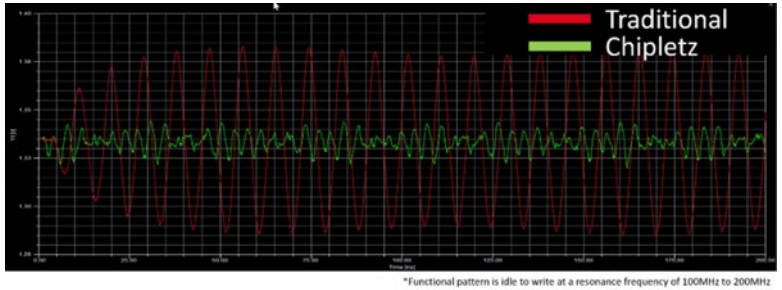


Silicon interposer Organic substrate

32% noise reduction



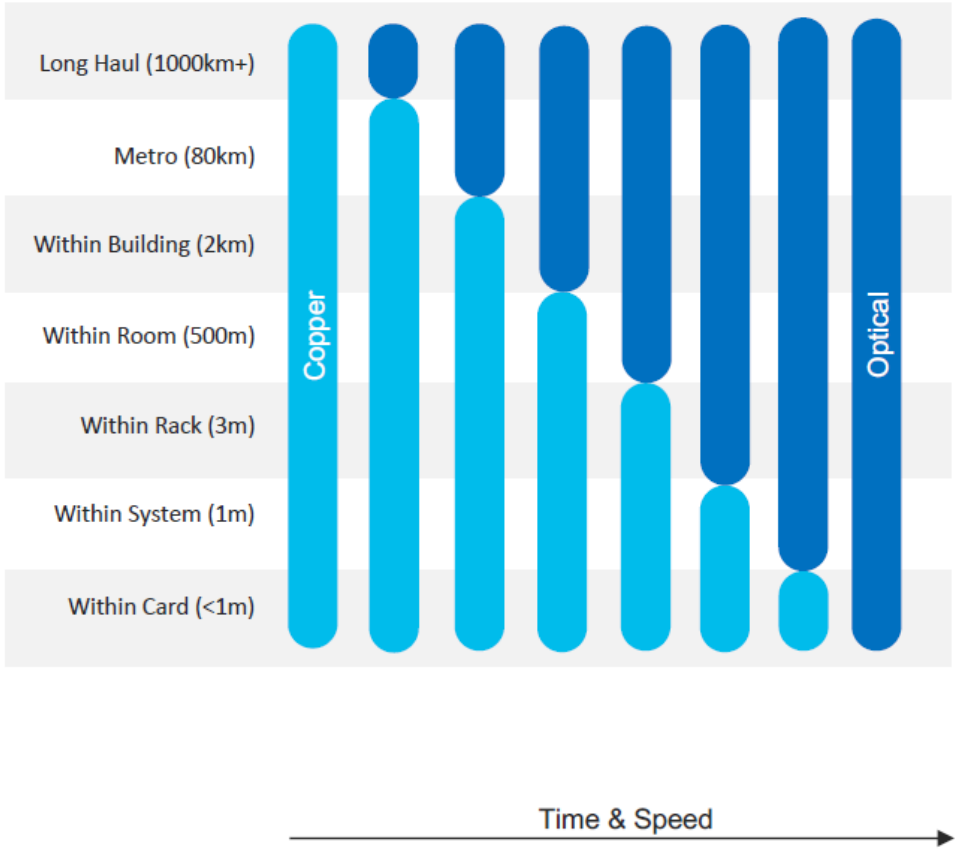
32% noise reduction in I/O



The future is optical

Future system capacity will only be possible with Silicon & Optical Integration

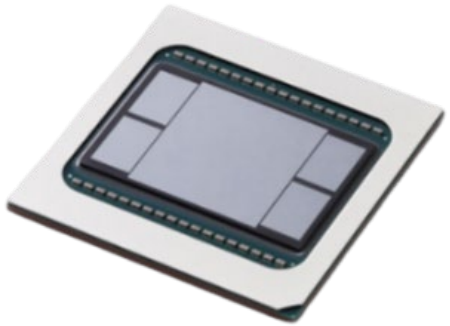
Si Silicon + **Op** Optics



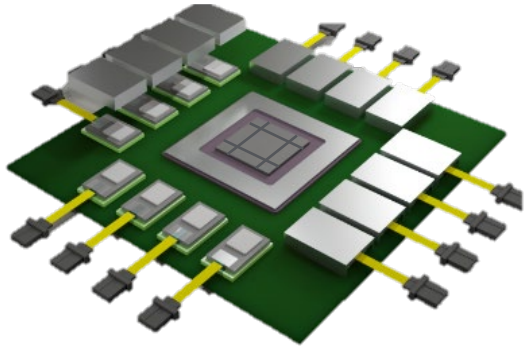
Source: Cisco 2024

Heterogeneous Integration: Silicon Photonics

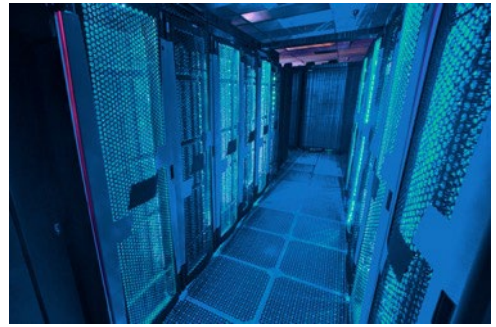
Chiplets

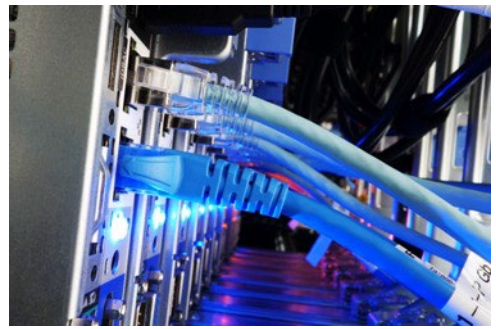


CPO
(Co-Packaged Optics)

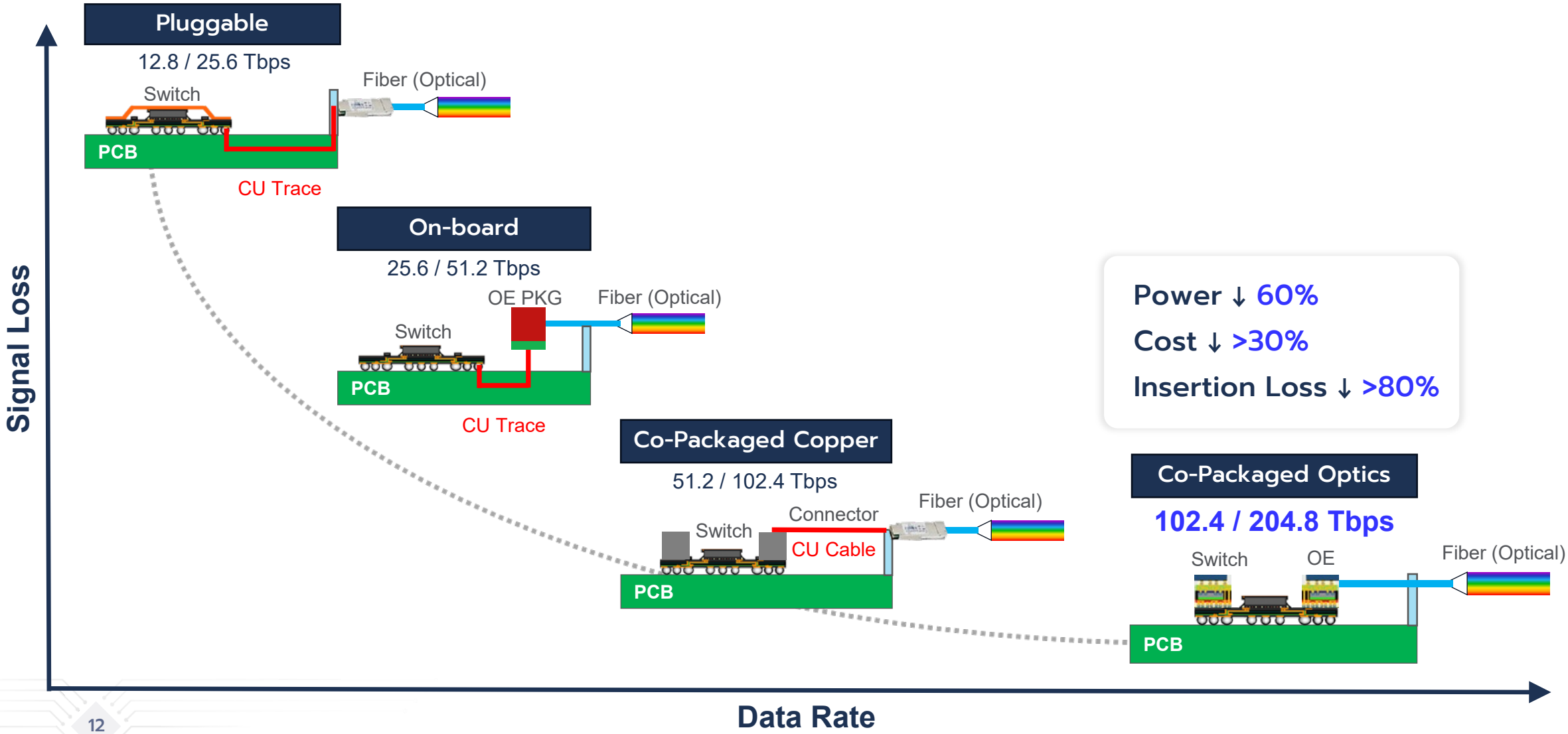


Data Center





Power Efficiency through Silicon Photonics

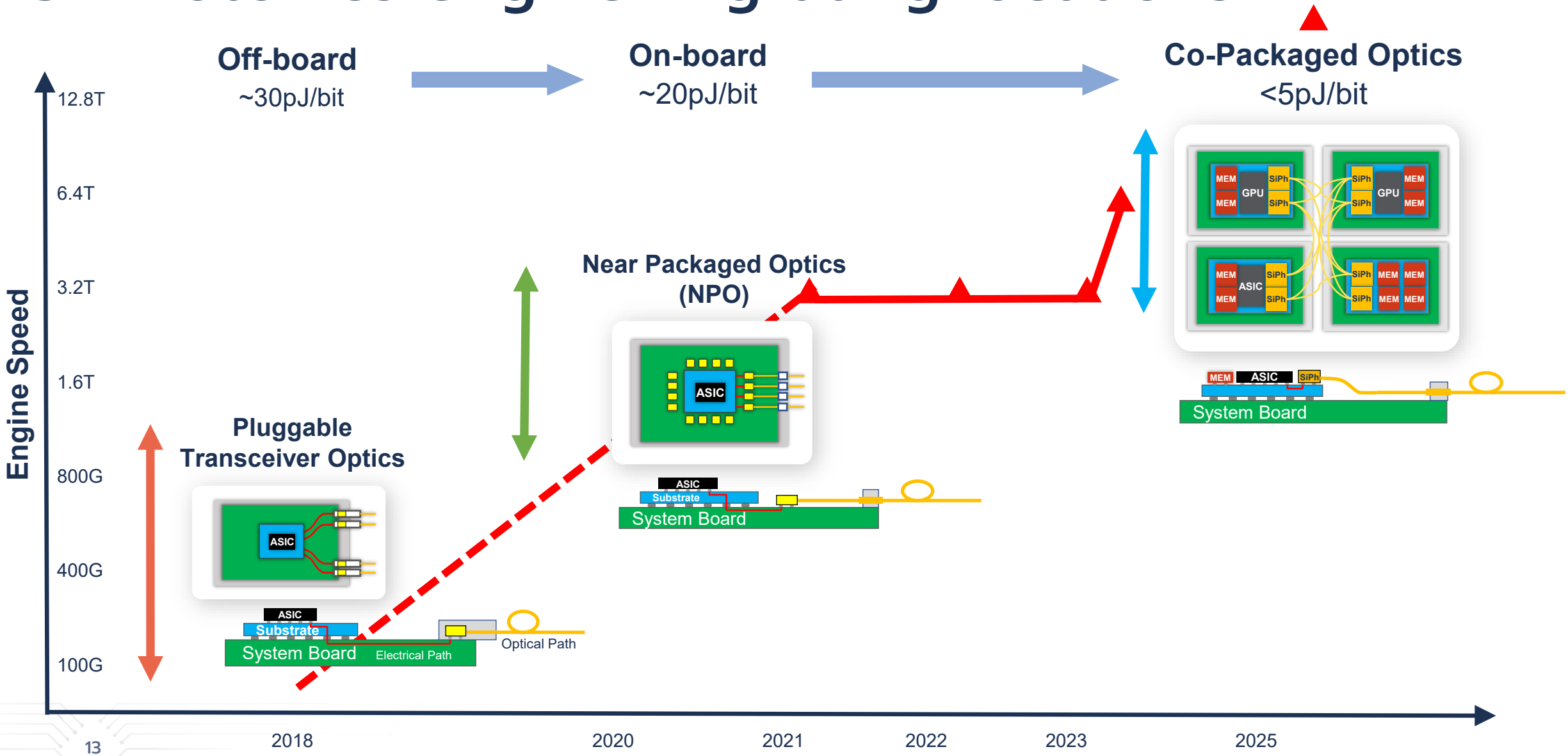


Power ↓ 60%

Cost ↓ >30%

Insertion Loss ↓ >80%

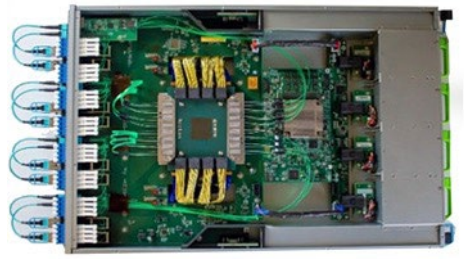
Si Photonics engine migrating locations



CPO System - Supply Chain Ecosystem

Data Center Architect

System Requirement



ODM - OEM
System Integration

Optical Requirement

New Generation ODM-OEM

Chip Design
PIC/EIC

Foundry
Chip MFG

OSAT
EIC/PIC
Integration

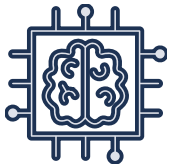
OSAT/EMS
Optics
ASSY & Test

OSAT/EMS
Module/OBO/CPO
ASSY & Test

Summary

- AI and Data continue to fuel semiconductor innovation, with exponential proliferation through 2030 and beyond that will shape global life and lifestyle in unimaginable ways.

- Collectively, our industry is accelerating the AI economy through Heterogeneous Integration advancements.



- Packaging creativity is enabling seamless integration of multiple chiplets, SiPs, modules into one single package optimized for enhanced functionality and operating characteristics.

Thank you