Leveraging AI to Optimize DFT and Test Implementations

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Outline

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- Motivation
- Design-for-test (DFT) challenges
- Scan architecture optimizations and DFT assistants
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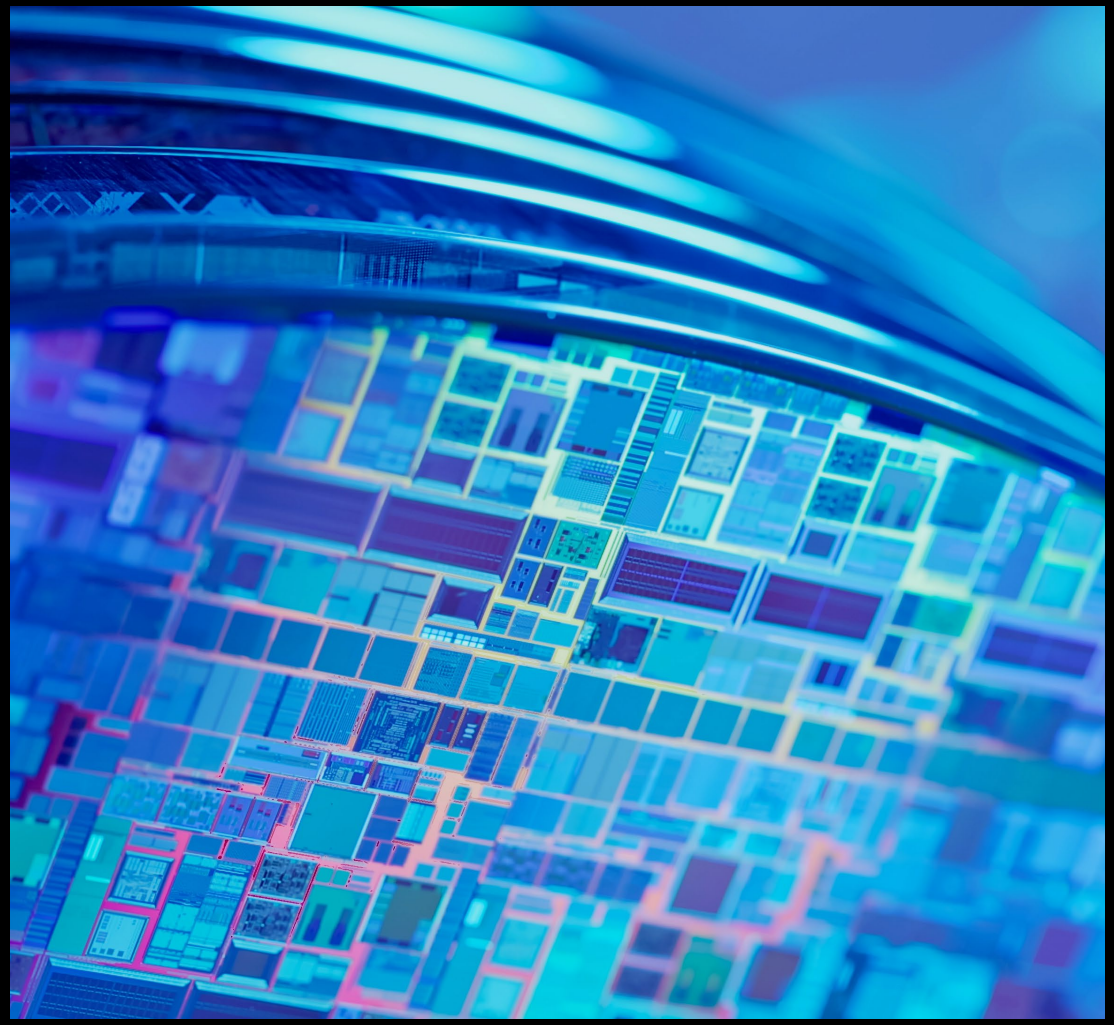
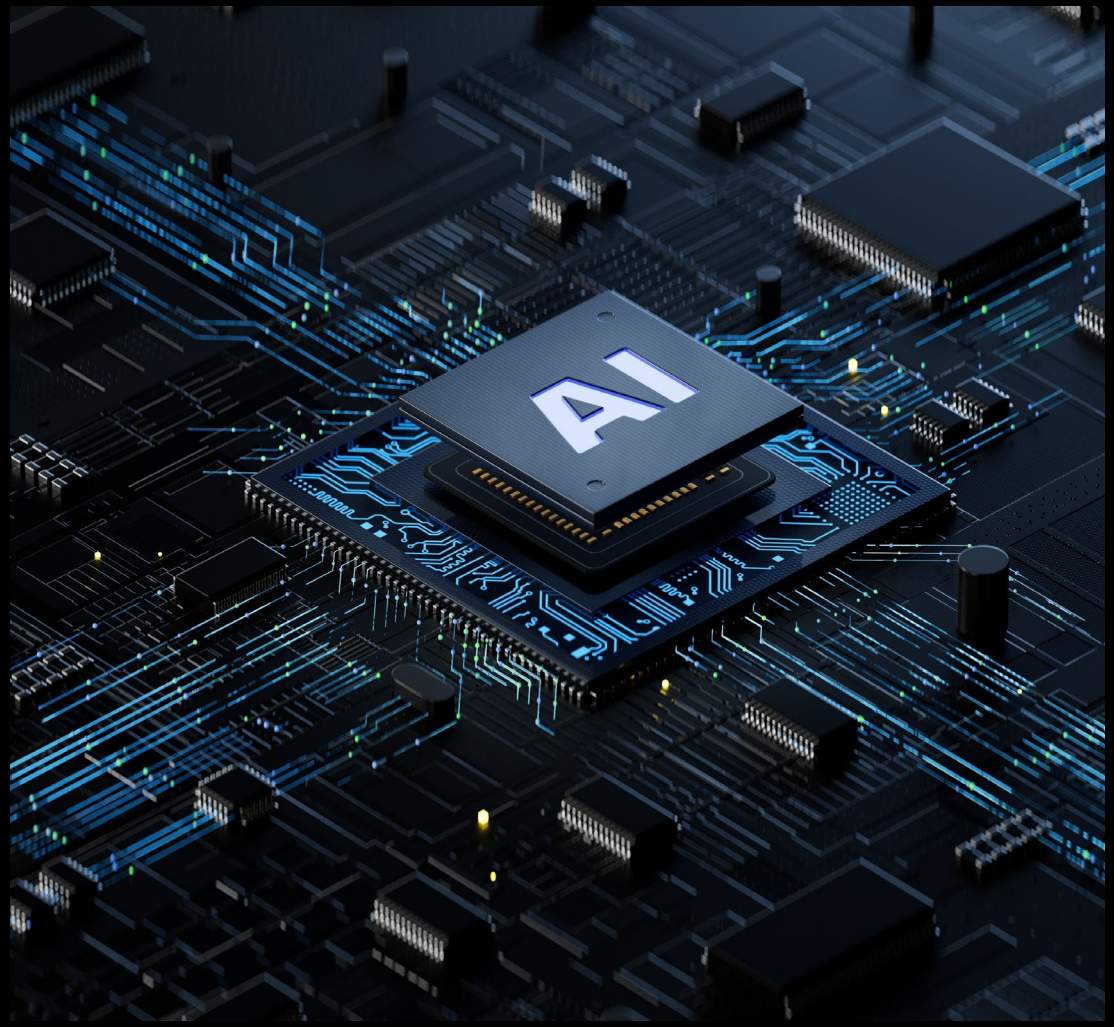
Introduction



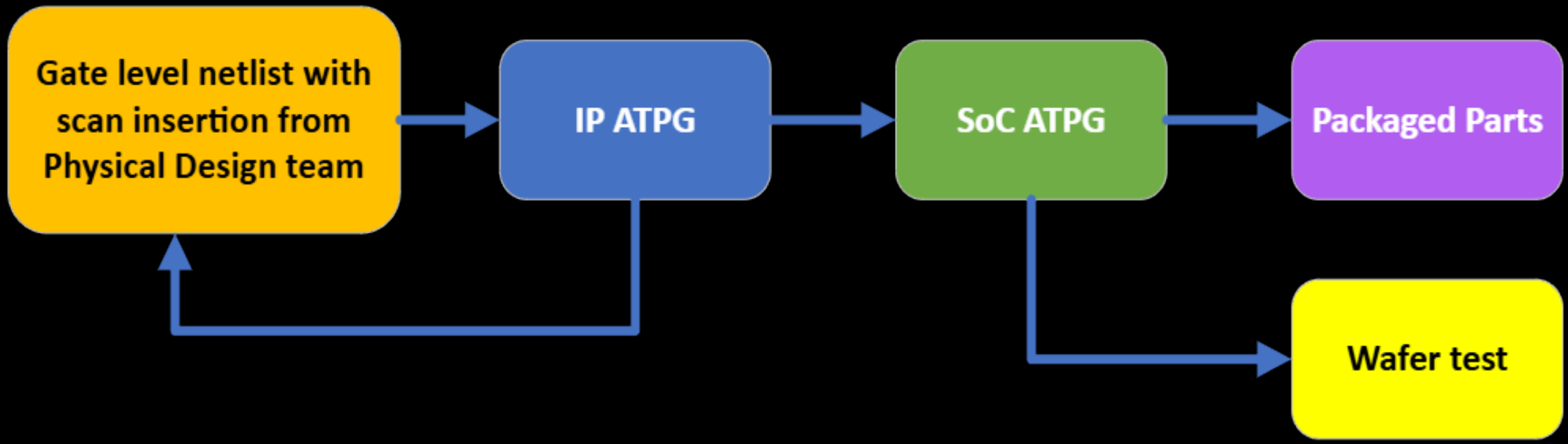
- Design-for-test (DFT)
  - A discipline in silicon design focused on techniques assuring integrated circuits are testable
- Automatic Test Pattern Generation (ATPG)
  - Generate patterns to detect modeled manufacturing defects
- Defect parts per million (DPPM)
  - The lower the better

Introduction



- Machine-learning
  - Allows for the development of algorithms that can learn from data to perform tasks requested by users
  - Utilizes predictive analytics, natural language processing, and speech recognition
  - Confidence score
  - Large Language Model (LLM)

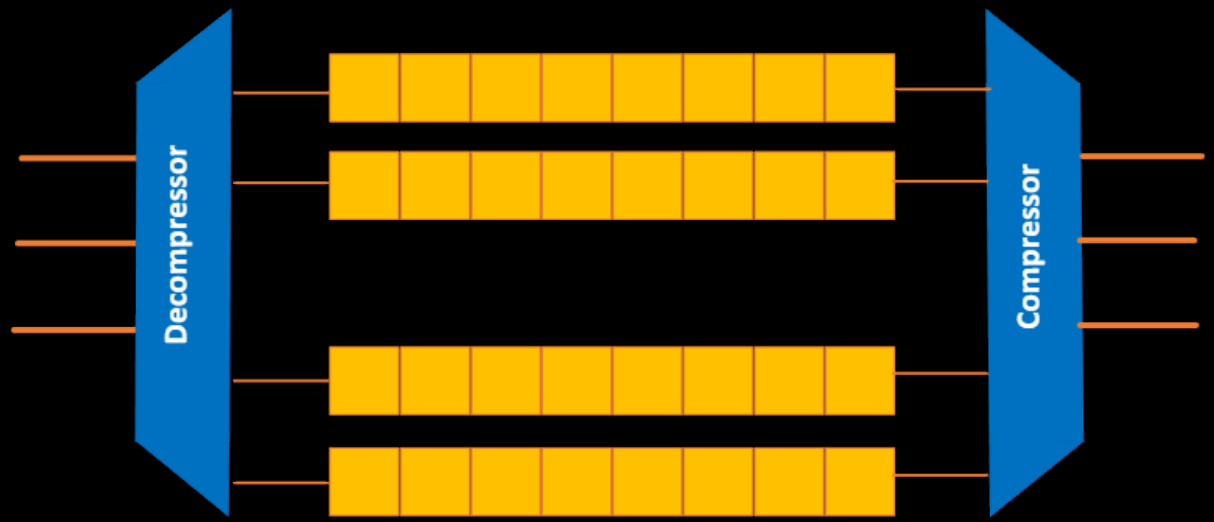
Motivation

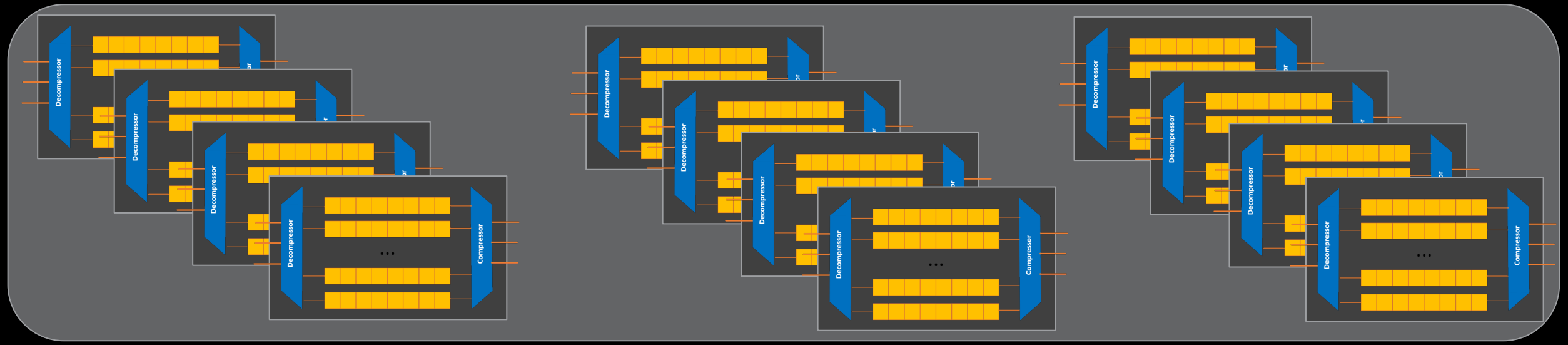


- Save iteration time in defining and implementing optimized scan structure
- The need for lower pattern count and high-test coverage
- Bug and information broadcasting or distribution

DFT challenges

- Optimized compression ratio
- Optimized scan chain channel distribution
- Optimized scan chain length



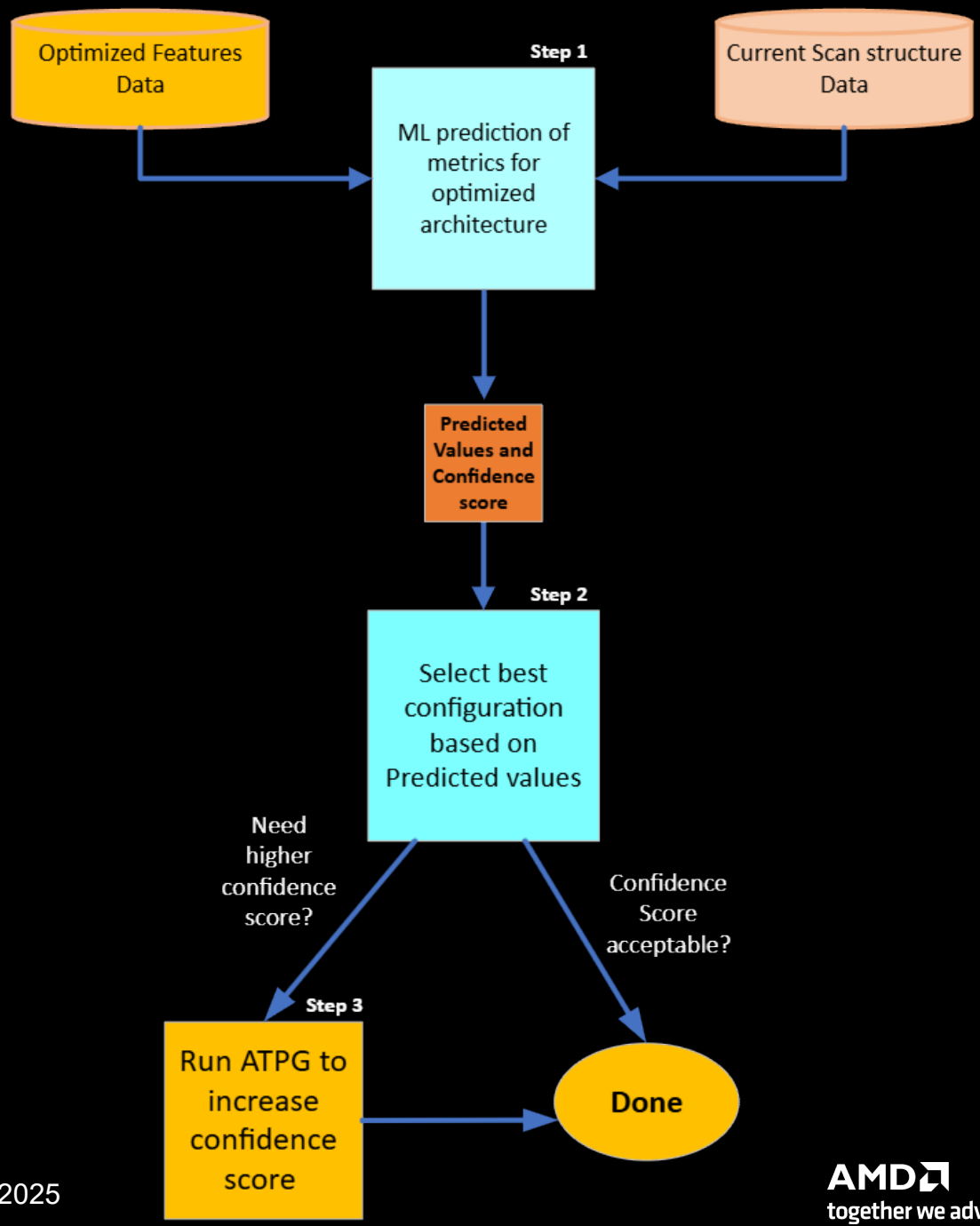


DFT challenges

- Not easily accessible or understanding of DFT and ATPG learnings, information, and documentations
- Overwhelming volume of irrelevant data when searching for specific topic, issues or solutions
- Time consuming iteration of ATPG run to find optimized scan compression and architecture

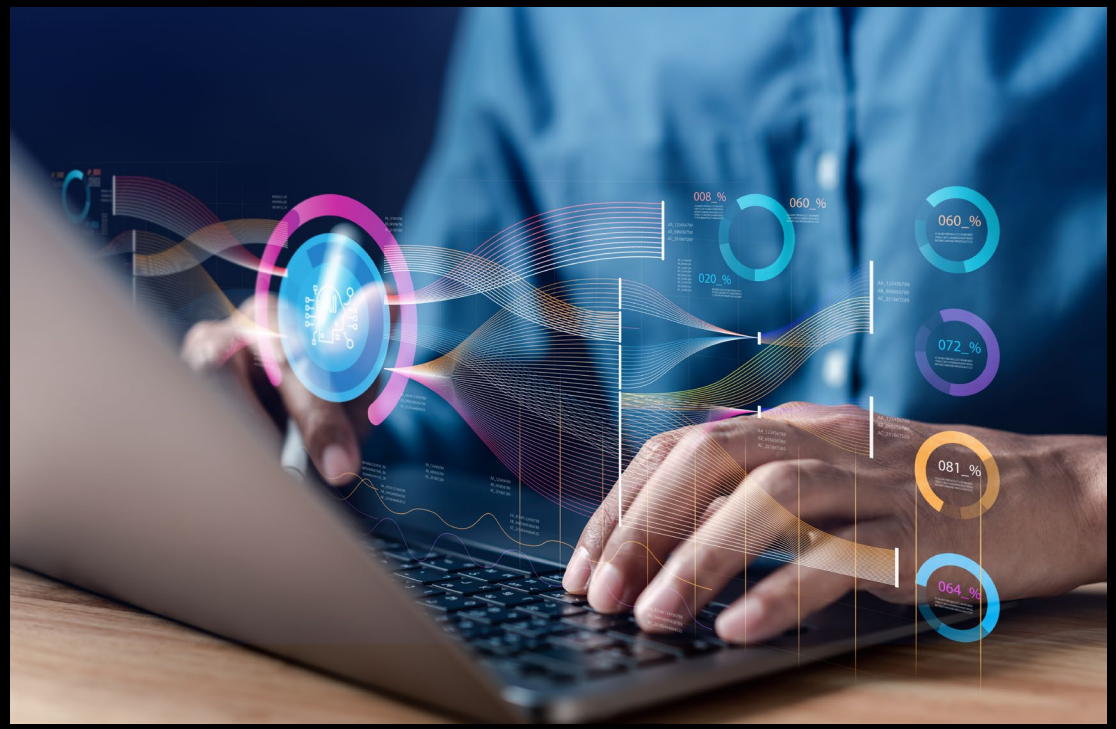
Scan architecture optimization

- Input data:
  - Optimized features
  - Current design scan structure
- ML Prediction
- Select best configuration
- Check confidence score
- Accept or Run ATPG to increase confidence score



Virtual assistants

- Can use utilized by DFT verification, design and structural engineers
- DFT verification debug helper – collect verification logs to streamline debug process
- DFT chatbot – trained with DFT related documents, learnings, bugs. Utilize learning abilities to differentiate relevant from irrelevant information



Benefits

- Expected benefits are lower pattern count, higher test coverage, optimized compression ratio
- DFT assistants can support engineers to increase productivity
- DFT assistants can also help in distributing information

Conclusions

- ML engine to improve scan designs and structures
- AI assistants to help DFT engineer productivity
- Optimized scan structure with less ATPG iterations

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Thank you

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