

Process Technology/Packaging/Assembly Technology

"Split-Gate Inter-Poly Architecture for Electrical Gate Leakage and Mechanical Wafer Warpage Optimization in Trench FP-MOSFETs"

Mechanical wafer warpage is a critical challenge in advanced Trench Field-Plate MOSFETs (FP-MOSFETs), becoming more severe with deeper trenches and higher trench densities. In wafer fabrication plants, high warpage causes severe mechanical robot handling failures and lithography depth-of-focus degradation. While lower temperature processing (below 1000 °C) mitigates warpage, it fails to fully anneal out split-gate inter-poly oxide charges, thereby degrading device electrical performance. To resolve this stress-performance trade-off, this paper proposes a novel split-gate architecture featuring a robust inter-poly structure that physically and electrically isolates the polysilicon layers. This architecture effectively suppresses leakage paths while fully preserving the warpage reduction achieved through thermal optimization. Experimental results demonstrate a practical solution that balances mechanical stress mitigation with high inter-poly oxide integrity.

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