GLOBALFOUNDRIES has shipped >250,000 32/28nm HKMG wafers to date. The milestone represents a significant lead over other foundries in HKMG manufacturing.

LEADING THE FOUNDRY RAMP IN 32/28nm WAFER PRODUCTION

On a unit basis, cumulative 32/28nm shipments for the first five quarters of wafer production are more than double that achieved during the same period of the 45/40nm technology node ramp, demonstrating that the overall HKMG ramp has significantly outpaced the 45/40nm ramp.

The tradition of rapidly ramping leading-edge technologies to volume production continues.
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MISSION AND VISION STATEMENT
ACCELERATE THE GROWTH AND INCREASE THE RETURN ON INVESTED CAPITAL OF THE GLOBAL SEMICONDUCTOR INDUSTRY BY FOSTERING A MORE EFFECTIVE ECOSYSTEM THROUGH COLLABORATION, INTEGRATION AND INNOVATION.

- Address the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging
- Provide a platform for meaningful global collaboration
- Identify and articulate market opportunities
- Encourage and support entrepreneurship
- Provide members with comprehensive and unique market intelligence
A
alog circuit technology, once considered mature if not commoditized, is experiencing a renaissance in growth, due to its essential role in a wide range of new devices. According to GBI Research, the analog circuit industry can look forward to attractive expansion through 2020, as new OE product platforms proliferate around smartphones, tablets, radio basestations, portable device batteries, medical imaging scanners, electric cars and a wide variety of other industrial and medical applications.

Barriers to New Analog Products
Discussions with decision-makers and technical users at a range of OE end-users in North America suggest that analog circuit manufacturers face significant barriers to getting their newest innovations adopted in the fast-growing small- and mid-sized horizontal OE market:

- After years of digital technology adoption, today’s product development engineers at small- to mid-sized original equipment manufacturers (OEMs) lack a deep understanding of analog technology and its latest developments.
- Lack of analog expertise means that most OE product and purchasing engineers will default to familiar legacy brands and trial-and-error component selection and procurement. The supply chain process is seen as cumbersome, risky, time consuming and inadequate.
- Rapid consolidation of semiconductor distribution means that the bulk of today’s analog products are distributed through a small number of global players offering extensive assortments, ease of order entry and competitive prices. Promotional materials by these players aside, the reality on the street is that the field application engineering support craved by small- and mid-sized OEMs is wholly inadequate.
- The pinched economics of small- to mid-sized OEMs requires a multi-year lifecycle approach to customer development and demand creation investment that large global distributors and traditional manufacturer reps find hard to square with financial pressures. Streamlined websites and don’t offer proliferating online data sheets or webinars are great, but not the high-touch assistance smaller OEMs require.

The bottom line for analog circuit manufacturers investing heavily in technology innovation and product differentiation for industrial and medical OEMs is this: incremental growth will come from building new demand creation capacity and competence in their distribution channels.

Restructuring Distribution for Growth
Research has shown four growth avenues for analog electronics manufacturers in rapidly expanding horizontal markets:

- Broaden the distribution system to channel models willing and able to overcome sourcing inertia at small- and mid-sized OEMs.
- Determine improved online and offline channel activities required to drive profitable adoption of new off-the-shelf products.
- Structure viable and attractive channel economic models that ensure profitable execution of demand generation activity.
- Identify new types of channel partners with field reps and mindshare capable of driving adoption by harder-to-reach OEMs.

Customer Driven Channel Reinvention
A market-focused approach to helping companies pursue the four growth paths above brings fresh perspective and new ideas to experienced distribution managers who are under pressure to put growth- and profit-driving distribution channels in place. Collaborating side-by-side with a company’s own distribution managers in a straight-forward process is outlined below in Figure 1.

Mapping End-User Markets
Successfully distinguishing one technology channel from another requires that end-customers perceive a tangible difference in their
total product buying and usage experience. One approach to
reinventing high-tech channels starts with immersion in the voice-of-
the-customer. Unlike conventional market research, this exploration
is done through one-to-one strategic dialogues with important
decision-makers, influencers and internal customer users. Goals
include surface distribution whitespace in the market, identifying
high-value customer segments willing to pay for improved performance and laying out the lifecycle economics of a new OEM
distribution relationship.

**Designing Optimal Channels**
The basic premise of using distribution to build high-tech competitive
advantage is this: superior customer experiences are delivered through
superior channel activities, whether they’re performed directly or
through independent partners. As outlined in Figure 2 below, the
optimal channel structure divides these value-creating distribution
activities among participants in a way that is both effective in creating
customer satisfaction and efficient in driving return on investment and profitability.

**Figure 2. Designing the Optimal Distribution System**

<table>
<thead>
<tr>
<th>Demand-Side Issues</th>
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<tr>
<td>Customer Desire for Elements of Channel Experience</td>
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<table>
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<th>Supply-Side Issues</th>
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<tr>
<td>Activities Required to Deliver Channel Experience Elements</td>
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</table>

| Division of Labor to Optimize Effectiveness and Efficiency |

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**Building Channel Networks**
Once the improved distribution system’s activities are allocated among
participants, a new channel model is built detailing the competencies,
systems, investments, assets and human capital needed to successfully
expand in targeted end-customer markets. Working closely with companies to screen, recruit and organize the network of partners aids in the ability to execute a new channel model. Most often the execution work begins in a tightly-defined geographic territory, in close collaboration with a few highly-motivated channel partners.

**We’re Often Asked….**

How is it possible there might still be fresh opportunities to improve distribution that we, or others in the industry, haven’t tried yet?

One of the most frustrating aspects of managing an external system of independent channel partners is the need to respond to countless day-to-day demands and to find quick resolution to urgent problems. Not only that, the repetitive nature of these channel management demands and problems tend to push all of us toward tried-and-true, conventional responses. That’s only natural. For managers steeped in day-to-day logistics and quota management pressures, it’s hard to take a step back and a fresh look, to re-think customer pain points in a different way. And of course for field sales leaders trying to meet their goals, it’s harder still to move forward with new, better ways of operating that might feel risky, costly or longer-term. But fast-changing markets are where the richest sources of high-profit growth will lie. An objective new look at customer needs continues to be the surest path to competitive advantage.

**Don’t all the channel options we can choose from already exist?**
The biggest opportunities for share growth and differentiation often arise from a fresh look at end customers and a search for new routes to their market. Way back when, any industry’s original channels were custom built in direct response to end-customer needs. Over time, however, as sales have grown and competition intensified, legacy channel structures tend to grow more complex, putting greater and greater distance between manufacturers and their end customers.

The highest-performing channel systems resist this separation. Their managers take a proactive role in designing and shaping their channel structures. They also take steps to ensure that the activities performed by their channel partners, their partners’ economics and all of the various touch points in the channel perform in ways that add new and improved value to the end customer. Proactive channel managers take pains to select, shape, guide and train only those channel partners that have the ‘skill and will’ to meet end-customers’ demands.

**OK. But don’t economic realities prevent us from seriously innovating our channel model to smaller OEM customers?**

Channel economics are certainly an essential nut to crack. But a lot has been happening to make the pursuit of whitespace distribution opportunities more viable. Forward-looking channel managers are harnessing the latest online technologies and offline tools in ways that tighten up channel efficiencies and raise market effectiveness simultaneously. Often this calls for new channel activities and sometimes new kinds of partners or partners with new skills.

The important thing is to focus on customer acquisition and retention levers first, and then work back to the economics necessary to support them. Higher conversion rates and loyalty can improve the revenue side of channel business models tremendously. Moreover, in most instances there are new ways to make the economics work, both for the producer and for the right channel partner.

**About the Author**
Richard E. Wilson, Chicago Strategy Associates founder, has over twenty years of experience working with technology, industrial and consumer companies to improve channels for accelerated growth. Rick is also clinical associate professor of marketing at the Kellogg School of Management, Northwestern University, where he teaches distribution channel strategy and co-directs the Kellogg Center for Global Marketing Practice.
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A n industry changing decision was made in the semiconductor industry as it hit the 22nm node – Intel chose to move from a planar device, as has been used since time began (as it were in our industry), to the brave new world of three dimensions. The question “Why?” has been asked many times, and many different answers have been given. Whatever the real underlying reasons, one thing is clear – something was not right with the world as we knew it up to that point. The move to a Tri-Gate (or FinFET) structure has happened, products are in full production and as we can see from the UBM Insights teardown pictures, the very pretty Intel Tri-Gates are clearly a technical marvel.

As Intel will gladly tell you, it believes that - from a practical, business and technical perspective - this increases its process technology lead on the rest of the industry. Intel has declared itself the winner, the first company to have fully depleted devices in production and the owner of a four-year advantage over everyone else in the semiconductor industry. Indeed, while the rest of the pure-play foundry industry continues on a path of rolling out its 20nm process in a planar flavor, Intel carries on with its inexorable march to the next fully depleted device in its tick–tock strategy.

As you see in the diagram farthest to the left, the depletion zone is variable and bridges the gap between source and drain in a variable manner and, in fact, is created as a function of doping. You want a thin depletion zone, and to get the depletion zone thinner as the device scales, you dope more. However, doping strength only goes so far. The further you reduce the volume of the depletion zone, the more you get Random Dopant Fluctuation (RDF), which becomes increasingly intrusive. With the latest extremely deep sub-micron devices, you need an increasingly small and increasingly heavily doped area for source, drain and channel.

Such extreme doping levels in such small areas make it more likely the dopant will be distributed unevenly, and in different densities, over a relatively larger area of dispersion as the total doped volume reduces. The resultant increase in RDF gives much more variability on silicon, specifically for statistical variation, which is the largest contributor to SRAM performance and variability. And, Intel is known for large SRAM arrays for the L2 and L3 cache on its products, up to several megabytes per chip.

As you can see in the other two options, whether in a planar, Tri-Gate or FinFET device, the channel size and the depletion zone are of equivalent size, so the device is fully depleted as all the available silicon in the channel is the depletion zone. This gives you the possibility of having an undoped channel, since the depletion zone is no longer a function of doping. Then all the RDF issues go away – no RDF means much lower variability, which in turn means better performance, higher yield and, most critically, a lower minimum operating voltage on the SRAM. To a slightly lesser degree, this benefits all other areas of final silicon as well, due to the reduced variability; but SRAM remains the part of the design that will see the biggest impact from the undoped and fully depleted channel. Was it the large impact of variability on power and performance, especially at low voltage, on its SRAM arrays with a 22nm planar process that caused Intel to move to fully depleted?

Whatever the case, Intel saw a clear requirement for a fully depleted device and has been quite vocal in explaining the technology and its benefits. The company is so confident in its technological prowess that it is practically taunting the rest of the industry to try and put FinFET into production. Talking to contacts in the industry that have been working on FinFET definition and creation for quite some time, the consensus seems to be that those relatively new to the technology trying to catch up with Intel "don’t know what they don’t know yet.”

The Future
So where does this leave the semiconductor industry, and what does it mean for the ongoing Intel versus ARM debate? Let’s see what the future might possibly look like in 2015 / 2016.
If we look into the future using the industry standard cadence of a two-year cycle between process nodes, something quite interesting stands out. When the rest of the semiconductor industry gets access to its first fully depleted FinFET device from a pure play foundry, Intel will be on its third incarnation of its Tri-Gate process.

To date, the biggest value proposition for using an ARM-based processor is power efficiency. This is well known, as there are billions of low power devices that incorporate an ARM processor across a vast array of industries. If, however, Intel’s published details on the power efficiency of its underlying process technology are accurate and keep improving at historic levels, we can expect to see a tipping point in the balance between process node and processor architecture. A two generation fully depleted process technology lead could well create an inflection point where many in the industry may finally start to believe that Intel’s process technology dominance could well outweigh the energy efficiency benefits of the ARM architecture.

Now, take into consideration the greater performance and inevitably more power-hungry next-generation ARM Cortex™-A15 processor, along with the pending move to a larger 64-bit architecture, and those nagging thoughts get a little louder. Of course, we can point to an ARM “big.LITTLE” implementation, the power-efficiency benefits of cache coherency (which is also being adopted by Intel’s competitors in the x86 space), the strong ARM ecosystem (especially in the low-power mobile sphere), and many other factors that could help counterbalance Intel’s process technology leadership. But I still have that little guy with the horns and pitchfork on my shoulder, whispering in my ear. Of course, only time will tell.

What’s at stake in the mobile market during the next few years? With a projected one billion mobile processors expected to be sold in 2014, the stakes are high. For a chipset maker, a one percent increase in market share equates to roughly $200 million in additional revenue. Not too shabby. For handset makers, the impact is more significant, with a one percent increase for them equating to more than $1.5 billion in additional revenue! With that in mind, it’s easy to see why Intel believes its vast capital and R&D expenditure are worth it.

Intel clearly decided that they required a fully depleted device and its published results show impressive Vmin (minimum operational voltage), power and performance numbers, and I’m sure most of us have enjoyed the YouTube videos that walk us through the technology and its benefits. As for the planar process, it’s something pure play foundries know a lot about, and they’ve had plenty of time to optimize (as previously mentioned, planar has been around since time began). Furthermore, all the equipment they need is already in house and most likely somewhat depreciated, so planar should also be a cheaper option. But perhaps the most telling and important point is that it’s easier to do than a Tri-Gate or FinFET. When you take that into account, along with the other aforementioned points, it means you can bring your fully depleted device to market much more quickly than is possible using other paths.

In fact, GlobalFoundries has announced support of a fully depleted planar process in its fabs for 28nm and 20nm, and a scaling path to 14nm already has been demonstrated. This is the only fully depleted semiconductor process available today from a pure-play foundry and it’s not a one-shot wonder – it has a proven scaling path. This puts this technology in the enviable, unique and welcome position of being the only fully depleted semiconductor process available for all fabless players to take advantage of now, until the global industry shift to three dimensional fully depleted devices happens.

So how do companies give their mobile processor the next kick in the power and performance race? How can they say “me, too” to Intel before it hits its third-generation of fully depleted technology? How can semiconductor companies start leveling the playing field in terms of process technology, and help preserve or even increase market share with the least amount of risk?

Move to a fully depleted device today. It’s already available. All you need to do is ask for it.

About the Author
Tim Robson is currently product marketing manager at Soitec, where he is responsible for product marketing of all products in the Microelectronics BU. He started his career in 1993 at what was then SGS-Thomson doing transistor level layout with 500nm technology on the last of the Transputer products. Since then his career has grown from transistor level to complete RTL to GDSII implementation of products with hundreds of millions of transistors. In the last decade he has been at the forefront of leading low power and process technology, defining and implementing 45nm, 32nm and 28nm processes and low power design technologies for mobile applications, bringing together requirements from system and platform architecture through to process definition.
Confronted by rising costs, constrained resources and a challenging technology roadmap, the semiconductor industry faces difficult technology and investment choices. In my interview with Dave Bell, president and chief executive officer of Intersil, we discussed how Intersil stays competitive in such a difficult environment; its most recent and exciting product offerings; its asset-lite operations strategy; and much more.

— Jodi Shelton, President, GSA

Q: Intersil offers high-performance, analog, mixed signal and power management products for a variety of markets. Tell us about some of your most recent product introductions and which product offering you’re the most excited about.

A: Intersil does have a very broad product offering, and it addresses many different markets. About a year ago, we identified what we call our Top Ten Growth Drivers. These are the areas that we’re most excited about and on which we’re focusing nearly all our resources. Out of that Top Ten, I would say that pico projectors and Thunderbolt cables are probably the most exciting.

Pico projectors are very tiny projectors that you can hold in your hand. Unlike the larger ones you see in conference rooms, these are personal devices that are very low power. Intersil has developed a complete chipset to drive a pico projector light engine. One of the first pico projectors on the market is from Pop Video, and it’s an accessory that that attaches to your iPhone. We believe in the next couple years you’re going to see small pico projectors embedded into smartphones and tablets.

This is a nascent market that’s just beginning, but we can see there’s enormous potential when these devices start being embedded into handheld devices. I remember the first time I saw a camera in a cell phone, and it struck me as pretty odd. I thought, why would anybody want a camera in their cell phone? Well, now, as we all know, you can’t even buy a cell phone without a camera. Pico projectors may not become quite that ubiquitous, but we think there’s going to be a very large number of handheld products that will contain embedded pico projectors for looking at photos, HD full color movies and presentations. It’s becoming clear that social networking is one of the things that will really drive this area.

The other exciting area is Thunderbolt. Thunderbolt is a new high-speed cable protocol that has been created by Intel and Apple. Apple began including Thunderbolt ports on some of their products about a year ago, and it’s now putting Thunderbolt ports on all of their computing products. I think eventually we’ll see them on handheld products as well. This is like a USB cable on steroids, and we think it’s going to be adopted by most computing and even consumer products down the road.

Today, when you buy a USB cable at Best Buy, it’s a copper cable with simple connectors on each end. However, due to the extremely high data rates, Thunderbolt cables must embed electronics inside the connectors at each end of the cable. Intersil has developed a 40nm mixed-signal IC, plus a power management IC specifically tailored for Thunderbolt cables. If this gets embraced by the computing and consumer industries as we expect it will, it’s going to drive a lot of sales.

**Q:** Intersil serves a broad set of markets and applications including consumer, computing, industrial, medical and automotive. Which end market do you believe provides the greatest opportunity for Intersil and how are you addressing that opportunity?

**A:** All of them provide great opportunities, but in different timeframes. For instance, we sell into the industrial and automotive markets, and those markets have above average gross margins; however, the downside is that the growth rate of those markets is very slow and the design cycle can take many years. The compensating benefit in the industrial and automotive markets is that even though it might take a number of years to get a chip designed into an end product, it tends to stay there for many, many years, and in some cases, even for decades.

On the other hand, when you look at some of the more fast-paced markets, including the consumer and notebook computer markets, those move quickly. We might have a new product that gets designed into a smartphone and have it ramped into production within a quarter or two. These are very rapid design cycles, with very rapid growth and large sales dollars. The compensating disadvantage is that those sales can go away just as quickly, so you must have a very rapid product development cycle, generation after generation.

One of the strengths of our business is our diversity. Companies need to have market diversity in our rapidly changing world where it’s really difficult to predict the next hot market.

If somebody had asked me before Apple introduced the iPad if I thought tablet computers would be successful, I would have laughed and said, “Are you kidding?” Every prior attempt at a tablet computer had been a failure. But look today at how popular the iPad and other tablets are. It’s a very fast-paced world, and placing multiple bets in multiple markets is really important for stable growth.
The semiconductor industry has been doggedly shrinking process technologies for over 30 years. The economic enticement for this behavior is waning, however, as we reach 20nm and the end of both conventional lithography and the conventional planar, bulk transistor. The excessive cost of 20nm and smaller process technologies due to double-patterning or EUV lithography, as well as three-dimensional transistors, requires that the industry rethink its roadmap. Products that command a high margin and create additional value from density will continue to migrate to 20nm and smaller process technologies, but nevertheless want to minimize cost. And what about low-margin products that don’t require greater density to add value? Those products need a way to add value without shrinking to 20nm.

The semiconductor industry needs an economically sensible roadmap that addresses the excessive cost of 20nm and smaller process technologies. This article argues that the semiconductor process technology roadmap should now be split in two: a roadmap with the classical “Moore’s Law” benefit of greater density from shrinking, and a “More-than-Moore” roadmap that enhances the capability of a given process technology by reducing power consumption.

This process technology enhancement (i.e., improvement) is important, because IC products need to add value even if they cannot economically shrink to a smaller process technology. Reducing power consumption is a particularly good way of enhancing the value of a given process technology, because a majority of today’s IC products are very power-constrained. The amount of functionality that can be packed into mobile computing devices such as smartphones, tablets and notebooks is now limited by power consumption. In addition, power density will soon limit process technology applications from CPUs in data centers to small ICs stacked together in 3-D packages because of the amount of heat generated.

Beyond 28nm and the Conventional Planar, Bulk Transistor

The excessive cost of 20nm process technology is caused by two things: the move beyond conventional 193nm wavelength lithography, and the move beyond the conventional planar, bulk transistor.

The industry agrees that the next step in lithography is extreme ultraviolet (EUV) wavelengths, but the low efficiency of the EUV source technology makes this step prohibitively expensive today. Instead, the industry will use double-patterning with conventional 193nm wavelength lithography to pattern the critical layers in the 20nm process technology. This choice causes excessive, but not prohibitive, cost.

The industry does not yet agree on the next transistor structure, but there is general agreement that conventional planar, bulk transistors cannot be scaled beyond the 28nm or perhaps the 20nm generation. The need to control power consumption makes the move to a depleted-channel transistor architecture inevitable. A depleted-channel transistor reduces power consumption both by decreasing threshold voltage variation and enabling the supply voltage reduction that has been missing from the last several generations of process technology shrinks.

A depleted-channel transistor can be three-dimensional (e.g., FinFET), planar on silicon-on-insulator wafers (e.g., FD-SOI), or planar on bulk silicon wafers (e.g., the Deeply Depleted Channel technology). The table in Figure 1 summarizes these three main options to achieving a depleted-channel transistor.
Fig 1: The Three Main Options to Achieve a Depleted-channel Transistor Architecture

<table>
<thead>
<tr>
<th>Metric</th>
<th>FinFET</th>
<th>FDSOI</th>
<th>DDC: Enhanced Bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idsat</td>
<td>Excellent</td>
<td>Fair</td>
<td>Good</td>
</tr>
<tr>
<td>SOC Support</td>
<td>Difficult</td>
<td>Good (Except ESD)</td>
<td>Excellent</td>
</tr>
<tr>
<td>Multi $V_T$</td>
<td>Difficult</td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Power</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>$F_T$</td>
<td>Poor</td>
<td>Poor</td>
<td>Excellent</td>
</tr>
<tr>
<td>Junction Leakage</td>
<td>Good</td>
<td>Excellent</td>
<td>Average</td>
</tr>
<tr>
<td>Cost</td>
<td>Poor</td>
<td>Average</td>
<td>Excellent</td>
</tr>
</tbody>
</table>

Each option presents different trade-offs in cost, performance and power. The FinFET structure promises the most drive current and therefore performance; however, it has difficulty supporting multiple threshold voltages that are necessary to minimize power consumption. FD-SOI supports multiple threshold voltages well and has very low junction leakage, but has lower drive current than a FinFET structure. The DDC structure supports multiple threshold voltages, but also has lower drive current than the FinFET structure. Economically, the FinFET structure is an expensive architecture to manufacture, the FD-SOI structure is manufactured on expensive SOI substrates and the DDC structure is the least expensive to manufacture.

Ultimately, product application requirements will dictate which depleted channel architecture to select. On one hand, performance has historically been the primary driver of the CPU roadmap. On the other hand, system-on-chip (SOC) products are coming to dominate the IC market, and for SOCs minimizing power consumption is a major priority. There are various design techniques to optimize dynamic power. Among them, multiple threshold voltage (multiple-$V_T$) flow is very popular because it doesn’t require changes to the SOC architecture. A multiple-$V_T$ flow in conventional planar, bulk CMOS technology is well mastered, and is achieved by multiple channel implants. However, for most depleted channels that rely on maintaining undoped channels, achieving multiple-$V_T$ is more difficult. For example, in a FinFET the body biasing is so small that heavy FinFET doping becomes necessary to deliver a large enough $V_T$ range, degrading the depleted-channel behavior. Due to its unique multi-layer architecture, the DDC transistor can deliver a large range of $V_T$’s by way of dopant implantation while still maintaining an undoped surface channel.

Enhancing 90nm to 28nm Process Technologies by Reducing Power Consumption

The reduction in power consumption that comes with a depleted-channel transistor can also enhance process technologies from 90nm to 28nm. Products that are using a given process technology today need a roadmap that allows them to increase value, and it needs to be economically sensible. Rather than migrate to a smaller process technology, especially when it is new and still immature, why not enhance the existing process technology? The DDC transistor architecture offers the most cost-effective way of enhancing a given process technology by reducing power.

While there are enhancement costs for a given process technology, they are minimal compared to the cost of migrating to smaller process technologies, especially when the smaller process technology is new and still immature. An effective technology enhancement delays the significant cost of technology migration by retaining the mature design rules, design methodologies and circuit intellectual property (IP), and the manufacturing tool sets of the mature technology.

The costs of migrating to new and still immature process technologies is well documented in terms of the need for new manufacturing tool sets and circuit IP, as well as for design and mask technologies. But migration is also expensive because it runs into the steep portion of several learning curves, including the cost-of-entry learning curve and the first-time-failure learning curve. For a majority of products it makes economic sense to delay the cost of migrating to new and still immature process technology.

Figure 2: Cost-of-entry for 90nm through 40nm Process Technologies

The cost-of-entry learning curve, illustrated in Figure 2, shows that early adopters of a new process technology generation pay significantly more entry costs than adopters who wait. Cost-of-entry refers to the non-recurring engineering (NRE) costs associated with migrating to a different process technology generation, including design migration, third-party design IP, masks and package development. The data is a blend of entry costs from 90nm through 40nm for many products compiled by VLSI Research. On average, the cost-of-entry decreases by five times in the first four years after the introduction of a new process technology generation, as the early adopters drive the maturity of the items mentioned. The cost savings obtained by delaying migration are extremely important for products that don’t have the huge volumes and/or high average selling prices (ASPs) needed to amortize the cost-of-entry at the introduction of a new process technology.
Performance. To get it right, you need a foundry with an Open Innovation Platform® and process technologies that provides the flexibility to expertly choreograph your success. To get it right, you need TSMC.

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Supply chains are as much an economic, as a manufacturing phenomenon. Somewhat similarly, the illegal production of counterfeit electronic components is an activity that is highly dependent on economics. With this in mind, there are a couple of facts that can serve as guideposts for implementing a tangible strategy for best practices to combat the counterfeiting of electronic components:

▪ The always shifting economic climate and geographic location of manufacturing opens opportunities for counterfeiters and challenges for manufacturers
▪ Implementing an encompassing quality management systems (QMS) within your own organization is an essential first step to risk management.

Challenges Come from Structural Changes
In response to increased margin pressures and lean inventory management, today’s global electronics supply chain has, over many years, promoted geographic manufacturing clusters. This type of structure is evidenced in the many industrial parks where manufacturing partners cluster to reduce logistical costs and improve collaboration, as well as quality oversight.

Simultaneously, the supply chain has moved to a Japanese tiered structure, as presented by Thomas Choi and Tom Linton in their December 2011 article in *Harvard Business Review*. As Choi & Linton explain, these tiered-structures can be understood as an ordered set of layers or hierarchical tiers, where in response to controlling costs through outsourcing, large OEMs focus their relationship on their top-tier supplier who is responsible for managing the sub-tiers that comprise the manufacturing and procurement supply chain. Again, a highly efficient system that addresses lean management goals, but also exposes the OEM to significant risks as a result of decreased visibility into the entire supply chain.

Among the serious risks from decreased visibility are production slowdowns or stops due to unforeseen disruptions (e.g., natural disasters, merger and acquisition (M&A), insolvency, etc.), and increased exposure to counterfeit or non-conforming parts. The reason that global semiconductor supply chains face an increase in risk to both disruptions and quality can be traced back to the visibility point. The funneling of various sub-tiered suppliers and manufacturers into localized areas means that when a natural disaster, power failure or other disruptive event occurs, more of the supply chain is affected. The greater the number of sub-tiered supply chain partners affected, the greater the chance of a longer or more severe disruption, such as witnessed with the 2011 natural disasters in Japan and Thailand.

The decrease in visibility is not just from the funneling of supply chain partners by clustered geographic location, or agglomeration, but also from funneling the engagement with each supply chain partner into the hands of the top-tier partner. In other words, outsourcing supply chain management by pushing more responsibilities to first-tier suppliers means that the OEM loses insight to the various partners selected along the supply chain, and this is where quality risks occur.

It is essential, not only for market agility and business strategies, but especially for quality management and anti-counterfeiting that visibility is not only maintained, but also kept at the forefront.

Given that the semiconductor and electronics industry supply chain continues to increase in complexity as it evolves, how do those of us along this chain respond? Are there tangible means for mitigating these risks that can be readily implemented without having to move mountains and change the industry, which is more than any single business strategy can do? Indeed, the answers are happily more straightforward and familiar than one might think. These risk mitigation solutions are ones that can be found in place across the supply chain by those companies pursuing best-in-class QMS.

Building on Standards
Let’s start with the importance of QMS and why we need to remember that QMS is not just something handed down from executive offices. When QMS is truly adhered to, it means that everyone in the organization not only understands but also follows the QMS regularly and in every aspect of their daily business.

To best understand how to go about ensuring that QMS is part of the daily fiber of an organization, and how to make sure that you are choosing value chain suppliers who provide true quality services, you need to start with requiring industry standard certifications. Certifications that are widely recognized are also those that have published requirements and use third-party auditors to certify companies. This process gives an unbiased evaluation of the
Ongoing Vendor Management

In global semiconductor supply chains, it is important to require that companies have various certifications, registrations and affiliations. A list of the most important for distributors include, but are not limited to the following:

- ISO 9001, ISO 17025 and ISO 14001
- ANSI ESD S20.20
- IDEA-STD-1010-A, IDEA-ICE-3000 and IDEA-QMS-9090-A
- CTI-CCAP-101
- AS 5553 and AS 9120-A
- GIDEP
- C-TPAT
- ISA
- IPC-A-610 and IPC J-STD-001
- CAGE codes (for US government contracts)

While there are many relevant and essential standards that you should expect a distributor to be certified to, it is equally important to understand that these QMS standards are just the starting point. Through careful due diligence and auditing processes, ensuring that your supply chain partners have the essential standards in place and weave in their own set of processes and procedures is the best and most time-tested risk management approach that can be recommended.

One example of what to look for in a supplier’s internal processes beyond QMS certification standards, is their vendor screening processes and procedures. The true first line of defense against counterfeit or non-conforming parts is a stringent vendor screening and vendor management system (VMS). This requirement might sound routine, but a solid VMS is going to present many opportunities to diversify a procurement supply chain, on to ensuring that only quality parts are sourced. In reviewing a VMS, there are a few key aspects that should be in place, known and understood throughout the organization, and be used in every applicable instance. These aspects can be generalized into three main areas to provide a generalized understanding:

**Vendor Screening**
- Formal selection process
- Vendor application
- Vendor performance metrics
- Vendor audits

**Ongoing Vendor Management**
- Internal Vendor Rating System (VRS) based on:
  - Performance
  - Credit worthiness
  - Delivery record
- Regular auditing of approved vendors
  - Certifications
  - Laboratory and testing facility certifications

**Custom Sourcing**
- Based on customer specifications
- Customized Certificates of Conformance (CoC)
- Other customized requirements

In the end, beyond certification standards and regular audits of suppliers, visibility and knowledge are at the core of successful risk management in the global semiconductor supply chain.

**Careful Diversification Brings Opportunities**

After careful screening and vendor selection, it becomes possible to add a next layer of risk management, that of supply chain diversification. With the knowledge of, and visibility into a supply chain partners’ QMS and operational processes and procedures, it is possible to then mitigate the risks of single- or limited-sourcing by strategically branching out to include a second line of approved suppliers in the event of disruptions, shortages or the need for greater market agility.

The careful selection and then extensive screening and due diligence process for approving new suppliers for procurement ought to be a meticulous process. The risks of a poor selection are great, and the responsibilities continue to increase, both by enforcement agencies and within the industry, to protect against the introduction of counterfeit or non-conforming product and to report instances of fraudulent parts into the supply chain.

As the global semiconductor supply chain continues to evolve, best practices will similarly evolve. However, the most tried and true risk management practices are still the most successful. Namely, requiring industry-recognized QMS and testing laboratory certifications, ensuring visibility into the entire procurement and manufacturing value chain, regular vendor screening and VMS implementation along the value chain, and ensuring that supplier diversification strategies are kept up-to-date with open lines of communication. After all, disruptions generally do not occur at convenient, nor regular intervals, and when they do, rather than facing serious challenges, a well-prepared company will find market opportunities instead.

**About the Authors**

Kirk Wehby joined Smith in 2008 to head worldwide operations and quality. He was formerly director of operations and supply chain for Cardone Industries (1997-2008) where he managed start-up and integration of operations in Belgium and Mexico. Kirk received a BS from Oral Roberts University and an MBA from Westchester University. Kirk can be reached at kwehby@nfsmith.com.

Lisa Ann Cairns joined the Smith network of businesses in 2001 as a technology strategist and became the chief strategy officer for a Smith subsidiary the following year. Since 2007, Lisa has been involved with strategic marketing projects for the Smith network and is the senior market analyst & contributor for Smith’s MarketWatch. Lisa received her Ph.D. (1998) and AM (1992) from The University of Chicago and BA from Hofstra University (1988). Lisa can be reached at lcairns@nfsmith.com.
CamSemi is an emerging leader in power management ICs for optimized cost and energy-efficient off-line (i.e. mains voltage connected) power conversion. The company’s unique patented solutions and approach help many of the world’s top electronics original equipment manufacturers (OEMs) to develop smaller, lighter and more energy-efficient mains-powered products while also reducing their design timescales and manufacturing costs.

The company continues to enjoy rapid market share growth in external adaptors and chargers in its core application areas. CamSemi works with leading suppliers in SOHO networking products and mobile consumer space – which includes both cordless and mobile phones and cameras. New product announcements extend the power and performance capabilities of its products to consumer tablets and also allow original design manufacturer (ODM) & OEM partners to meet the ever more stringent requirements for more energy-efficient end products, such as those being introduced in 2013 under the EU eco-design directive for Energy-Related Products.

CamSemi’s desire to deliver significant energy savings has led the company into the solid state (LED) lighting space where it offers best-in-class solutions and efficiency improvements of more than 500 percent compared with traditional filament lamps. The company’s “Standards Time” blog – at www.camsemi.com/standards-time-blog - has been specifically created to highlight the latest proposed changes to mandatory and voluntary regulations for power supplies and solid-state lighting products.

Over the years CamSemi has received a number of awards for its technologies, products and commercial achievements and recently announced that one of its founders, Professor Florin Udrea, was awarded a Silver Medal from The Royal Academy of Engineering for his pioneering work in Ultra High Voltage power devices and CMOS sensors. He co-founded CamSemi with Professor Gehan Amaratunga, who was elected a fellow of the Academy in 2004 and also received its Silver Medal in 2007.

Abilis Systems, a Kudelski Group company, a fabless semiconductor company headquartered in Geneva, Switzerland. Abilis is provides ICs for the digital TV market and has sold over 100 million units to consumer electronic customers across the world.

The current media and digital TV landscape is showing important market shifts, in particular, the evolution of media convergence, home networking content propagation, media gateway and over-the-top (OTT) content delivery ("Anywhere and Anytime”).

This is driving the need for highly secure video stream processing and distribution from a wide range of broadcast network and Internet sources to a variety of end user devices, including multiple set top box (STB)/digital TVs (DTVs), PCs and mobile devices over both wired and wireless networks.

Abilis is developing a family of highly secure multi-stream media gateways to enable the reception of DTV streams from different sources and secure distribution over wired and wireless Internet protocol (IP) networks to multiple end user devices. The ability to protect premium content is one of the most serious concerns facing the industry.

Abilis has a unique technology and market position to enable secure distribution to multiple screens in the home. Abilis plans to introduce its first secure broadcast (TS)-to-broadband (IP) transport bridge device in 2012.

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– Yves Mathys – CEO, Abilis Systems

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ANATOMY OF A SUCCESSFUL SUPPLY CHAIN INTEGRATION

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Collaboration is essential for semiconductor companies today. Nowhere is this more true than supply chain integrations for outsourced production processes. Semiconductor companies and their suppliers need to exchange information as seamlessly as possible to ensure timely and accurate inventory production. This article looks more deeply into this topic from three unique perspectives. The semiconductor company, the supplier and the supply chain provider all add their unique voices to this topic. The three companies collaborated in the supply chain integration for the semiconductor company.

This type of information exchange collaboration benefits from understanding each perspective on three questions: (a) What are your goals for the integration? (b) What tips do you have for effective partnering? (c) Can you apply these goals and tips to a sample project implementation?

Participants Overview

The three companies supporting this article include a fabless semiconductor company, an assembly and test provider and a fabless semiconductor industry supply chain management (SCM) provider.

What are Your Goals for Supply Chain Integration?

Fabless Semiconductor Company
An accurate and up-to-date view of work in process (WIP) and activity to support planning and customer fulfillment is needed. Meeting finance department requirements for procurement management, transaction traceability and inventory tracking to manage expenses and to value inventory are also needed. Without supply chain integration, information is entered manually, which delays insight and introduces possible human error. With the supply chain integration, the information comes straight from the supplier’s system and is pre-processed by the SCM provider and is then checked by our operations team before being allowed into its system.

Assembly and Test Provider
Data integration and reporting are viewed as a high priority service to customers, and a centralized data warehouse for all worldwide operations is key and requires significant investment. There are external and internal goals for this investment. These include providing customers with near real-time high quality production data that supports their internal business process and helps them reduce costs and increase productivity. Internally, this should be done as repeatably and efficiently as possible. Custom integrations for each customer slow the ability to meet customer goals, increase internal costs and can impact the quality of the data since non-standard processes are used in customized routines. One preference includes implementing business-to-business (B2B) reporting using an industry standard such as RosettaNet, or a data warehouse-driven customer portal and data repository.

SCM Provider
SCM integration should be approached as a service. While there is technology involved with the delivery, the customer goal is the ongoing successful operation of the SCM integration, rather than software deployment. Responding and addressing any issues that arise, no matter what the source of the issue is necessary. All goals relate to the quality of the service provided and the effectiveness and efficiency of the team in providing the service. Like the assembly and
test provider, repeatable, robust and sustainable processes are desired. SCM providers want the best quality data possible, so seek to leverage standard supplier processes rather than asking them to adapt to us. SCM Providers also need to build in responsiveness, and to monitor the health of many simultaneous integrations, so should look for built-in monitoring and communications along with appropriate error trapping and precautions to handle the unexpected.

What Tips Do You Have for Effective Partnering?

Fabless Semiconductor Company
The most important learning experiences revolve around the importance of communication at every step of the process. In the beginning it is important to establish basic definitions. It may appear clear what good outs, yield loss and vendor loss are, but data definitions – even for fairly common information in some cases – are not universal. Supplier billing might be based on one step in the process, while the production receipt from supply chain integration might be from another step. The number of outs from these steps might be the same most of the time, but when discrepancies occur, it is very difficult to figure out the reason why. In addition, the procedures for common exceptions like reversals, where lots are sent back to previous steps or are merged and re-worked, need to be clearly defined so that the factory, supplier headquarters, supplier billing and the fabless company are in agreement about how to handle these occurrences.

Assembly and Test Provider
It is very helpful to identify and involve all stakeholders who will be directly or indirectly impacted by the B2B integration project. For this integration, the list included the assembly and test provider’s IT, factory, finance and sales teams; the semiconductor company’s planning, operations and finance teams and the SCM provider’s technical project team. This let us train stakeholders on how the B2B integration works: What are the key triggers? What is the critical data for reporting? How is the data being applied in the customer system? Once stakeholders are trained, they will understand how a change in process (manufacturing or billing) can impact the B2B integration and notify others of changes. Additionally, we are looking to develop test plans and scenarios that will validate that all requirements have been met during User Acceptance Testing (UAT).

Fabless Semiconductor Company
The amount of different UAT test cases was not expected at the start of our project – but we see how it is a critical part of ensuring the entire process works as needed. Beyond basic process and data definitions, it is important to establish the timing of when suppliers are to send transactions through their B2B feed. This has been an issue with many assembly and test suppliers at one time or another. Examples of timing challenges include the supplier sending invoices a few days before the supply chain integration data is sent, or sending test transaction data before the assembly data, or holding back on production data until after shipment or even sending no data at all unless requested each time.

SCM Provider
The tips above on specific communication topics are very important, including UAT. A project plan or task list based on best-practices, an ongoing commitment from decision makers, as well as the doers among the stakeholders, and the need to leverage a best-practices approach to the implementation are also necessary. Deviation from best-practices may be required – but should be explained and approved. While it may appear obvious, busy schedules and executive focus are not always easy to obtain. At the same time, getting all parties involved at the appropriate times remains critical for an efficient and effective supply chain. These projects are not massive efforts with hundreds of tasks, but they do require coordination among multiple teams in multiple time zones – all with multiple demands on their time.

Assembly and Test Provider
Any new business processes or data input requirements should be addressed ahead of the B2B integration project (i.e. change in customer part numbers to be reported or a new service being introduced) since this type of effort can be time-consuming and negatively impact the B2B project schedule. If such changes cannot be made ahead of the B2B integration project, then these activities should be planned for in the B2B Integration project plan.

Fabless Semiconductor Company
A third important communication requirement is the need for a clear escalation procedure – not just for the semiconductor company – but for the SCM and assembly and test providers as well, when problems with the supply chain integration occur. A daily e-mailed dashboard that shows what vendor files were processed without issues the night before, as well as those that may have failed, should be provided by the SCM Provider. With this daily e-mailed dashboard, both the fabless company and the SCM provider will know that there is an issue and to investigate. Knowing who to contact to quickly address the issue keeps the collaboration operational.

SCM Provider
Our final tip is to stress the importance of visibility in supplier data quality and successful B2B integrations. Integration quality can suffer from a lack of internal focus on the quality and repeatability of SCM integrations and perceived value at the executive level of collaboration. It is often amazing to see the impact of small changes, such as adding supply chain integration quality to the semiconductor quarterly supplier review meetings. Knowing what is important helps all of the collaborators deliver!
Customer-Driven Foundry Solutions

UMC's customer-driven approach is based on strengthening our partnerships with customers, providing competitive advanced technology, and committing sufficient capacity to secure mutual long-term growth opportunities. We offer advanced technology down to 28nm, multiple specialized technologies, and a broad IP portfolio including ARM, Faraday, and Synopsys offerings. These foundry solutions establish a comprehensive process platform to streamline our customers' path to SoC silicon success, for now and the future.
Up until the 1990s, companies in the semiconductor industry were usually vertically integrated, meaning that the development of process technology for manufacturing chips and the entire fabrication facilities were owned and operated by the companies themselves. In the 1980s, small companies began to form with a focus on innovative chip solutions. Since the production process of silicon is very costly, it was not financially feasible for small companies to produce the chips on their own production sites. A way around this was to ask for production capacity at integrated device manufacturers (IDMs) to produce their chips. Thus, the first model of a fabless IC company emerged. At the same time, the foundry industry was established as non-competitive manufacturing partners, which was essential for the viability of fabless companies.¹

This article describes how a former IDM company managed to become a fully fabless company. The company’s production of almost all of its back-end and test services was still with its former mother company and had to be transferred to new suppliers.

Project Set Up and Approach

The main working packages within the project were the transfer of wafer sort, assembly and final test to new suppliers, as well as qualification and system verification with the new material. The biggest challenge was to manage the high amount of transfers (233 products) in a short amount of time.

The major goal with this project was to simplify matters for all parties involved in the process. A project approach was developed that kept all efforts for customers to a minimum. Based on a newly implemented fabless sourcing strategy for assembly and test services, special focus was addressed to secure deliveries to customers by reliable service suppliers.

In the following the key aspects of the transfer approach are described.

Process Change Notification (PCN)

Bundling Approach

Before a change in the production process could occur, customers had to be informed of the changes, be given the possibility to qualify products and give their approval. In order to do so, PCNs were sent to all customers. Upon receiving the PCN, customers were given the opportunity to order samples for their own qualification.

With the aim of avoiding multiple qualification efforts for customers, the product transfer focused on application-oriented product bundles as opposed to single products. One PCN bundle included all products used for a typical set of applications. Through this approach, the qualification process was significantly simplified. Normally, more than 100 PCNs would have been required for the transition process, leaving customers to handle multiple PCNs at a time. Due to the bundling approach in this project, that number was reduced to 25, thus saving effort on all sides.

PCN Schedule

Several conditions for issuing PCNs needed to be established in order to keep efforts for customers to a minimum.

The respective PCN was sent out after all references (as defined for a bundle) had been qualified within the company. At the same time, the PCN samples were manufactured so as to ensure that they would be ready for shipping without delay when required by customers. Arrangements with suppliers were made so that qualified samples for all products of one bundle would be available within two weeks of PCN release dates at most. It was suggested that customers would order samples without delay. In addition, the qualification results from reference qualification were available at the PCN release date as part of the customer information.

Customer qualification was done according to international standard JEDEC.

Management and Feedback

The immense complexity of the project required exceptional tracking and feedback. For each PCN product bundle, a “Bundle Project Manager”, who was responsible for coordinating all activities, such as tracking milestones, aligning in cross-functional projects (CFPs) and
releasing PCNs to customers was defined. A Microsoft Excel-based tracking software was established for feedback and keeping track of all the files.

**Test Transfer**

Thirty wafer test packages and 134 final test packages were transferred. Whenever possible, the same tester and testing hardware and software as well as standard IC packages were used. If identical test platforms and test houses had already been established for any products, no PCN was issued. All other test transfers were explicitly stated in PCNs.

**Qualification**

Every product needs to be qualified after transferring the production to new suppliers. In order to reduce the number of products for qualification and thus the efforts at qualification, similar products were organized in appropriate packages. The most complex products of these packages served as reference products and thus were the only ones that needed to be tested. The number of reference products per package platform depended on the numbers of suppliers, critical packages and wafer suppliers used. In addition, products had to undergo a series of tests, such as Basic System Tests, High Temperature Storage Test, Solder Simulations and Unbiased Highly Accelerated Stress Test (UHAST). After these tests had succeeded, qualification reports were written for the products and packages were internally released.

**System Verification (see Figure 1)**

Subsequent to qualifications, the products had to be verified within application-oriented bundles. Once all reference product qualifications needed for one application were approved, IC combinations underwent a system test for each application bundle.

For some products it was impossible to avoid combining old and new materials. These in particular needed to be considered in system verification. Each device could be identified with old or new material by the printed lot-number.

**Figure 1: System Verification per Bundle.** First, all products were qualified. Second, the system application was verified using the entire set of products. Only if the system test passed the product bundle was released to the customer.

**Milestones**

In order to track the progress of the project, a milestone plan was implemented. These milestones tracked and controlled wafer test, assembly, PCN releases, final test, qualification, verification and logistics. Figure 2 gives an overview of the major milestones and their intercorrelations though merely displaying a very simplified version. The first milestones marked the availability of test cells for wafer sort and test and respectively the availability of samples for assembly. As this was achieved, the test packages for wafer sort and test, and accordingly, the production for assembly were released. When the internal qualifications were terminated, PCNs were sent out to customers. After the approval of the PCNs by customers, two milestones marked first the start and then the completion of the volume shift for each wafer sort, assembly and test. The final milestone represents the termination of the production transfer. In reality, there were a lot of intermediate milestones – about 25. Considering that 233 products needed to be transferred, this resulted in roughly 6,000 milestones for the entire transition process.

**Process Stress Test**

In order to identify and decrease risks during the transition process, a Process Stress Test was established implementing a product specific transfer risk assessment. In meetings, risk topics were discussed and actions determined to limit these risks and prevent complications. About 80 percent of the high risk topics were continuously reduced to medium or low risk topics. Certain risks were not possible to eliminate (such as global disasters), but close monitoring ensured that the quick response was implemented in case of any issues.

Topics that were tackled within the stress test included improving the PCN status tracking and the technical preparation of sample runs within qualification, amongst many more. Purchase orders and sample transactions were followed up with great detail on a daily basis.

**Communication**

Sustaining and strengthening comprehensive communication within the company, as well as with suppliers and customers greatly contributed to making this a positive and smooth transition process. A constructive communications program was established with customers and suppliers. In the beginning of the project, the sales department arranged a customer road show with face-to-face meetings to go along with the information package. The goal was to get general feedback from customers of the project impact on their side and get information on the customer’s qualification plan. In order to strengthen communication with customers throughout the project, proactive information communication to customers on the project progress was established. In addition, the chief operating officer (COO) visited key customers and suppliers on a regular basis to keep up a positive communication level and support. This was especially important in order to give customers extensive support for qualification.
Continuing the capital-lite start-up investment theme from the last column, this issue features Ambiq Micro, which has delivered its first product with a scant few million in funding. Ambiq was founded in 2010 and is backed by DFJ Mercury, ARM, Huron River Ventures, Draper Fisher Jurvetson and several other investors.

Ambiq's founders have been designing ultra-low power ICs since 2004, with technology pioneered at the University of Michigan. This technology includes a range of analog and digital intellectual property (IP) targeted at nanoamp operation, perfected over a six-year period by University researchers and over a subsequent two-year period by Ambiq engineers.

Leveraging its Sub-threshold Power Optimized Technology (SPOT), Ambiq's approach to low power is comprehensive, from the transistor level up, through the architecture level. Ambiq has produced 32-bit ARM Cortex-M class processors that are more energy-efficient than the simplest 8-bit solutions on the market today. The company is currently focused on energy efficient timing ICs, power management ICs and microcontrollers that solve the most demanding system requirements for battery life, enabling months, years or decades of operation.

In early 2012, Ambiq unveiled the AM08XX and AM18XX families, two of the world’s lowest power real-time clock (RTC) chips. Typical active current ranges from 15 to 55 nA, which is an order of magnitude lower than competing devices. Ambiq argues that its devices enable 20 times better sleep mode, powering MCUs down to zero, and overall two to 10 times better active power consumption.

The Ambiq RTC families are targeted at applications such as real time backup, wireless sensors and tags, and smart cards and security tokens. Additional target applications include medical electronics, utility meters, data loggers, handsets, consumer electronics, appliances and more. Ambiq believes the market size for RTCs and PMICs is several billion dollars with a current target market size of 300Mu.

Going beyond simple RTC functionality, Ambiq has extended the functionality of its devices by adding advanced power management capabilities. A patented on-chip Power Switch and System Sleep Manager allow the AM18XX family to be used as a supervisory element in a host microcontroller–based system, minimizing the overall power used by other system components.

Ambiq plans to extend the capability of its devices in future versions, offering devices with multiple power zones, as well as more highly integrated PMICs, including devices with integrated ARM processors. In the near-term, Ambiq plans to focus on developing a family of ARM-based microcontrollers that apply SPOT to the analog and digital domains, including the peripherals. The company is developing a micro-display controller that integrates an ARM core, display driver, GPIO and button management for a targeted high volume consumer market. Compared to existing alternatives, the device will have lower power, as well as additional features.

Ambiq plans to accomplish all of this without seeking the tens of millions of dollars that is typically required by most startups – an impressive, and in this day and age, necessary accomplishment.

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In 2011, the global semiconductor components market generated over $300 billion in revenue according to Gartner. With the exception of the great recession of 2008 and 2009, the semiconductor industry has continued to demonstrate consistent growth since 2002 with a compounded annual rate (CAGR) of 7.7 percent and is projected to reach $413 billion in revenue by 2015.

As the cost to develop next generation solutions at advanced geometries continues to rise, many have maligned the semiconductor market as a commodity space with a rapidly slowing growth profile. However, semiconductors continue to penetrate an increasing number of products and applications. With no sign of this penetration changing anytime soon, semiconductors will continue to be a vital component in the value chain for the foreseeable future.

Innovation Challenges are Mounting as Costs Rise

Since Gordon Moore defined Moore’s Law in 1965, the semiconductor market has experienced an extremely high rate of development and innovation, fueled by a plethora of investment by the venture capital (VC) community. However, in recent years VCs have dramatically reduced their investments in the space (both total capital invested and number of investments) citing a multitude of challenges as the cause for diverting their funds to other opportunities and sectors (e.g., clean tech, SaaS, cloud computing, online gaming, social networking, etc.). Many VCs believe that building a successful semiconductor company absolutely requires large capital investments ($50 million plus) to cover the increasing cost of mask sets, tape-outs, design tools and talented technical and executive teams (a notion that this article seeks to dispel). In addition, many VCs fleeing the space believe that investments in semiconductor start-ups overall have not delivered positive cash-on-cash returns (another notion that this article seeks to dispel).

As a result, the number of new semiconductor companies based in the Western Hemisphere (North America, Europe and Israel) receiving early stage funding (seed and series A) has dropped off significantly in the last five years. As illustrated in Figure 1, during 2003 and 2004 over 60 semiconductor start-ups received initial funding each year, but in recent years that figure has declined to less than 20 companies annually. This steep decline in start-up funding is expected to create a significant innovation challenge for the industry as a whole, and for larger public semiconductor companies specifically, over the next five to ten years. In the short-term, larger public semiconductor companies will see fewer and fewer high-growth start-ups available for acquisition, and in the long-term they will be forced to shift away from acquisitions as a strategy for innovation and growth. Instead, larger public semiconductor companies will be forced to fund next-generation technology developments with cash from their own balance sheets and recognize increased development costs in their ongoing R&D expense line.

Figure 1: Growing Disparity Between Early Stage Funding and M&A Exits

**A Perspective on Semiconductor Investment Returns: 2002 – 2011**

Charles Welch, Managing Director, Pagemill Partners
Matt Sachse, Managing Director, Pagemill Partners
Jared Furutani, Associate, Pagemill Partners
Do Investments in Semiconductor Start-ups Present a Compelling Opportunity?

With the number of early stage investments in Western Hemisphere-based semiconductor start-ups at a 10-year low and VC investments in other sectors proving to be equally challenging (with a few exceptions), many investors are considering whether the investments in semiconductor start-ups have delivered positive returns historically. The remainder of this article is focused on analyzing exits of private companies in the semiconductor sector, between 2002 and 2011 and responding to the following question:

“What cash-on-cash returns have venture investors actually realized from private semiconductor targets they have exited (IPO, M&A or bankruptcy) from 2002 through 2011?”

Summary of Analysis and Results

Venture investment and transaction data on privately-held semiconductor companies based in the Western Hemisphere was aggregated using various resources, databases, publications and proprietary sources. Between 2002 and 2011, approximately 487 privately-held, VC-backed, semiconductor exits were included within the scope of the analysis; 30 of those companies successfully completed an IPO, 362 exited via M&A transactions and 95 start-ups went out of business. As with any quantitative analysis, a number of challenges were experienced related to incomplete or undisclosed data, and therefore it is important to understand the scope of the analysis and the assumptions used throughout, which are highlighted at the end of this article. The following sections present the results of the analysis and provide various perspectives based on criteria such as exit type, total invested capital and exit year.

Overall Returns by Exit Type (2002 – 2011)

The aggregate venture investment in the 487 Western Hemisphere-based private company exits analyzed totaled an estimated $18.2 billion and returned to investors an overall exit value of $22.4 billion or approximately 1.2 times invested capital. IPOs as a group generated the strongest returns to investors, producing an aggregate exit value of $7.0 billion or approximately 3.3 times invested capital. However, most semiconductor start-ups are acquired well before the company reaches the business and financial maturity needed to complete an IPO. The 362 M&A exits during the analysis period returned $15.1 billion of exit value to investors, representing a more modest aggregate return of approximately 1.1 times invested capital. Start-ups that went out of business accounted for 20 percent of the number of exits during the period, but only 13 percent of overall invested capital, indicating that prudent VCs are often able to identify poor investments and cut their losses before they consume a disproportionate amount of available investment funds.

Returns by Quartiles (2002 – 2011)

When looking at the consolidated investment and exit value data of all 487 companies, ranked based on exit value multiple of invested capital and grouped by quartile, companies in the first and second quartiles generated aggregate exit values of 4.5 times and 1.2 times invested capital, respectively. In fact, contrary to the belief held by many VCs that semiconductor start-ups rarely return capital to investors, the top 40 percent of all transactions resulted in a positive cash-on-cash return.

As shown in Figure 2 below, when IPO and M&A exits are separated and then broken down by quartile, the exit value multiple generated by top performers in each category increases substantially.

The top seven IPO exits returned 9.1 times invested capital, while the second and third quartiles returned 4.5 times and 2.9 times invested capital, respectively. By comparison, the top 25 percent of M&A exits, composed of 90 transactions, generated an aggregate return of 4.6 times invested capital, illustrating that companies with relevant and leading technologies do not have to complete an IPO in order to generate solid returns for their investors.

Returns by Total Invested Capital (2002 – 2011)

As development costs continue to rise (mask sets, design tools, skilled technical teams, etc.) semiconductor start-ups that are developing technologies at leading edge geometries and using exotic materials will continue to require larger investments. As shown in Figure 3 below, there is little correlation between invested capital in a start-up and cash-on-cash returns generated at exit. The 202 semiconductor start-ups that exited during the period with less than $25 million of VC funding generated an overall return of 2.0 times invested capital. However, companies with large levels of investment have produced significant returns in select instances; P.A. Semi (2.2 times invested capital) and Beceem Communications (3.3 times invested capital) are a couple of examples.
SOLVING 3D-IC ECOSYSTEM CHALLENGES

Ken Potts, Chairman, GSA 3D-IC Working Group

The semiconductor industry has been following Moore’s Law for the last 50 years through the continued advancement of planar integration technology and techniques. We have been able to move the minimum feature geometry from 10µm to 20nm today, and will move to 10nm sometime in the next 10 years.

That being said, there are a couple of huge issues with planar integration. First, we are running out of the electron density needed to ensure stable and robust storage elements. This pushes the industry to explore new technology. Resistive DRAM and spin-transfer torque memory are examples of how our storage elements may evolve to enable us to continue pushing toward planar integration. However, new technology is expensive, and that brings up the second main issue of our planar integration roadmap – cost. A $10 billion fab presents a significant expense, and there are few designs today that have the volume level and sustainable market margins to make the investment economically viable.

There is a growing industry consensus that three-dimensional ICs (3D-ICs) can offer a seamless convergence of performance, power, capacity and form factor. The ongoing demands of end users – reducing power, increasing performance, improving time to market and reducing product risk – can all be addressed by a viable 3D-IC approach. This isn’t a new idea. The original patent with claims describing a 3D-IC was awarded in the early 1960s. Today, the 3D-IC discussion is focused on 3D heterogeneous stacked dies (such as logic and memory) with through-silicon vias (TSVs), as well as “2.5D” implementations in which dies are placed side-by-side on a silicon interposer.

Since early conceptualization, there has been quite a bit of research activity, as well as isolated examples of commercial 3D-ICs. This is most commonly seen today in the case of sensors like Sony’s back-illuminated sensor (BSI) for high-quality image and movie capture for smartphones, and stacked Elpida (Micron) DRAM modules. More recent examples include the often-cited Xilinx 2.5D field-programmable gate array (FPGA) and demonstrations of early 3D-IC work from Samsung, TSMC and ST Microelectronics.

It is clear from the wealth of activity in the 3D-IC area that the technical barriers won’t stay barriers for long. 3D-IC is a very integrated technology for which value creation is required at every step of the supply chain. Broad and deep activities are underway to realize the ultimate promise of 3D-ICs. The challenge lies in addressing the business issues posed by a disaggregated supply chain, and one requirement is standards.

Disaggregated Supply Chain Collaboration

Currently there are standards activities ongoing at the Silicon Integration Initiative (Si2), SEMI and at Sematech. The IEEE P1838 Test Working Group is working on 3D-IC design-for-test (DFT) architectures. In the memory domain, there is strong activity in JEDEC, which has ratified the Wide I/O memory standard. Micron and Samsung have jointly announced the formation of the Hybrid Memory Cube (HMC) consortium, which seeks to develop HMC stacks that can be integrated into 3D-IC systems. Figure 1 shows the types of design standards that are needed in the 3D-IC supply chain.

Figure 1 – Cooperation Throughout the Supply Chain is Needed to Develop 3D-IC Standards

Every major semiconductor research institution in the world is running projects to create solutions for the technical problems. Every major semiconductor manufacturer and design house are actively looking at how to leverage 3D-ICs. Electronic design automation (EDA) companies are investing in the tools and methodologies to make the promise of 3D-IC realizable. Intellectual property (IP) vendors are actively looking at their IP and determining extensions required to enable their IP to scale to the 3D-IC context. With this kind of industry-wide focus, it is safe to say that the technical issues will be overcome. What may be more interesting is how we as an industry address the considerable business challenges created by the 3D-IC paradigm.

Disaggregation Challenge

The electronics industry was once dominated by integrated device manufacturers (IDMs). We didn’t call them that because they were simply companies that owned everything from concept through packaging. The supply chain consisted of the IDM, the semiconductor equipment provider and wafer processing and packaging materials suppliers. In this supply chain structure, 3D-ICs would only pose the overall question of ultimate return on investment to the IDM. Internal margin tradeoffs could be made between different steps
in the process to achieve the desired economic result. Faced with a technology development imperative like 3D-IC, the IDM could bring all their resources to bear and do the technology and business development necessary to ensure return on investment.

In the case of 3D-ICs, it might cost more in the process and package, but that could be mitigated by differentiation and improved margin. When it came to warranty and profit sharing, the IDM could handle revenue allocations internally. The downside of this was that the IDMs were limited by their scale and time to market for new technology. IDMs were uniquely positioned to solve the technical issues as long as these issues didn’t exceed their innovation capacity.

Once the fabless model came on scene, the IDM acronym was created. Today, there are few true IDMs and none that can respond alone in the 3D-IC context. The disaggregated supply chain enables competition in each of the critical supply chain dimensions and, as a result, has the potential for much more rapid convergence on a technical solution in a given area. In a topic area as complex as 3D-IC, the investment that would be required for an IDM to solve all issues would be prohibitive from a headcount and financial standpoint. Thus, the disaggregated supply chain is clearly a necessary market structure to bring 3D-ICs as an economically viable reality to the semiconductor industry.

**Business Model Challenges**

Some would say that 3D-ICs shift value creation to the package domain. Design, manufacturing, EDA, IP and OSAT companies all argue that a significant portion of the value creation is from their domain. Interestingly enough, in the 3D-IC context, all of the supply chain domains must innovate for semiconductor companies to realize an economically viable 3D-IC capability.

So where are the dollars, both positive and negative? If there is a $100 million system-on-chip (SOC) design that realizes an additional 15 percent in gross margin due to the utilization of 3D-ICs, does the design company get all of the margin? Obviously, it cost the manufacturer to add 3D-IC capability, so how much beyond normal markup of costs is fair? How do EDA and IP vendors get paid for their contributions?

With the current EDA licensing model, it is hard to see how that portion of the supply chain can be justly rewarded for the contributions necessary for 3D-IC realization. On the IP side, it is a little easier to see, as there is a concept of technology access and royalty. What about the “negative” dollars? Said another way, what happens when a $100 million project misses a market window because of a 3D-IC manufacturing problem traced back to a piece of faulty IP in the stack that failed because the thermal analysis was off by an order of magnitude because of a bug in the EDA tool? We all know that $100 million projects are chasing billion-dollar opportunities, so the scale of the preceding warranty scenario is daunting.

Everyone in the supply chain wants to be rewarded when good things happen. Will they also be there to indemnify losses created by their actions? In the world of 3D-ICs, we see all sorts of approaches that are reacting to this warranty reality. For example, TSMC’s 2.5D Chip-on-Wafer-on-Substrate (CoWoS) process requires die manufacturing and assembly to be performed in-house at TSMC. What happens when part of the die stack isn’t manufactured by TSMC?

The Global Semiconductor Alliance (GSA) 3D-IC Working Group’s vision is to build a consortium of leading representatives within the 3D-IC ecosystem in order to accelerate the adoption and commercialization of 3D-IC technology through collaborative efforts. The Working Group is a neutral, non-competitive forum. The group consensus is that the key barriers to widespread 3D-IC adoption are technology maturity and business model viability. As the group explores these two issues, member companies represent their interests while helping to stimulate and shape the overall adoption of 3D-IC technology. The Working Group forum facilitates communication and shared knowledge base across the 3D-IC supply chain (IP, EDA, packaging and test, foundry), which improves efficiencies and collaboration. Members also are able to present their accomplishments and solicit input on key challenges. More information can be found at http://www.gsaglobal.org/working-groups/3d-ic/.

**About the Author**

Ken Potts’ background is a unique blend of practical electronic and mechanical engineering experience, including marketing, sales, executive management and entrepreneurship. After receiving a BSEE from Montana State University, his engineering career has been spent in advanced development groups for the U.S. Navy as well as two Fortune 500 companies. He has also been a consistent contributor to innovations in solid-state lasers, neural networks, 3D-IC technology, high-performance chipsets and graphics processors, and he is a co-inventor on five U.S. patents. Since moving into the EDA and IP industry, he has held several product and services marketing, as well as sales executive positions at Cadence Design Systems and Virtage Logic. In his current position at Cadence, Potts is responsible for leading the company’s strategic planning process. Ken can be contacted at kpotts@cadence.com.
Semiconductor Leaders Use Model N To Improve Margins

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Returns on Semiconductor Investments Much Better Than Expected

Returns on semiconductor investments over the last decade have outperformed the perception of many in the VC and hardware technology communities. Of the 487 privately-held, Western Hemisphere-based, semiconductor company exits that were analyzed, nearly $23 billion of value was returned to investors, resulting in an overall cash-on-cash return of 1.2 times invested capital. Not only have investments in semiconductor start-ups resulted in positive cash-on-cash returns, the industry has shown a surprising level of consistency over the last ten years; only 2008 and 2009 (i.e., the great recession) resulted in annual losses on semiconductor company exits. Finally, despite the rising costs of developing solutions at leading-edge process technologies, only five percent of semiconductor start-ups analyzed (26 companies) raised more than $100 million. In fact, about 75 percent (366 companies) received less than $50 million of VC investment and 41 percent (202 companies) received less than $25 million of VC investment. This latter fact directly conflicts with the typical perception of what a semiconductor company/investment requires to reach the maturity necessary for exit.

Future Implications on Semiconductor Returns

Many global semiconductor players still rely heavily on private company acquisitions to accelerate growth, strengthen their product/IP portfolios and build strong technical development teams. Over the last decade, the number of private semiconductor acquisitions ranged from 33 to 62 transactions per year (including companies without VC funding), with an average of 51 transactions annually (including IPOs). As previously illustrated in Figure 1, a significant imbalance is building between the projected demand for semiconductor start-ups as M&A targets and the number of VC-backed semiconductor start-ups receiving early stage funding. However, the disparity between new start-ups and historical levels of M&A should bode well for investors. With fewer competitors and greater scarcity value, private semiconductor companies should realize increased valuations upon exit due to competition amongst buyers.

Conclusions

As many VCs have recently been inclined to invest in other technology sectors, the next several years will be critical in the development of the innovation model that has served the semiconductor industry well in the past. Despite the beliefs of many VCs, there are still numerous segments within the semiconductor industry that do not require outsized amounts of capital to build a successful company (e.g. analog/mixed-signal). While the greatest cash-on-cash returns to investors are still generated through IPOs, sizable returns are also generated through M&A exits. As the scarcity value of start-ups in the semiconductor space continues to grow, we believe there is a significant opportunity for skilled semiconductor investors to realize excellent returns on their investments.

About the Authors

Charles Welch is a managing director at Pagemill Partners. Charles has extensive experience in mergers and acquisitions, business and corporate development, finance, capital raising, investor relations, human resources and law. At Pagemill Partners, he has successfully completed numerous M&A and strategic capital raise transactions. Prior to joining Pagemill, Charles co-headed the Semiconductor, Communications Equipment and Diversified Transactions practice groups at SVB Alliant, the then investment banking arm of Silicon Valley Bank. Before SVB Alliant, Charles was the vice president, finance, corporate development & strategy at NetScaler, an Internet infrastructure company that was eventually acquired by Citrix. Prior to that he held the position of vice president, corporate development at Selectron, an EMS company, and was the vice president, business development and general counsel at SMART Modular Technologies, a memory module manufacturer that was acquired by Selectron. Charles was also a corporate securities attorney at Wilson, Sonsini, Goodrich & Rosati. Charles has a bachelor of science degree in civil engineering from Virginia Tech, a masters in real estate development from the University of Southern California, and a J.D. from the University of California at Berkeley (Boalt Hall School of Law).

Matt Sachs is a managing director at Pagemill Partners and brings more than ten years of transaction experience to the firm, including completed transactions representing over $1.5 billion in aggregate value. Matt has spent his entire career representing information technology companies in transactions and his execution experience spans both software (wireless, infrastructure, embedded) and hardware (telecom, semiconductors, storage, photovoltaicsolar) segments. Prior to Pagemill, Matt was a vice president at SVB Alliant, where he provided a variety of advisory services to technology clients worldwide. He was also responsible for managing the firm’s activities in consumer and wireless markets. Previously, Matt worked in the technology investment banking practice of SoundView Technology Group, where he was responsible for the execution of public and private equity transactions for leading software, semiconductor and communications companies. Matt holds a bachelor of arts degree in economics from Stanford University.

Jared Furutani is an associate at Pagemill Partners and has over four years of investment banking experience. Jared joined Pagemill in 2009 and has worked on numerous M&A and private capital raise transactions while with the firm. Previously Jared served as an analyst with Duff & Phelps Securities, where he worked in their investment banking group. Prior to working at Duff & Phelps, Jared provided assurance services with PricewaterhouseCoopers (Los Angeles) for both SEC and privately held clients, with an emphasis on technology and middle market sectors. Jared is a graduate of the University of Washington, where he earned a bachelor of arts degree in accounting and information systems and is a Certified Public Accountant licensed in the State of California.

Pagemill Partners, a Duff & Phelps business, (www.pmih.com) is a premier investment bank located in Silicon Valley. Pagemill has built a solid track record of completing successful transactions for middle market technology companies. With a specialization in merger and acquisition advisory, the firm has completed more than 115 transactions since 2008, including over 37 semiconductor-related transactions. Pagemill’s bankers have deep domain expertise and transaction experience in enterprise, infrastructure, and application software, semiconductors, internet and media, communications, storage, security and technology enabled services.

Scope of Analysis and Assumptions

Scope of Analysis:

• Private, VC-backed semiconductor companies, headquartered in North America, Europe or Israel
• The target companies included in the analysis were exited through an IPO or M&A transaction between January 1, 2002 and December 31, 2011
• Or, received financing between January 1, 2000 and December 31, 2011 and subsequently went out of business, unless such companies were documented to have gone out of business prior to January 1, 2002

Invested Capital Assumptions:

• Invested capital is based on disclosed investment amounts
• For companies where no funding data was available, total invested capital was assumed to be $30 million per company (total value of undisclosed investments assumed in this analysis is $1.2 billion)

Exit Value Assumptions:

• IPO exits were valued based on the stock price six months after the IPO date
Supply Chain Integration continued from page 15

Fabless Semiconductor Company:

- Initiate the request with the SCM and assembly and test provider and send out 3-way non-disclosure agreement (NDA).
- Analyze semiconductor company-specific requirements.
- Initiate kick-off meeting to go over requirements with the SCM and assembly and test provider and to give background to all parties involved. Reach agreement on timeline and deliverables.
- Monitor the SCM and assembly and test provider progress to initiate the B2B links.
- Send out sample purchase orders for UAT with test cases and ask for B2B reporting to be uploaded to file transfer protocol (FTP) site.
- Ask SCM provider to process sample information.
- Perform UAT, provide feedback and repeat with the SCM and assembly and test providers until satisfied.
- Ask SCM Provider to deploy to production.
- Continue to monitor the B2B integration in live operation.

Assembly and Test Provider:

- Receive request from the fabless semiconductor company and start the process to initiate the project, identify all stakeholders and obtain necessary approvals.
- Perform analysis to identify assembly and test provider sites and billable services being performed to select the standard WIP transactions that align with customer-specific bill trigger/pay points.
- Configure and test B2B reporting (unit test, integration test, connectivity) and promote to quality assurance (QA) environment.
- Deliver data to assembly and test provider’s FTP service via a secured customer account for pick and processing by the SCM provider.
- SCM provider to transform data into the SCM provider system and work with the customer to support UAT.
- Upon UAT approval, deploy to production.
- Perform post-deploy validation and customer satisfaction survey.

SCM Provider:

- Help define required data and training on the required system processes.
- Supply best-practices knowledge and templates to the process.
- Deploy the required software tools.
- Support accurate definition of the required information to the assembly and test provider’s team.
- Focus on data quality first and the supportability of the resulting integrations.
- Complete required data transformation from the assembly and test provider’s format to support the SCM system.
- Support the semiconductor company’s testing and UAT processes.
- Continue to monitor and support operational B2B integration.

About the Authors

Trisha Giacopazzi has over 25 years of experience in manufacturing. For the last 18 years, she has been with Amkor Technology, Inc., one of the world’s largest providers of contract semiconductor assembly and test services. Her current role is with Amkor’s IT Department, managing customer B2B projects and activities with a special emphasis on Amkor Standard Reporting of WIP, shipment and invoice information by way of RosettaNet, EDI, flat files or from Amkor’s Web data™ self-service customer Web portal. In her past roles at Amkor, she supported end-users, developing and deploying internal software training programs and beta testing applications.

Heather Salonga joined Amalfi Semiconductor, a fabless semiconductor company specializing in cost-effective, high-performance CMOS power amplifiers and transmit modules in 2010 as their cost accounting manager. She was integrally involved with the implementation of Tensoft FSM and Microsoft Dynamics, acting as their SCM project lead. Before joining Amalfi, Heather was a senior financial analyst at Intel for over four years. She holds both an MBA from the Booth School of Business at the University of Chicago, and an MS in computer science from the University of Chicago.

William White is a co-founder and CTO at Tensoft, an ERP and supply chain management (SCM) software provider to semiconductor companies. His business management system experience includes large-scale projects to support over a thousand end-users. In addition to supporting Tensoft customers, William oversees technical development at Tensoft. Prior to co-founding Tensoft, William was manager of software development at Lockheed Martin in Santa Clara, CA. He holds a BS in electrical engineering from Texas A&M University, and an Executive MBA from the Anderson School at UCLA.

Semiconductor Investment Returns continued from page 25

multiplied by the number of shares of common stock issued upon conversion of total convertible preferred stock outstanding

- M&A exits were valued based on the disclosed transaction value, adjusted for an assumed 10 percent management carve-out
- M&A exits with an undisclosed transaction value were assumed to have a gross exit value of $10 million and were adjusted for an assumed 10 percent management carve-out
- The analysis excludes any impact of earn-outs or transaction expenses
- Companies that filed for bankruptcy or went out of business were assumed to have garnered a $2.5 million liquidation value of the business assets; no management carve-out was assumed

Note: Return on invested capital is calculated on a cash-on-cash basis; no adjustments for time value of money are considered

Acknowledgements

2Gartner, Inc.
3VentureSource, Capital IQ, Thomson, Reuters, SEC filings, Wall Street reports, press releases and proprietary data
Q: In today's volatile business environment, it's difficult to efficiently manage a technology-driven supply chain. Describe Intersil's "Asset Lite" operations strategy and how it helps Intersil deliver exceptional service to customers.

A: Several decades ago, Jerry Sanders was famous for saying that real men have fabs. If you wanted to make semiconductors, you had to build your own wafer fabs. Then, around 15 years ago, we saw the emergence of the fabless industry, and that was the genesis of what was then the Fabless Semiconductor Association (FSA).

Many companies today are fabless and use foundries exclusively. At Intersil, we've taken a blended approach. We still have one wafer fab at Intersil where we manufacture specialty products that are difficult to fabricate in foundries. We use that captive fab for products such as radiation hardened ICs for satellites, military ICs and high voltage ICs. For the rest of our products, we run mostly proprietary processes, but at foundries. Ours is a balanced model where we can go either way; either fab, assemble and test internally, or do that with partners on the outside, and that gives us the flexibility to choose the best path.

Q: How has Intersil's strategy with suppliers and partners changed in light of 2011's natural disasters?

A: Well, it really changed the approach of our customers, as well as the way we are managing our own supply chain. The natural disasters, specifically the earthquake and tsunami in Japan, and the flooding in Thailand, were a wakeup call to the industry to have multiple suppliers. There is now much more sensitivity on the part of our customers, so we're making sure that we've got multiple manufacturing sources for all of our high volume products, at both the wafer fab and at the assembly and test level.

We're also discovering that it's not just adding multiple sources, but making sure we have geographically dislocated sources. For instance, if we had two sources but both were located in Thailand, a flood might take out both of those sources. Now it's becoming important for us and our customers, that if we do have multiple sources, they're located in different parts of the world, so that one natural disaster can't take out both sources.

Q: KPMG recently released the results of its 2012 Global Tech Innovation Survey. The results showed that 43 percent of respondents stated it was likely the technology innovation center of the world would move from Silicon Valley to another country in the next four years, naming China as the most likely next innovation center, followed by India, Japan and Korea as other options. What are your thoughts on this projected shift, and how is Intersil preparing for this potential change?

A: There's no doubt that more and more product development is going to occur in locations outside the United States. We have design centers in China and in India, and I think that there is going to be an increasing amount of product development going on there. On the other hand, I certainly would not count out Silicon Valley. People have done that for decades. Silicon Valley is amazingly resilient, and it's gone through many different phases. If you went back to the beginnings of the semiconductor industry, Silicon Valley has been involved in the development of computers and disk drives, and then networking, and more recently, social networking.

Silicon Valley keeps reinventing itself. I think the real strength of Silicon Valley is the critical mass of truly innovative people and the unique collaboration you see here. For many years to come, Silicon Valley is still going to be the world's headquarters for innovation, where the real visionary products get defined and the new technologies get invented. However, getting those inventions translated into products is a process that will increasingly happen in other parts of the world.

Q: Confronted by rising costs, constrained resources and a challenging technology roadmap, the semiconductor industry faces difficult technology and investment choices. What must semiconductor companies do to stay competitive?

A: One of the biggest challenges we face is that the semiconductor industry is becoming a mature industry. Unfortunately, it's likely to be a zero growth industry in the coming years. Right now, the worldwide semiconductor business is around $300 billion, and it's been there for a few years. Given the worldwide economic challenges that we face, the business is likely to stay at about that level for the coming years.

The real challenge is how do you grow in a zero growth environment? It's a little bit like the mythical Lake Wobegon, where everyone is above average. Every company says they plan to grow, but in a zero growth environment, that's just not going to happen. So how do you distinguish yourself and make sure that you are one of the companies that is going to grow in that environment? The solution is innovation and differentiation – you need to be visionary enough to see where the market is heading, what the customer is going to be requiring down the road, and come out with truly unique and differentiated products. If your company is coming out with "me-too" products, it just becomes a price war, and clearly that's not the way to grow revenues or profits.

Q: To sustain Moore's Law, the industry's brightest minds have explored the boundaries of technology and innovation to boost computing power at 22nm and beyond. The standout solutions include 2.5D and 3D packaged ICs, SOI technology and 2D planar/3D FinFET transistors. How do you feel these multiple technologies will further business growth and a competitive edge in the near future?

A: Both 2.5D and 3D packaged ICs are required for our industry to deliver a sustained performance trajectory. We all know about Moore's law and how feature sizes have shrunk year after year for decades. Sustaining Moore's law may be possible from a purely technical perspective, but it may not be practical from a cost perspective. The costs to build a state-of-the-art fab are just becoming too large for all but the very largest companies. Building a 22nm fab is probably a $5 billion investment — who knows what it's going to be at 14nm.

That's why I think it's essential to start moving to 3D ICs and more parallel architectures – this is what many are calling "more than Moore." Rather than simply building faster processes, you're going to see more parallel processing. And likewise, I see stacking ICs together to get increased performance and density. So I absolutely believe that going to some of these new technologies, especially in the assembly industry, is going to be essential to continue the growth of semiconductors.

Q: Recruiting and retaining talent has long been a difficult task for semiconductor companies. How does Intersil attract and retain the talent necessary to sustain technology and drive innovation?

A: I'm a firm believer that people are the essential ingredient for success. If you want to be an innovation driven company, you have to attract the best and brightest in the industry. I think there are a couple of ways to do that. One of them is the culture of the company — you have to create a culture that values and rewards innovation. Along with that, you need a culture that allows people to be innovative, that empowers them to do creative things, and that manages risk in the right way.
Whenever people are pushing the limits, there are going to be failures. I believe that the way a company deals with failure, is really, really important. If you’re completely intolerant of failure, guess what? Nobody’s going to take any risks! A lot of this comes under the umbrella of corporate culture.

If you start attracting and building critical mass with really outstanding people, they themselves will attract more outstanding people. If people in our industry recognize the caliber of the people we’re hiring, and the way we’re empowering them to innovate, they’re going to be motivated to join our team. Outstanding people attract other outstanding people.

Increasing amounts of redesign work are needed to achieve Moore’s Law scaling of a product design into the next technology generation to accommodate the altered design rules, and this migration of the design costs both money and time. This increase in the amount of money at risk when migrating a design is a strong motivator to embrace technology extensions for products that don’t require a large increase in feature density and/or don’t have huge volumes.

The 28nm process technology is a unique generation in the semiconductor roadmap because it is at the inflection point for the effective use of conventional 193nm wavelength lithography and the conventional planar, bulk transistor. Furthermore, the migration cost beyond 28nm process technology will be even greater than for previous migrations because patterning costs will increase dramatically, first through the use of double-patterning with 193nm immersion lithography tools and later through the transition of EUV lithography tools. Some of the transistor architecture changes that the industry is considering beyond the 28nm process technology may require excessive manufacturing costs as well, and possibly new design methodologies for creating circuit IP.

As a result of these two factors, 28nm process technology will most likely be a long-lived process technology.

Conclusion

The semiconductor industry needs a process technology roadmap that allows companies to increase their product value despite the excessive cost of 20nm and smaller process technologies. A depleted-channel transistor architecture is critical to controlling power consumption and making highly-integrated, low-power SoCs possible at 20nm and smaller geometries. Furthermore, enhancing process technologies from 90nm to 28nm with a depleted-channel transistor architecture that reduces power consumption is an excellent economic alternative to shrinking a product to the next process technology until the cost of migrating to leading-edge process technology is beyond the steep portion of the cost-learning curve.

About the Author

Nick Kepler is vice president of products for SuVolta. Prior to joining SuVolta, Kepler spent 22 years in a variety of management and technical roles at Advanced Micro Devices, concluding with vice president, advanced CMOS process technology development followed by three years in executive-level positions at GLOBALFOUNDRIES.
Internal communication within the company was enhanced by training sessions and weekly steering committee meetings, as well as daily project team meetings. Twice a week, a meeting within the supply chain management was arranged, in addition to weekly updates in worldwide sales calls. Furthermore, monthly presentations were held at the Executive Committee Board. In order to ensure transparency between the company and its former mother company and to discuss progress and critical topics, meetings with high management were held weekly, and regular updates took place with representatives from both companies. For documentation and quality management, an internal data organization was established. In addition, weekly project reports in terms of cockpit charts were created.

**Conclusion**

After the time target of one year, the production transition process was finished and thus all products were phased out from the mother company and are being produced by new suppliers. While the production was moved to other suppliers, as few changes as possible were made to the products themselves.

Transferring such a great number of products from one manufacturer to new suppliers within a short time period required excellent logistics and a team dedicated 100 percent to the project. A total of 233 products were transferred on time and within budget, making the company fully fabless. A total of 95 package projects, 30 wafer test packages and 134 final test packages were transferred. In order to prove the functionality system, verification was conducted by testing 85 system applications. Through the application-oriented PCN approach, 8,500 product-customer combinations were made to the products themselves.

Very fast transfer of Flood Bangkok and Fukushima affected products

Managed impact of Fukushima and Bangkok catastrophes

Smooth phase out of end of life products

Dual source strategy for critical products

Standardized packages and Au–Cu conversion

System test reports included in PCNs for customer confidence

8,500 product/customer combinations in 28 PCNs

Project and manufacturing cost controlling

All cost savings implemented product fine in planning tool

Track and control project expenses and savings

Figure 3: Project Summary and Achievements

**Projects**

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**Acknowledgment**

The author would like to thank Dominik Bilo for sponsoring this major production transition project and to Benno Fritzler for excellent cooperation and his continuous support with the phasing-out process. The author would also like to show his appreciation to Juliane Kurmann for her significant contributions to the documentation of the project as well as her great assistance with the manuscript.

**References**


About the Author

Ferdinand H. Bell brings more than 20 years of experience in the semiconductor industry to his current position as director at Lantiq. He leads a department responsible for new product introduction, product-portfolio and cost management. Prior to joining Lantiq, Ferdinand spent 20 years at Siemens and Infineon Technologies. His responsibilities included process development and advanced process control in wafer fabs, yield management and methodologies in frontend and backend fabs and backend technology development. Ferdinand holds a master degree in physics from the Technical University of Munich and a Ph.D in material science from the University of Nantes. Ferdinand H. Bell can be reached at fernand.bell@lantiq.com.

**Figure 3: Project Summary and Achievements**

- **Overall Project**: Make a fully fabless company
  - 233 products transferred on time and within budget
  - Very fast transfer of Flood Bangkok and Fukushima affected products
- **Project Office**: Control and track project progress
  - Track and control of > 6,000 project milestones
  - Managed impact of Fukushima and Bangkok catastrophes
- **Sales & Marketing**: Alleviate customer’s fear of supply risk and quality concerns
  - Customers still trust in company despite many tedious changes
  - Smooth phase out of end of life products
- **Purchase**: Establish a “best-in-class” sourcing strategy
  - New fabless optimized sourcing strategy
  - Dual source strategy for critical products
- **Assembly**: Package portfolio: establish international standard packages
  - 85 package projects transferred with significant cost savings
  - Standardized packages and Au–Cu conversion
- **Test**: Tester platforms: establish international standard
  - 30 wafer test packages transferred with significant cost savings
  - 134 final test packages transferred with significant cost savings
- **System Verification**: Prove functionality in system application
  - System verification done for 85 products/ product families
  - System test reports included in PCNs for customer confidence
- **Quality**: New strategy: application orientated PCN approach
  - Qualification of 30 reference packages
  - 8,500 product/customer combinations in 28 PCNs
- **PCN Management**: Close alignment between project, sales and customers
  - PCN approvals in time
  - New efficient and effective PCN process introduced
- **Logistics**: Basic data and logistics flow set up, provide customers samples
  - 290,000 PCN samples provided
  - 3,800 operations executed
- **Supplier Cooperation**: Smart phase over from mother company to new suppliers
  - Trustful partnership with mother company established
  - New suppliers enabled with excellent partnership
- **Finance**: Project and manufacturing cost controlling
  - All cost savings implemented product fine in planning tool
  - Track and control project expenses and savings