READINESS OF 2.5D/3D IC PACKAGE DESIGN ENVIRONMENT
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BACKGROUND

- Founded: 2007
- Location: San Jose, California
- BroadPak is a 2.5D/3D integrator
- Provider of total solution and technologies to develop and launch 2.5D/3D products
- Services: Low cost, high performance package co-design, signal/power Integrity, robust packaging solution
- Customers: Major semiconductor players
On a daily basis we deal with:

- Various companies
- Various IC design teams
- Various IC Fabs, various process nodes
- Various package substrate manufacturers
- Various package assembly vendors
- Various PCB vendors
Much “More than More” Direction

If you can’t shrink it, stack it.
Farhang Yazdani

Multiple

- Physics
- Technologies
- Materials
- Interfaces
- Disciplines
- ...

Sensors
RF/Analog
Memory
Processor
WHAT DO WE HEAR ABOUT 2.5D/3D?

**Benefits**
- Improves overall die yield
- Lowers the power
- Allows mixed node
- Allows IP reuse
- Smaller footprint

**Challenges**
- Expensive
- Integration & Design
- Limited in size
- Reliability
- KGD, Yield
- Test
- Supply Chain
What are the main barriers to 2.5D/3D adoption?

• Cost
• Reliability
What does it take to co-design and co-simulate this structure?
3 FALVORS OF 3D IC CONSTRUCTION

- Via First
- Via Middle
- Via Last
<table>
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<th></th>
<th>Compared to circuit elements (Inverter, SRAM cell, etc.):</th>
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<tr>
<td>1.</td>
<td>TSVs are huge</td>
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<tr>
<td>2.</td>
<td>TSV count is crucial</td>
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<tr>
<td>3.</td>
<td>TSV placement and location is crucial</td>
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<td>4.</td>
<td>TSVs cause coupling</td>
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<td>5.</td>
<td>TSVs require design-for-manufacturability/reliability</td>
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<tr>
<td>6.</td>
<td>TSVs require design-for-testing</td>
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**TSV Placement and Impact on Reliability**

- **Uniform TSV Pattern**
- **Non-uniform TSV Pattern**
MANUFACTURING CHALLENGES

Warpage

Wafer warpage
1. Thinning
2. TSV reveal

Impacts yield during processing and production

Interposer die level warpage

Impacts yield during packaging and assembly

Wafer level simulation doesn’t cut it
Effect of assembly must be included at the wafer level
2.5D/3D Pathfinding & Design Optimization
WHAT IS OUR GOAL?

- Higher Performance
- Lower Cost
- Higher Reliability
- Smaller Foot-Print
Your package ball-out is fixed (i.e. defined by your customer)

Your IC design team has frozen the Die bump/pad pattern

Then you will end up with a very expensive package substrate

Meaning: Your package could cost more than the die it contain
Typical 2D Connectivity

- First Order Effect
  - Performance
  - Cost
  - Time to Market

- Collaboration
  - Two Different Industries
  - Two Different Teams

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- First Order Effect
  - Performance
  - Cost
  - Time to Market

- Collaboration
  - Semi-Similar Industries
  - Two Different Teams
2.5D/3D: Total System Connectivity

Pathfinding: Total End-to-End System Connectivity and Exploration

IC Design Tools → Package Design Tools → PCB Design Tools

Single Database to Address Ultra-Dense Connectivity Across the System
COMMON 2D SILICON-PACKAGE DESIGN FLOW

IC Design
- Device Spec
- Design rules

IC Package Design
- Cross section definition
- Device placement
- Wirebonding or Fanout
- Routing and editing
- Netlist/DRC verification
- Documentation

Manufacturing & Assembly

Analysis
- Thermal
- 3D Modeling and Parasitic extraction
- Via and plane modeling
- Signal/Power Integrity analysis

Performance information

In 2D designs, some Packages cost more than the die
High Level 2.5D/3D Flow

- Design Constraint
- Intellignet Pathfinding
- 2.5D/3D Package Integration
- System Integration Optimization
- Thermal, SI/PI, Stress, Warpage, EMI, Cost, ...
- System requirement
- Logic Partitioning
- Data Structure
- Device Input

2.5D/3D Device

Product Definition

BroadPak 2.5D/3D Technologies
WHAT IS PATHFINDING?

Pathfinding is a methodology for optimal integration of components and systems.

Aren’t we doing this right now?

Pathfinding is emerging as an area of expertise due to ultra-dense connectivity. Partitioning and Pathfinding are coupled.

Pathfinding will directly impact the success of a product. It could be a deal breaker.
Fixed Netlist Drives the Connectivity

EXAMPLE, BGA PATTERN

Before

After
EXAMPLE: I/O CELL TO BUMP OPTIMIZATION

New EDA Tool Announcement

June 9, 2014
Mentor Graphics Launches Xpedition Path Finder Suite for Efficient IC/Package/PCB Design Optimization, Assembly, and Visualization

WILSONVILLE, Ore., June 9, 2014 - Mentor Graphics Corporation (NASDAQ: MENT) today announced its Xpedition™ Path Finder product suite, providing designers with the ability to assemble and optimize complex electronic systems, and thereby enabling improved design, increased chip performance, and cost efficiency. This product, the newest addition to the Mentor Graphics® Xpedition platform, supports a methodology that leverages layout data from the IC and board design teams to guide and automate IC package selection and optimization.

The Xpedition Path Finder suite provides a single environment that gives cross-domain design teams the ability to model every device/interface to the level of detail and accuracy they require. IC layout design data can be represented as a virtual die model (VDM), containing all of the IC-level detail specific to the co-design and optimization process.

SOURCE:
Summary
STATUS OF 2.5D/3D READINESS

- Design: Logical & Physical Co-design
- Analysis: Multi-physics Co-simulation
- Test: Co-design for test
- Reliability: Co-Design for Yield and reliability
- Cost: Co-design for cost (cost aware design)
- Verification (LVS)
What’s next?
TAKE THE PLANK WALK (MOUNT HUASHAN, CHINA)

TAKE THE PLANK WALK (MOUNT HUA SHAN, CHINA)

It’s a centuries-long tradition, still followed by many Chinese today, to climb Mount Hua at night. Many report it’s actually easier to tackle in the dark since you can’t look down and get scared. Image by Aaron D. Feen/Flickr

http://www.attractioneers.com/uncategorized/hill-walking-in-china/