Advanced 2.5D and 3D IC Systems Enabled by Mechanically Flexible Interconnects and Advanced Embedded Cooling Concepts

Muhannad Bakir
Muhannad.bakir@mirc.gatech.edu

School of Electrical and Computer Engineering
Georgia Institute of Technology

Jan 20 2016
Off-Chip Bandwidth Trend

[Graph showing trend of off-chip I/O bandwidth over years with markers for different companies such as IBM P7 and Oracle T3]
Off-chip Bandwidth and I/O Power

Power Breakdown for Intel Ivytown (22 nm)

Off-chip Interconnects

- Highly bandwidth limited due to coarse pitch at the motherboard level
- Interconnects can be 'messy'
- Still relatively coarse pitch
- Fine pitch interconnects possible
- Channel becomes extremely lossy for longer lengths
- Longer length interconnects possible with low loss
- Typically limited by pitch (~60 um)

Electronic

Optical
• Enabling Technologies for Next Generation 2.5-D/3-D Systems
  – Scalable Interposer Platform
  – Low-Loss TSV technology
  – Monolithic-scale TSV technology
• Embedded Microfluidic Cooling For Densely Integrated Altera Stratix V FPGAs
  – FPGA-CPU Integration
  – Thermal (and Power delivery) Challenges and Solutions
2.5D Systems

Challenges:

1. ‘Small’ area and warpage (More Functions)
2. Lossy Signaling
3. Fabrication processes are not ‘low cost’

Wish List:

1. Large area and scalable interposers; warpage free
2. Low-Loss platform for interconnects and RF components
3. Low-cost batch fabrication process
   • High aspect ratio Bosch-free TSVs
4. Advanced cooling integration
Interposer Based System

- Traditional 2.5D interposer based system Vs. MFIs and PSAS enabled platform
Interposer Tiles and Bridges

An inverted pyramid pit

- Diameter of PSAS = 300 μm
- Width of Pit = 300 μm

H. S. Yang et al., IEEE TCPMT 2014
An inverted pyramid pit

- Diameter of PSAS = 300 μm
- Width of Pit = 300 μm

Fine pitch MFIs

H. S. Yang et al., IEEE TCPMT 2014
Interposer Tiles and Bridges

An inverted pyramid pit

PSAS

Memory Stack

MFIs between interposer tile and bridge
- Diameter of PSAS = 300 μm
- Width of Pit = 300 μm

MFIs between interposer tile and motherboard

Fine pitch MFIs

H. S. Yang et al., IEEE TCPMT 2014
Interposer Tiles and Bridges

An inverted pyramid pit

PSAS

Diameter of PSAS = 300 μm
Width of Pit = 300 μm

MFIs between interposer tile and bridge

Fine pitch MFIs

Optical wave guides

Highly flexible MFIs

Motherboard
Mechanically Flexible Interconnects

- Thickness of Au-NiW MFIs = 9.1 μm
- Resistance of Au-NiW MFIs = 118 mΩ

C. Zhang et al., IEEE TCPMT 2013
Mechanical Characterization

- Indentation test results show the Au-NiW MFIs have up to 65 μm vertical range of motion
Outline

• Enabling Technologies for Next Generation 2.5-D/3-D Systems
  – Scalable Interposer Platform
  – Low-Loss TSV technology
  – Monolithic-scale TSV technology
• Embedded Microfluidic Cooling For Densely Integrated Altera Stratix V FPGAs
  – FPGA-CPU Integration
  – Thermal (and Power delivery) Challenges and Solutions
• 3D IC Technology for Bioelectronics
Low-Loss Silicon Interposer Platform

- Silicon interposer platform with low-loss TSVs using air.

- Conventional TSVs in silicon

- Low-loss TSVs using air

- Result in reduced capacitance and coupling between TSVs.

Low-Loss Through-Silicon Vias Using Air: Fabrication

1. Deposit and etch silicon dioxide.

2. Etch silicon using oxide mask.

3. Perform wet oxidation for oxide liner.

4. Deposit seed layer and do electroplating.

5. Pattern metal pads and etch silicon.

6. Perform high-frequency measurements.

- Conventional TSVs
- Low-loss TSVs

**Y. Zhang, H. Oh, 3DIC 2013**

Low-Loss Through-Silicon Vias Using Air: Fabrication

TSV dimension: 13 µm in diameter, 300 µm in height (AR = ~23:1), 100 / 200 µm in pitch
Silicon pillars: 50 µm in diameter (circular pillars)
50 µm in width and 200 µm in length (rectangular pillars)

*HAR TSV technology demonstrated at 3DIC 2013.

Low-Loss Through-Silicon Vias Using Air: TSV Loss Measurements

• To extract the loss of a single TSV from de-embedding structures.

Two-port measurements with L-2L de-embedding technique.

SEM images: TSVs with metal pads

Insertion Loss [dB]

- Air-isolated TSVs
- Conventional TSVs

46.7% Reduction

Low-Loss Through-Silicon Vias Using Air: TSV Capacitance Extraction

- To extract TSV capacitance and conductance using single-port measurements

1. Convert s-parameters to z-parameters.

\[
Z_{11} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}} \quad (*)
\]

2. Take real and imaginary parts of it.

\[
C_{TSV} = \frac{1}{\text{Im}(Z_{11}) \cdot \omega} \quad (**)
\]
\[
G_{TSV} = \frac{1}{\text{Re}(Z_{11})}
\]

Polymer-embedded Vias

65 µm Diameter and 370 µm Tall Polymer-Embedded Vias on 150 µm Pitch

Coaxial Vias: Impedance Extraction

Fabrication Process

1. SiO$_2$ and Ti-Cu Seed Layer Deposition, Si Etch, Ti Etch, and SU-8 Coating and Baking

2. SU-8 Photodefinition to Obtain Vias

3. Cu Electroplating and CMP

4. Fabrication of Metallization and CMP for Open Structure

Fabricated 65 µm diameter and 285 µm tall copper vias

Extracted Impedance from RF Measurements

Simulations give 0.1 dB insertion loss at 50 GHz for the 150 µm pitch structure.
W-band Antenna Fabrication and Measurement

Fabricated Antenna

1100 μm x 650 μm and 2 μm thick patch antennas over 1530 μm x 1030 μm and 280 μm deep wells.

Return Loss Measurement

- 13.35 GHz 10-dB return loss bandwidth
- 4.4 dBi gain and 70% radiation efficiency at 100 GHz

Simulation at 100 GHz

P. A. Thadesar, and M. S. Bakir, IEEE TCPMT 2015/2016 accepted
Inductors:
Measurements for Inductor Over SU-8 Well

Extracted L and Q of the Inductor Over SU-8 Well:
\[ Q_{\text{peak}} = 55 \text{ at } 6.75 \text{ GHz with } 1.14 \text{ nH inductance and an SRF at } 21 \text{ GHz.} \]

Fabrication Results

Inductors over thick SU-8 layer

Inductor over polymer well
Outline

• Enabling Technologies for Next Generation 2.5-D/3-D Systems
  – Scalable Interposer Platform
  – Low-Loss TSV technology
  – Sub-micron TSV technology

• Embedded Microfluidic Cooling For Densely Integrated Altera Stratix V FPGAs
  – FPGA-CPU Integration
  – Thermal (and Power delivery) Challenges and Solutions

• 3D IC Technology for Bioelectronics
Motivation for TSV Scaling

![Graph showing the number of TSVs available vs. via height (microns)]

- **HAR TSVs enable 10x denser integration**
- **Monolithic-scale TSVs enable up to 1000x denser integration**

**Through Silicon Via Scaling**

- **AR=26:1**
  - Tohoku University
  - M. Koyanagi et al., Proc. IEEE, 2009
- **AR=5:1**
  - Tezzaron
- **AR=10:1**
  - IMEC
  - Redolfi A. et al., ECTC 2011.
  - Xilinx
  - Banijamali B. et al., ECTC 2011
- **AR=8:1**
  - Oracle
  - Shubin I. et al., ECTC 2013
- **AR=17:1**
  - GLOBALFOUNDRIES
  - Zhang D. et al., TSMC 2015.
  - TSMC
  - Chang H.B. et al., VLSI 2012.
- **AR=23:1**
  - Georgia Tech
  - Zhang Y. et al., 3DIC 2013.
  - Abbaspour R. et al., Device.
Sub-micron Via: Fabrication

The wafer is backside-etched and the void-free 920nm vias are showing up from the buried end.

Cross-sectional view of a cleaved sample, shows void-free copper filled 480nm diameter via with 17:1 aspect ratio.

Side-view: Cleaved sample right after deep Si etching using developed nano-Bosch process.
Resistance Measurement

\[ R_{\text{Measured}} = R_{\text{parallel}} \]
Current Carrying Capacity & Capacitance

- **Current Carrying Capacity**
  - Graph showing the relationship between Resistance (Ω) and Current [μA]
  - Data points and fitted curve

- **Capacitance Change vs. SiO2 thickness**
  - Graph showing the change in Capacitance [nF] with varying SiO2 thickness [nm]
Outline

• Enabling Technologies for Next Generation 2.5-D/3-D Systems
  – Scalable Interposer Platform
  – Low-Loss TSV technology
  – Sub-micron TSV technology

• Embedded Microfluidic Cooling For Densely Integrated Altera Stratix V FPGAs
  – FPGA-CPU Integration
  – Thermal (and Power delivery) Challenges and Solutions
Power Integrity and Thermal Challenges for 3-D/2.5-D IC stacks

- 3-D/2.5-D stacking of multiple high performance chips
  - Higher power density
    - heat removal
    - power delivery (multiple power hungry chips)

Source: Intel, Altera, Microsoft

Next generation system: high performance processor with deep learning FPGA accelerator
Power Integrity and Thermal Challenges for 3-D/2.5-D IC stacks

- 3-D/2.5-D stacking of multiple high performance chips
  - Higher power density
    - heat removal
    - power delivery (multiple power hungry chips)
  - Heterogeneous stack of multi-functional chips
    - Thermal crosstalk: high power processor heats up the other dice
    - Multiple power domains: I/O pins, analog, digital; critical block, low power block)

Source: Intel, Altera, Microsoft

Next generation system: high performance processor with deep learning FPGA accelerator
Modeling Overview --- Power Delivery Network

- Power supply noise consists of
  - IR drop
    - On-chip, package, board resistive loss
  - $L \cdot \Delta I / \Delta t$ noise
    - Inductive elements: board wire, BGA, package wire, microbump, TSVs
    - Frequencies from MHz (package/board) to GHz (on-chip)

- Comparison to literature

<table>
<thead>
<tr>
<th>Institution</th>
<th>IR drop</th>
<th>Transient noise</th>
<th>Distributed on-chip PDN or lumped</th>
<th>Detailed Board/packaging model</th>
<th>VRM incorporated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gatech, J. Xie</td>
<td>Yes</td>
<td>No</td>
<td>Distributed</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>UVA, R. Zhang</td>
<td>Yes</td>
<td>Yes</td>
<td>Distributed</td>
<td>Partially(^1)</td>
<td>No</td>
</tr>
<tr>
<td>Harvard, X. Zhang</td>
<td>Yes</td>
<td>Yes</td>
<td>lumped</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>RPI, H. He</td>
<td>Yes</td>
<td>No</td>
<td>Distributed</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>OSU, Y. Shao</td>
<td>Yes</td>
<td>Yes</td>
<td>Distributed</td>
<td>Partially(^1)</td>
<td>No</td>
</tr>
<tr>
<td>Gatech, G. Huang</td>
<td>Yes</td>
<td>Yes</td>
<td>Partially(^2)</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>This work</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Distributed</td>
<td>Yes</td>
<td><strong>Yes, it can be incorporated</strong></td>
</tr>
</tbody>
</table>

1. Lumped wire model and distributed C4 model
2. Uniform power density assumption
Distributed Circuit Model for Power Delivery Network

- Finite difference method
  - Finite volume scheme for IR drop (resistance network)
  - Trapezoid scheme for transient noise analysis

Conventional PDN as an example
Numerical Modeling for On-Die PDN: Full Chip Simulation

- Two-die stack simulation.
- Noise suppression
  - Adding decoupling capacitors
  - Adding P/G pads/TSVs

PSN of the top die (Max PSN 242.8 mV)

Double decap in IV: 10.2% noise reduction, Max PSN 218.1 mV

Double pad/TSV in IV: 13.8% noise reduction, Max PSN 209.4 mV

Double decap in I - IV: 17.2% noise reduction, Max PSN 201.0 mV

Double pad/TSV in I - IV: 24.6% noise reduction, Max PSN 183.1 mV
Microelectronic Cooling

- Power limit $\sim 100\text{W/cm}^2$
- Large Footprint
- Incompatible with high power 3DIC
Microelectronic Cooling

- Liquid cooled cold plates used in some datacenters, supercomputers, and enthusiast PCs.
- IBM Aquasar server cooling
  - PowerxCell 8i Processor (TDP 92W)
  - $R_{th} \approx 0.16$ °C/W
- Used in SuperMUC supercomputer (#20 in TOP500)
  - Xeon E5-2680 (TDP 130W) and Xeon E5-2697 v3 (TDP 145W) processors

More Commercial Liquid Cooling Examples

Asetek Liquid Cooled Cray Blade
Asetek.com

CoolerMaster Liquid Cooling System
Coolermaster.com

AMD Radeon Fury X HBM
http://techreport.com/review/28513/amd-radeon-r9-fury-x-graphics-card-reviewed/2
Our Approach: Monolithic Microfluidic Heat Sink in IC

Assembled Microfluidic-cooled FPGA

Etched FPGA Backside

Micropin-fin Dimensions

T. Sarvey et al IEEE CICC 2015
Demo with Pulse Compression Core

- A functional design for Stratix V DSP kit
  - Multiple independent Pulse Compression test units. The number of active cores to be enabled is run time configurable

- Design optimized for streaming data and low latency
Microfluidic Cooled FPGA Performance

Baseline Design

1.5x of Baseline Compute Capability

<table>
<thead>
<tr>
<th>Power</th>
<th>Flow Rate</th>
<th>Die Temp</th>
</tr>
</thead>
<tbody>
<tr>
<td>29W</td>
<td>147mL/min</td>
<td>24°C</td>
</tr>
</tbody>
</table>

Junction-to-ambient $R_{th} \approx 0.08^\circ$C/W
Thermal Isolation for Heterogeneous 3D IC

- Processor on memory: thermal coupling

High power (CPU)
Top: 75w

Low power (Memory)
Bottom: 2.8w

Proposed stack
1. Microfluidic cooling
2. Air gap isolation
3. Thermal bridge for isolated die

Prototype of proposed stack

Bottom die power maps for isolation demonstration

Conclusion

• Plenty of open questions and new concepts for next steps in research

• We look forward to collaboration with colleagues in our community on current and forward looking research
Off Topic: Questions from GT Team for an NSF Program We are Part of

- **Q1** What are the major challenges in packaging, interconnections and/or testing of next generation electronic systems?

- **Q2** What are the projections for pad or I/O pitch scaling and what are the foreseeable challenges pertaining to it?

- **Q3** What are the challenges in replacing or upgrading a chip in electronic devices? Or thoughts about modular electronics?