Wafer Level Packaging

John Hunt
ASE Group
October 21, 2015
Technology & Market Evolution

1970s
Aerospace
Thousands of Units

1980s
Mainframe
Millions of Units

1990s
PC (PM)
350M+ Units
Cell Phone (PP)
1.8B+ Units

2000s
Smart Computing (PMP)
10B+ Units

2010s
Internet of Things (IOT)
(PMMP)
100B+ Units
Exponential Connectivity & Big Data

2020s
We are here

Newer & Bigger Markets

© 2014 ASE Group. All rights reserved.
Drivers for Advanced Packaging

- **Drivers**
  - Small, Thin for mobile applications
  - Low cost for Consumer Products
  - Good Electrical performance
  - Low power

- **Solutions**
  - Wafer Level Chip Scale Package
  - Fanout Chip First Package
  - Fanout Chip Last Package
iPhone Trends: Increasing Number of WLPs

iPhone Evolution

<table>
<thead>
<tr>
<th>iPhone Model/year</th>
<th>WLPs</th>
<th>Thickness (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>iPhone 1 2007</td>
<td>2 WLPs</td>
<td>6</td>
</tr>
<tr>
<td>iPhone 3GS 2009</td>
<td>4 WLPs</td>
<td>7</td>
</tr>
<tr>
<td>iPhone 4S 2011</td>
<td>7 WLPs</td>
<td>8</td>
</tr>
<tr>
<td>iPhone 5 2013</td>
<td>11+ WLPs</td>
<td>10+</td>
</tr>
<tr>
<td>iPhone 5S 2013</td>
<td>22 WLPs</td>
<td>13</td>
</tr>
<tr>
<td>iPhone 6 2014</td>
<td>26+ WLPs</td>
<td>15+</td>
</tr>
<tr>
<td>iPhone 6 Plus 2014</td>
<td>26+ WLPs</td>
<td>16+</td>
</tr>
</tbody>
</table>

Source: TechSearch International, Inc., adapted from TPSS.

Shown to scale
Denser & Thinner

- Apple Watch SiP demonstrates the evolution in miniaturization

Source: TechSearch, TPSS Level 2.5E July 2015
What do we mean by Wafer Level Package (WLP)?

- All IC packaging is done in wafer form
  - No handling of discrete devices during packaging assembly

- A Wafer Level Chip Scale Package (WLCSP) is a subset of WLP
  - It is a “Chip Scale (<= 1.4 X area of die)” package
    - The package is only the die - therefore it is “die size”
  - Compatible with Standard SMT Assembly Processing
    - Placed with existing SMT tools, no flipchip bonder required
  - Current Ball pitch 0.3mm – 0.5mm
  - No underfill is required, but can be used for added reliability
Wafer Level Chip Scale Package
WLCSP
The Beginning......

It started with . . . . Then . . . . And . . . .
Evolution........

1st Point Contact Transistor 1948

1st Junction Transistor 1951

WLCSP 2001

Volume
6,000,000 : 1

WLCSP 2015

Approximately to scale
WLCSP Evolution

Die Size

5x5-7x7mm
Combo/Connectivity, MCU
Wider adoption outside portable products, expect up to 8x9mm die size
Fan out and enhanced versions in HVM

5x5-6x6mm
Transceiver, Power Manager, Image Sensor, Audio Codec
Wide adoption in smartphones

4x4mm
Bluetooth, WLAN, TV Chip, Transceiver

4x4mm
Additional Device Types: Analog, IPD, MOSFET
Nokia phones with 7-8 WLCSP

1x1-2x3mm
EEPROM, MCU, Security Chips, Watches

Prismark

© 2014 ASE Group. All rights reserved.
ASE Has Multiple WLCSP Solutions

Sputtered UBM on Nitride

Sputtered Repassivation

Plated Repassivation

3-Layer Plated Redistribution

Cu UBM on Pad For Embedding

Cu UBM on RDL For Embedding

Plated Repassivation on top of UBM

4-Layer Sputtered Redistribution

4-Layer Plated Redistribution

Cu Thick RDL For Embedding

2-Layer Plated Redistribution

6-Layer Plated with 2 Redistribution Layers

Cu UBM on RDL For Embedding

But, there are more than One Hundred variations of these basic structures in production!
ASE’s Wafer Level Package Solutions

- Bumping
- ASE Wafer Level Packaging
- 3D WLP
- WLCSP
- WL IPD
- WL MEMS
ASE WLCSP Initiatives

- Larger WLCSP Packages
  - Increased Die Package size

- Improved Performance
  - Reliability - Reinforcement structures
  - Reliability - Solder Alloys
  - Current Handling Capacity

- Low Cost Structures
  - 3-Layer & 2-Layer

- Thin Package

- Improved Die Edge Quality

- MEMS/3D

- Low Cure Polymer
Reliability Factors

- Factors that improve WLP die performance
  - Solderball Pitch/Array pattern
  - Solderball Alloy
  - Die Thickness
  - Polymer/Polymer Thickness
  - RDL Material/Thickness
  - Reinforcement
ASE Large Die Development with Nokia – Phase I

- Large Die Board Level Reliability Co-Development (ASE 8x8mm – 63.2% Corner Ball)
  - Thick PI “○” and Thin Die “◇” can enhance both TC and Drop
  - Thick RDL “◇” can enhance the drop only

![Diagram showing TCOB and Drop comparison](image-url)
### Large Die Development with Microsoft - Phase II

- Phase II co-development with ASE & Microsoft

<table>
<thead>
<tr>
<th>Variable</th>
<th>Polymer 1</th>
<th>P1 Thickness</th>
<th>Cu RDL</th>
<th>Polymer 2</th>
<th>P2 Thickness</th>
<th>Cu UBM</th>
<th>Solder</th>
<th>Die Thickness</th>
<th>BSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Standard</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>Std</td>
<td>Std</td>
<td>Yes</td>
</tr>
<tr>
<td>2 Thick Dielectric &amp; Thin Die</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>Std</td>
<td>Thk</td>
<td>Yes</td>
</tr>
<tr>
<td>3 M758 Solder</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>Alloy A</td>
<td>Std</td>
<td>Yes</td>
</tr>
<tr>
<td>4 Superset</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>Alloy A</td>
<td>Thin</td>
<td>Yes</td>
</tr>
<tr>
<td>5 Optional</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>PI</td>
<td>Thk</td>
<td>Std</td>
<td>Alloy A</td>
<td>Std</td>
<td>Yes</td>
</tr>
<tr>
<td>6 PBO Effect</td>
<td>PBO</td>
<td>Std</td>
<td>Std</td>
<td>PBO</td>
<td>Std</td>
<td>Std</td>
<td>Alloy B</td>
<td>Std</td>
<td>Yes</td>
</tr>
<tr>
<td>7 SACQ Solder</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>PI</td>
<td>Std</td>
<td>Std</td>
<td>Alloy C</td>
<td>Std</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Conditions Color**
- Reference
- Variables
- All Variables

© 2014 ASE Group. All rights reserved.
ASE Large Die Development – Phase II Results

1st Fail

1. Standard
2. Thk Diel & Thin Die
3. Alloy A
4. Superset
5. Thk Diel & Alloy A
6. PBO
7. Alloy C

63.2% Fail
WLCSP Structure Developments

- **Solderball Pitch**
  - Production – 0.5, 0.4, 0.35 & 0.3mm pitch
  - Internally Qualified: – 0.2mm pitch

- **RDL Lines/Spaces**
  - Production:
    - L/S 10/10um - 4um thk Cu RDL
    - L/S 20/8um - 10um thk Cu RDL
  - Qualified:
    - L/S 5/5um - 4 & 9um thk Cu RDL
    - L/S 2/2.5um - 3um thk Cu RDL

- **Multiple RDL**
  - 2 RDL Layers in Production
  - 3 RDL layers Qualified
Cost Reduced WLCSP Structures

3-Layer WLCSP – Elimination of UBM
- Solderball dropped directly on RDL
- Eliminates 2nd metal layer
- Reduces Price & Cycle time

2-Layer WLCSP – Eliminates Polymer 1 & UBM
- Solderball dropped directly on RDL
- Eliminates 1st Polymer & 2nd metal layer
- Further Reduces Price & Cycle time
- Limited to small die <2x2mm

4-Layer with UBM (Large Die)
3-Layer No UBM (Medium Die)
2-Layer No Polymer/UBM (Small Die)
Embedded WLCSP

- Thick (>=10µm) Copper UBM for Laser Processing after embedding
- Developing die thinning to 50µm
- ASE developing total embedded die solutions
  - Thick Copper UBM & Thin Die
  - JV with TDK for SESUB Embedded Packages
  - ASE in production with embedded die for packages & modules
  - ASE in production with SIP Assembly in Embedded packages
Wafer Level IPDs

- Resistors, Capacitors, Inductors and integrated arrays
- Modeling, simulation, measurement
- Wafer Level or Modules
- Joint Activity with

[Images of various electronic components and layouts]
Example WL IPD Simulation vs. Measurement – Bandpass Filter

- **BPF layout**

![BPF layout image]

- **BPF spec**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Spec</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>2.4</td>
<td>2.5 GHz</td>
</tr>
<tr>
<td>Port Impedance</td>
<td>50</td>
<td>Ohm</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>2.4</td>
<td>dB</td>
</tr>
<tr>
<td>Return Loss</td>
<td>10</td>
<td>dB</td>
</tr>
<tr>
<td>Attenuation @ 824~960MHz</td>
<td>30</td>
<td>dB</td>
</tr>
<tr>
<td>Attenuation @ 1710~1980MHz</td>
<td>30</td>
<td>dB</td>
</tr>
<tr>
<td>Attenuation @ 4800~5000MHz</td>
<td>20</td>
<td>dB</td>
</tr>
<tr>
<td>Attenuation @ 7200~7500MHz</td>
<td>20</td>
<td>dB</td>
</tr>
</tbody>
</table>

- **BPF performance comparison**

![BPF performance comparison graph]
Wafer Level MEMS

- WL MEMS as single WLCSP or as Die to Wafer Assembly

Oscillator MEMS on ASIC – D2W
WLP Die to Wafer Assembly

Mother die

- Bumping Mother
- WLCSP1 Mother
- Flip Chip On Wafer
- Wafer Probe
- Wafer Saw
- PNP
- Ship out

Child die

- Bumping Child
- WLCSP 1
- Grinding Child
- Wafer Saw Child
- Flip Chip
- Test

Grinding Child

MEMS Die to Wafer WLCSP with Solder Bumps

IPD Die to Wafer WLCSP with Cu Pillars
WLCSP D2W MEMS
WLCSP D2W IPDs & Hybrids

- WLCSP D2W IPDs

- WLP D2W Hybrid FC & Wirebond Wafer

- WLP D2W Hybrid FC & Interposer Wafer
**ASE MEMS 3D WLP**

### TSV last manufacturing capability
- Temporary or permanent wafer bonding
- DRIE of TSV last
- Via isolation & Cu fill
- Passivation and RDL

### Wafer Level Molding:
- Wafer scale molding after either FC or WB (compression molding)

### Wafer Level Processing:
- Passivation, RDL & UBM
- Ball Attach
- Laser marking
- Dicing

### Wafer to wafer bonding (device capping):
- Top wafer: Si, Glass, active die wafer (dev)
- Bottom wafer: Si
- Bonding technology: polymer, glass frit
- On going (dev): metal bonding (solder, eutectic)
- Thin film capping, wafer scale plastic lid (under survey)

### Die attach (MEMS or ASIC) to wafer (MEMS or ASIC):
- WB (tape attach), Au wires
- FC attach MR or TCB, solder or Cu pillar, NCP or CUF

---

**Images:**
- Receiving wafer w or w/o carrier
- Molded wafer after die to wafer attachment
- TSV last manufacturing capability diagram
- Wafer Level Molding diagram
- Wafer Level Processing diagram
- Wafer to wafer bonding (device capping) diagram
- Die attach (MEMS or ASIC) to wafer (MEMS or ASIC) diagram
3D MEMS WLP Benefits

**Area** 25 – 77% Reduction

- **PKG** 30%
- **WLP** 70%

**Height** 11 - 40% Reduction

- Mold LGA
  - 30%
  - 74%

- Open Cavity LGA
  - 29%

- Cavity DFN
  - 40%

- 2 dice solution
  - 27%
ASE TSV last solution for MEMS & Sensors

Process 100% done by ASE, current production on 200mm

1. Shorter Development time. (OSAT Learning curve only)
2. Larger TSV size (>30 um)
3. Liability is clear

**TSV last with polymer isolation:**
- Isolation thickness up to 10um
- Good electrical performance & low leakage
- Good sidewall conformity & uniformity
- Low process temperature (below 250°C)
- Low via / Si stress
- Minimized warpage

HVM on 200mm environmental sensor, with high yield and reliability
Fan out Technology
Drivers for Fan out – Advanced Nodes

- **Die Shrinkage**
  - Advanced Technology nodes allow die shrinkage
    - Increased die per wafer & lower die price
    - But - Less die area for Ball placement
  - Fan out allows expansion of ball placement area beyond die borders
    - Fan out cost offset by lower die pricing
    - Retain Ball footprint of larger die WLCSP

- **Multi Die**
  - Advanced Technology nodes increases wafer cost for high technology nodes
    - Not all die functionality benefits from advanced nodes
  - Fan out allows Partitioning of functionality within a package
    - Digital functions can use advanced technology nodes
    - Analog, Power, MEMS, IPDs can use lower technology nodes
    - Fan out allows these various nodes to be embedded in same package
Drivers for Fan out – SiP is Ultimate Goal

- Fan Out SiP - Multi Die & Passives
  - Fan out allows Partitioning of functionality within a package
    - Digital functions can use advanced technology nodes
    - Analog, Power, MEMS, and IPDs use other technologies
  - Fan out allows these various nodes, components, and passives to be embedded in same package
ASE Fan out Strategy

**Chip First – Embedded Chips**

**Cost Driven**
- Panel Fan out (In Development)
- Fan Out Chip Last

**Median Level**
- SESUB Embedded Package
- Wafer Level Fan out
- Fan Out Chip Last

**Performance Driven**
- High Density
- Wafer Level Fan out
- 2.1/2.5/3D Package
- Wafer Chip Last

**Technology**
- Low
- Middle
- High

**Driver**

**Chip Last – Flip Chip**
- ~12µm L/S
- ~8µm L/S
- ~2µm L/S
Die are embedded in a “Reconstituted” plastic wafer that is processed like a Silicon wafer.
FOWLP eWLB Basic Process Flow

1. **Wafer Saw**

2. **Wafer Redistribution**

3. **Wafer Reconstitution**

4. **aWLP Package with Solder Balls & Singulated**
Evolutionary Paths for FOWLP

- Single Die aWLP (HVM)
- Multi Die 2D with Passives FOWLP (Prototype)
- Multi Die 2D FOWLP (Qualified)
- Double sided 3D FOWLP Module Assembly (Prototype)
- Double sided 3D FOWLP Package on Package (Prototype)
Advanced FOWLP (WL Fan Out Chip on Substrate - FOCoS)

- Structure is an Advanced Flip Chip BGA package using Fan out
- Alternative to 2.5D Silicon Interposer technology
- Initial Application
  - MultiDie in aWLP on FC Substrate
  - 16nm & 28nm Die
  - > 40 x 40mm Package
  - SnAg Bumps
  - I/O > 1000
  - Lines/Spaces <3/3µm
  - 3 RDL layers
FOWLP II PoP Chip First

○ Structure
  - Face-up Reconstitution + 3 RDL + UBM (X2)

*The drawing is not shown to scale
FOWLP II PoP Simplified Process Flow

150um Cu post (pitch/UBM = 0.3/0.1mm) RDL build-up on carrier with sputtered layer

Face up Reconstitution Process

Surface Grinding
Si/Cu post = 100/15um

RDL Side 2 Process

Ball Mount + SMT

Carrier DeBonding

Cu post = 150um
FOWLP – Fan Out Wafer Chip Last

- Die bumped with Copper Pillars
- RDL Trace pattern formed on 300mm Wafer carrier
  - Multi-Layer
  - 2µm/2.5µm Lines/Spaces
- Die to Wafer Flip Chip Mass reflow bonding
- Over mold to encapsulate and underfill die
- Wafer Level Backend processing
Fan Out Wafer Chip Last

**Single Sided**
- RDL on Carrier Wafer
- Flip Chip Die on Carrier
- Overmold Carrier
- Remove Carrier, Drop Solderballs

**Double Sided**
- RDL on Carrier Wafer
- Plate Copper Pillars
- Flip Chip Die on Carrier
- Overmold Carrier
- Grind to expose Cu Pillars
- Plate RDL on Top Surface
- Remove Carrier, Drop Solderballs
- Package on Package (POP)
- System in Package (SIP)
Fan Out Wafer Chip Last (FOWCL)

- **Advantages**
  - Known good die process before C2W
  - No die bond shift and wafer warpage
  - No need for low temperature cure dielectric material

- **Properties**
  - Embedded Silicon w/ molding compound surrounding (6-side)
  - Supports fine L/S to 2/2.5um, package size > 20x20mm

- **Applications**
  - Mid-end: AP/Baseband + RF/Analog, PMIC
  - High-end: Networking, GPU, APU

- **Fan Out Chip Last SiP**
  - > 50 Active & Passive components
Fanout Enables High Density SiP

- ASE is evolving new packaging innovations for miniaturization, performance, and cost improvements.
Fab Fanout SiP vs ASE Advanced Fan Out SiP

FAB Model

- Single-Sourced Die
  - Die 1 40nm Fab1
  - Die 2 28nm Fab1
  - Die 3 14nm Fab1

ASE Model

- Multi-Sourced Die
  - Die 1 40nm Fab1
  - Die 2 28nm Fab2
  - Die 3 14nm Fab3

- Multi-Sourced Components

- Multi-Sourced Passives

Single-Sourced Heterogeneous SiP
Fab Fanout SiP vs ASE Advanced Fan Out SiP

FAB Model

ASE Model

ASE’s Model allows greater versatility for SiPs
Ultimate Packaging Convergence

- Wirebond
- Substrates
- Flip Chip
- WLCSP
- Fan Out
- Embedding
- MEMS
- IPDs
- 2.5D & 3D
- Shielding
- Antennas

SiP
Thank You

www.aseglobal.com