Hierarchical 3D-IC Design
Enabling System Level Design Optimization

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| Founded                  | 1976 |
| Revenue Year Ended March 2014 | $202,920,030 |
| Corporate Headquarters    | Yokohama, Japan |
| European Headquarters     | Munich, Germany |
| North American Headquarters| Westford, Massachusetts |
| Stock Listing             | Tokyo Stock Exchange Level-1 |
| Employees                 | 1,171 |
| Operational Excellence    | Profitable, no debt |
Global Organization
More Than 30 Offices Worldwide

Zuken GmbH
European Headquarters
Munich, Germany

Zuken Inc.
Worldwide Headquarters
Yokohama, Japan

SOZO Center

Zuken USA Inc.
North American Headquarters
Westford, Massachusetts
Zuken Corporate Profile
What We Do

We partner with our customers to develop and deliver software and services to improve our customers’ business success

- Software development, sales, and support
- Implementation and integration services
- Process automation and optimization
Design Trends
Advancement in cloud computing and “Big Data”

Growth in wearable devices

Expansion of “smart” application in automotive, healthcare, and other industries

Ongoing integration of smart devices

Increased implementation of gestural computing

Continuous innovation in technology will require advancement in IC packaging technologies.

This includes substrate/silicon interposer design and 3D IC/TSV, and careful implementation of high-speed interfaces!
Historic System-level Design Challenges

• Single design tool view prevents system level optimizations and leads to over-margining

• Discrete design and planning databases create gaps in constraints, data fidelity/coherency and IP reuse

• Lack of ECAD and MCAD integration under-constrains design before prototyping

• Neutral file interchange formats have scant ECO support and are easily out of synch with current design status
System-level Co-design
System-level Co-design Challenges

Simulation and Analysis:
- Thermal, EM, RF
- Electrical
- Mechanical

ICs Interposers

2.5/3D design, optimization, and visualization

Mechanical Enclosure

Support for any combination of co-design is key!

DRC, MRC rules and electrical and physical constraints

System Co-Design

Package
- SiP
- PoP

Net assignment, routability and performance

PCB
- FPCB
- Rigi-flex
Chip/Packag Co-design
RDL/IO/bump Optimization

Feasibility and Design

• **Constraint Driven Route Pathfinding**
  • Fan Out/In
  • RDL
  • Die Escape
• **Bump ‘Tile’ Macros**
  • Supports System Level Hardmac P&R
  • Known RDL+Escape Solutions
• **Constraints Driven Pin Optimization**
  • Dsgn/Mfr. Rules
  • Interface Constraints
  • Routing Layer Availability
  • Partial Routes
• **OpenAccess IC Format**
  • LEF/DEF & GDS Import/Export
• **“In situ” Feasibility**
  • Route Feasibility & Design in One Tool

4 PKG Layer (1-2-1)
6 PKG Layer (2-2-2)
8 PKG Layer (3-2-3)
RDL Route (LSI side)
Escape Route (PKG side)
Interposer Co-design
Managing complex designs with TSVs

- Floorplanning of stacked/adjacent chips with TSV and Si-Interposer
  - Routing to fixed TSV on interposers from 1 or 2 sides
  - Solve the routing of chip RDL and fixed layer count interposer
  - Generate power/ground mesh in Si-Interposer
Advanced Package Co-design
PoP/SiP/WLP design

• System-level co-design enables intelligent PoP and SiP design
  – Seamless connection of independent databases
  – Focused design rule checks for PoP/SiP with real-time 3D view
  – Support for complicated bond wire placement of stacked die

3D DRC for bond wires
Package/PCB co-design
Multi-PCB/Flex

• Conduct real-time pins swaps between package and board
  – Improve routability with automatic or interactive untangling of nets
  – Improve signal performance and power delivery
  – Eliminate exchange of CSV or other neutral files to communicate change

Hierarchical structure of package and board

PCB Design
PKG Design

BGA Package Component

CSV

CSV File

Pin Number
Net Name

Reflect
Net Swap
System-level Co-design
SoC/SiP/PCB

• Supports state-of-the-art chip design with unique package technologies with multi-board integrated design
  – Optimize I/Os across the system in real-time
  – Conduct design trade-offs for various form factor or application
  – Consider board-level issues concurrently with the mixture of above technologies and SiP
Electromechanical Co-Design

- 3D environment enables design to true mechanical constraints
- Identify critical placement issues early in the design process
- Conduct measurements and collision checks for optimal floorplanning
System Co-design Case Study:

Portables
Case Study: System-level Co-design

- Challenges in form factor-driven design:
  - RF module placement
  - Physical specifications
  - Thermal dissipation
  - Form and fit
  - Product cost
  - Package technology

Almost all domains are modules
Case Study:
System-level Co-design

Existing RF module has to be redesigned to meet new form factor requirements

Profile of chip is too thick to be embedded within module package

Shrink module size 6mmX8mm ⇒ 4.5mmX6mm

Module height 1.7mm ⇒ 1.0mm

It is difficult to place all components on surface

Custom LSI won’t go into the module
Case Study: System-level Co-design
Optimizing Signals in the System

- Chip RDL routing optimized in context to the module and PCB without die redesign
- 3D rule and technology update enabled embedding and physical verification to new form factor specification

![RDL Package on PCB Module + RDL](image)
System Co-design Case Studies:

2.5D/3D Systems
Case Study: eWLB Wide IO Memory Design

Hierarchical System Architecture

System Level Constraints and Netlist

3D-IC System level Design
- eWLB
- 2 Embedded openAccess IC databases
- PoP Memory
- Memory

IC Hardmacro and Routing

3D Editing of Native Database
System Level Co-Design Functionality
Execution in Multi-board Database

- System Level Net Swap without .CSV
- IC HardMacro
- WLP Routing
- 3D Design in System Level Visual Context
Stacked 3D Pathfinding:
System “Best Pin” Pathfinding in Native Design Tool
Stacked 3D Pathfinding: Verification and ECO Management
Pathfinding: Logical, Physical & Cost Planning
Pathfinding:
Logical, Physical & Cost Planning
Component Weight & Power

Floorplan Driven

Functional Partition Driven

Enclosure Driven
Pathfinding: Logical, Physical & Cost Planning

System A

System B
Pathfinding: Planning to Realization….Planning vs. Final

- IP Reuse
- Planning vs. Design Coherency
- Properly Constrained Planning
- Planning Constraints Transferred to Design Stage
Roadmap and Summary
Roadmap

- System-level, Constraint-driven Design
  - System level physical and electrical constraints
  - Reduce program cost due to system over-constraining
  - System & Component PDK

- System-level analysis
  - Integrated cross module physics simulation, meshing and modeling
  - Removal of artificial modeling discontinuities at component boundaries

- Expanded system path-finding with IP reuse
  - System planning and path finding with direct translation to constraints and design jumpstart
Summary: Co-Design EDA Requirements

• 3D platform with dedicated DRCs to ensure system level physical verification and provide system level product insight

• Use of independent, but connected databases to provide opportunities for system optimization throughout the design process

• Pin assignment and routing automation to enable realizable path finding and quick turn ECO changes

• System level electrical and mechanical collaboration and checking to ensure realizable design
The Partner for Success