22FDX™ Platform
Enabling solution for IoT, Mobile, RF, and Networking Applications

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Leading Edge - Product Line Manager

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FD-SOI Enables Lower Cost per Transistor

Historical first: cost per transistor is rising

Source: Handel Jones - IBS, *Feature dimension reduction slowdown, 3/20/2012*
FinFET & FD-SOI Solve Different Market Needs

Bulk CMOS

- Lowest Cost
- Leakage

FinFET

- High Performance

FD-SOI

- Best Power/Performance/Cost Tradeoffs
22FDX™ Platform Enables Differentiated Customer Solutions

Server

High Performance Computing & Switching

High-end Mobile Application Processor

Wired Networking, Consumer Applications Mid-Range Smartphone

IoT, Wearables, Sensors, Low-end Smartphone

28HPP

14LPP/LPE

28SLP

22FDX
Introducing 22FDX™ Platform

- Industry’s first 22nm fully-depleted silicon-on-insulator (FD-SOI) technology
- Delivers FinFET-like performance and power-efficiency at 28nm cost
- Ultra-lower power consumption with 0.4 volt operation
- Software-controlled transistor body-biasing for flexible trade-off between performance and power
- Integrated RF for reduced system cost and back-gate feature to reduce RF power up to ~50%
- Enables applications across mobile, IoT and RF markets

- 70% lower power than 28HKMG
- 20% smaller die than 28nm bulk planar
- 20% lower die cost than 16/14nm
22FDX™ Transistors

Electron micrograph of GLOBALFOUNDRIES FD-SOI transistors

NMOS

PMOS
22FDX™ enables improved electrostatics

Improved electrostatics:
- Short channel effect
- higher gm
- lower gds

Achieved by truncation of both junction depth ($X_j$) and depletion zone width under gate ($T_{depl}$).

\[
DIBL = 0.8 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left[ 1 + \frac{X_j^2}{L_{el}^2} \right] \frac{T_{ox} T_{depl}}{L_{el} L_{el}} V_{ds}
\]

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\]
Agenda

1. 22FDX™/FD-SOI technology overview
2. Transistor control with body biasing
3. Applications – RF/Analog
Architected for Effective Body-biasing

Provides greatest power efficiency and design flexibility

- Forward Body Bias (FBB) enables low voltage operation down to 0.4V
- Reverse Body Bias (RBB) enables low leakage down to 1pA/micron
- Dynamic body biasing enables active tradeoff of performance vs. power
- Can be used to reduce variability across the die and/or die-to-die
Maximum Flexibility with Transistor Body Biasing

- **Leakage**
- **Power**

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**Reverse Body Bias (RBB)**

- Minimum Leakage
- In Standby Mode

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**Forward Body Bias (FBB)**

- Maximum Performance
- Operating Mode

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Max Frequency
Combining DVFS with Dynamic Body-Bias
Provides Best Performance-Power Tradeoffs

- Best perf./watt
  - 1x $F_{max}$
- Best performance
  - 1.6x $F_{max}$
- Lowest total power
  - 0.5x $F_{max}$

Graph showing relative leakage power vs. relative active power with different body-bias conditions:
- Fwd Body-Bias
- Rev Body-Bias
- No BB

Key points:
- Vdd-100mV
- Vdd+100mV
- -60mV Vt
- +60mV Vt
- 1x $F_{max}$
Forward Body-Bias Extends FD-SOI Flexibility

- 50% lower power at same frequency
- 40% faster performance at same power
- Low Vdd operation (down to 0.4 volts)
- FBB Advantage: Software-controlled body-bias enables dynamic tradeoffs between power, performance and leakage
22FDX™ Benefits for Low-Voltage Operation

Run at 0.5V with 76% lower power and iso-frequency compared to 28HKMG
22FDX™ Offers Multiple Types of Transistors

Optimize for Leakage and Performance

**Relative Performance**

- 1.0
- 0.8
- 0.6
- 0.4
- 0.2
- 1.2

**Relative Leakage**

- 0.0
- 1
- 10
- 100
- 1000
- 10000
- 100000
- 1000000

**SLVT/LVT**

- Lowest $V_T$
- Optimized for FBB
- Highest performance

**RVT/HVT**

- Mid-range $V_T$
- Optimized for RBB
- Balance of low leakage and high performance

**ULL**

- Optimized for leakage
- Coupled with RBB achieves ≈1pA/um leakage
Multiple Body-Bias and Vt Points on Same Die
Optimize Standby and Dynamic Power

FD-SOI Delivers:
- Low static and dynamic power
- RF integration for reduced BOM cost
- RBB and FBB for power/perf tradeoffs

Integrated RF
- Wakes up comms to transmit message
- RBB for lowest leakage
- Detects motion

Wireless Comms
- "Watchdog" Processor
- ON

FBB for lowest dynamic power
- Wakes up Image Processor to zoom in and analyze

GLOBALFOUNDRIES Confidential 16
### Agenda

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>22FDX™/FD-SOI technology overview</th>
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<tbody>
<tr>
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<td>2</td>
<td>Transistor control with body biasing</td>
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<td>3</td>
<td>Applications – RF/Analog</td>
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## End Market Success Demands Optimal Technology

<table>
<thead>
<tr>
<th>Segment</th>
<th>Requirements</th>
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<tbody>
<tr>
<td><strong>Consumer (STB/DTV)</strong></td>
<td>Energy Star goals and smaller form factors</td>
</tr>
<tr>
<td><strong>Wearables</strong></td>
<td>Longer battery life and RF integration to reduce system cost</td>
</tr>
<tr>
<td><strong>IoT/Industrial (MPU, ISP, MCU)</strong></td>
<td>HD image/video, integrated RF/eNVM, battery operation</td>
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<tr>
<td><strong>Mainstream Mobile</strong></td>
<td>Display, video, and wireless needs w/o FinFET cost</td>
</tr>
<tr>
<td><strong>Auto/Info-</strong></td>
<td>Lower $T_j$ at 125°C ambient and better Soft Error Rate (SER)</td>
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<tr>
<td><strong>WiFi/RF</strong></td>
<td>Higher data rates at lower power</td>
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22FDX™ Platform Extensions

- **22FDX Base Platform**
  - Core Vts
  - 2 IO Vts @ 1.2/1.5/1.8v
  - Passives
  - SRAMs (HD, HC, LV, ULV, TP)
  - 8T/12T libraries
  - Software controlled Fwd/Rev body-bias

- **-ulp adds** logic libraries and memory compiler optimized for 0.4v logic operation

- **-ull adds** devices, libraries, and memory compilers to achieve 1pA/um leakage

- **-uhp adds** optimized BEOL stacks, 12T libraries optimized at OD, high-speed SERDES (16/28GHz), and MIM capacitor

- **-rfa adds** RF enablement, BEOL passives, and IP for BTLE, WiFi

Base platform PDK & IP

Application-optimized extensions
22FDX™ Benefits RF Applications

• Device Physics Advantage with FD-SOI
  – SOI structure allows more flexible layout reducing overall parasitics at larger pitch
  – FD device gives higher self gain than bulk at the same Lg
  – Planar structure allows for lower Rsd and Rg compared to Finfet
  – Local Back Gate bias give dynamic control of threshold voltage for innovative circuits
  – 20nm short Lg increases gM and $f_T$ performance
  – HiKMG enables low Tinv and high channel charge
22FDX™ improved electrostatics enable higher operating $f_T$, higher self-gain at high gain efficiency bias

Each curve is constructed by simulating multiple $L_g$ for that technology. $V_g$ is swept and $f_T$ and self gain found for the $V_g$ where $g_m/I = 15$ V$^{-1}$. The right most point on each curve is the minimum allowed $L_g$. Longer FETs have higher self gain and lower $f_T$. 

**SelfGain vs. $f_T$ at $g_m/I = 15$ V$^{-1}$**
Compact Model
Simulation slvtnmos
Ids, gm
vs. Forward back-gate bias

Vds=530mV

Forward Back-gate bias enables linear Gm over wide output current range and to high current density
Dynamic Range Increase with 22FDX
For RF back gate bias reduces the VT and extends the dynamic range

- Dynamic range increases by ~60mV/V of FBB
RF Circuit Benefits for 22FDX
Reverse-back-gate biasing optimizes gain efficiency while maintaining dynamic range

Conventional approach (non IMG)

Approach w/ IMG

- High gm/l
- No bias circuit AC signal path losses
- Voltages held mid-rail for maximum dynamic range

- 22FDX is an Independent-Multi-Gate (IMG) Technology
- Back-gate utilized to optimize bias current and transconductance
- Free up front-gate voltage for signal path dynamic range
- Eliminate bias circuitry losses of single-gate technologies such as bulk and FinFET
FD-SOI Case Study – Smart Watch

Next Generation Device Specification

- CPU Freq. 1.5+ GHz Vdd 0.6v
- SRAM up to 16Mb
- -25C to +85C
- Integration Path: BLE, WiFi, PMIC

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<th>40LP</th>
<th>28SLP</th>
<th>FinFet</th>
<th>FD</th>
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40nm wearable device today
FD-SOI Case Study – Smart Watch

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~5x battery life increase from 4 to ~20 days
FD-SOI Case Study – Smart Watch

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RF Enablement

40nm wearable device today
Summary

• Leadership position with new 22FDX FD-SOI platform
• Best combination of performance, power and cost
• Enables FinFET like performance and power efficiency at 28nm cost
• Innovative circuit topologies by leveraging body-bias in AMS design
• Optimized for Mobile, IoT, and RF
Thank you for attending!

- Learn more at GLOBALFOUNDRIES.com
- Replay today’s webinar, available at:
  - Chipestimate.com
  - GLOBALFOUNDRIES.com

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Industry Support for FD-SOI

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<th>Foundries/IDMs</th>
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<tr>
<td>Global Foundries</td>
<td>SONY</td>
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<td>SAMSUNG</td>
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<td>cadence</td>
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<td>VeriSilicon</td>
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