Analog and Mixed Signal Designs using FinFET Technology

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Challenges for Analog Design in Advanced Planar Deep Sub-Micron Processes and FinFET as a solution

Extra Care Abouts for FinFET

Analog Benchmark FinFET vs. Planar

Broad Range of Platforms

Center of Excellence
- Analog & Mixed Signal Technologies
Challenges for Analog Design in Advanced Planar Deep Sub-Micron Processes and FinFET as a solution
Intrinsic Gain (Gm*Rout) decreases as we go from 28nm to 20nm.

Av: Normalized to 28nm

@ Same Bias Conditions
Headroom decreases as we go from 65nm -> 20nm

\[ \text{Headroom} = V_{gs} - V_{t(sat)} \]
For a given Useful Power Standby Power increases

Normalized to 65nm

3x increase in Standby Power
Planar CMOS on bulk substrate has been the workhorse of the foundry industry for high performance and low power. Cost effective substrate, easy to integrate SoC passives (diodes, capacitors, varactors, resistors).

Higher doping to control drain degrades sub threshold slope, mobility, junction leakage, and increases variation.
Evolution from Planar to FinFET

Increase gate control by wrapping the Gate around the channel and reduce drain control for steeper sub-threshold slope for lower voltage operation and better short channel effects.
Introduction to FinFETs and Analog Advantages of FinFETs
Fin Geometry, Dimensions & Operation for Bulk FinFET

- \( W_F = \text{Fin Width} \)
  - This is critical for maximizing FET density.

- \( H_F = \text{Fin Height} \)
  - This directly effects FET performance.
  - Effective Width = \( 2H_F + W_F \)

- \( L_G = \text{Gate Length} \)

Region where gate will cover

Regions of Current Flow

Shallow Trench Isolation (STI) or Local Isolation
FinFET (14XM) vs. Planar: Better Short Channel Effects (SCE)

Decrease in Vt: Planar -> FinFET

Better SCE due to the fin leads to -
- Larger Head room
- Better SS at lower Lg
- Higher Gain at lower $\frac{W_{\text{eff}}}{L_g}$
Analog Performance: FinFET (14XM) to Planar: Better Gate Control leads to Higher Gm

Gm is higher between FinFET and Planar and scales well with Length.
Analog Performance: FinFET (14XM) to Planar: Better Gate Control leads to Lower Gds

Gds is lower for FinFET compared to Planar.
Analog Performance: FinFET (14XM) to Planar: Better SCE, High Gm and Lower Gds leads to Higher Intrinsic Gain

Planar @ Same Bias Conditions

~45%

Av: Normalized to 28nm

28nm 20nm 14XM
RF Performance: FinFET (14XM) to Planar Similar in the Operation region of importance to RF

- FinFETs and Planar have similar cutoff frequencies in \( V_{gs-Vt} \approx 0.2 \)V region over lengths. (\( V_{ds} = V_{dd} \))
- For the bias conditions where the transistor operates in most of the low power Analog/RF applications, intrinsic \( f_t \) are comparable to the planar 20LPM devices.
FinFETs vs. Planar: Low Freq Noise: NMOS: Similar Slopes and Magnitude

\[ \gamma \left( \frac{1}{f^\gamma} \right) \text{ are similar between Planar and FinFET} \]

@ Same Bias Conditions
FinFET Process has Finified Passives: Characteristics of P+/NW Diode better than Planar

At least 5 orders of linear region
Extra care-Abouts FOR FINFET of analog BLOCKS
## SoC Electro-Migration Issue for FinFETs

<table>
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<tr>
<th>Challenges</th>
<th>Impact to EM</th>
<th>Mitigation Strategies</th>
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<tr>
<td>Normal node scaling challenges to EM Juse</td>
<td>High intrinsic EM performance needed, w/o big R impact</td>
<td>EM focused process improvements</td>
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<tr>
<td>Higher drive current requirements for FINFETs</td>
<td>Wider Power rails, Early failure and/or Area impact at SoC level</td>
<td>More accurate assessment of EM risk in complex geometries and Std cells should support Wider Power rails</td>
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No FinFET Solution without solving EM Issue!
Effect of $R_{EXT}$ on Analog FoMs

~20%
Gate Length Limitation is not really a Limitation!!!

- **Higher** \( R_{\text{OUT}} \) **OR Lower** \( G_{\text{DS}} \)
  - Similar \( G_{\text{DS}} \) can be got with much smaller length

- **Mismatch Criterion**
  - \( A_{\text{VT}} \) targets for FinFET are lesser than Planar, \( L_{\text{FinFET}} \) ~ is significantly smaller than \( L_{\text{Planar}} \) for similar \( \sigma_{\text{VT}} \) for same width.

- **Quantized Width**
  - Quantized Width could lead to some limitations on sizing of the device
Generic Process Flow: Mandrel Position determines Fin Position

Fins created at the sides of the Mandrel By SIT process.
One more layer to worry about to reduce mismatch during Layout : Mandrel

Odd # of Fins in a single RX

Polygon:
Identical Mandrel placement necessary
Non-Identical Mandrel placement could cause for variation

Even # of Fins in a single RX

Polygon:
Placement of Mandrel not an issue

Upfront Design Solution – Make sure that Diff pairs are designed such that they have even # of Fins. For centroid type layout, for example, designed # of Fins should be mod(#of Fins, 4)=0
Passives Limitations in a FINFET Process

- Compared to Planar:
  - Gate Density Requirements are stringent.
  - Length is quantized due to Dummy PC
  - Height is quantized due to Fin Pitch
  - Cut Mask mask for all the PC – (Good layout practice in general).
• **Power:** The TX pre-driver in 14nm takes about 40% less power than the 20nm design.

• **Performance:** The 14nm design edge rate for most of the stages is almost double as compared to the 20nm design.
Devices in 14XM that are important for Analog/RF

<table>
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<th>Active Devices</th>
<th>Passive Devices</th>
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<tr>
<td>Super-Low-Vt NFET</td>
<td>N+ diode</td>
</tr>
<tr>
<td>Super-Low-Vt PFET</td>
<td>P+ diode</td>
</tr>
<tr>
<td>Low-Vt NFET</td>
<td>N-well Resistor</td>
</tr>
<tr>
<td>Low-Vt PFET</td>
<td>Metal Resistor</td>
</tr>
<tr>
<td>Reg-Vt NFET</td>
<td>N-well Substrate Cap</td>
</tr>
<tr>
<td>Reg-Vt PFET</td>
<td>SG/EG NCAP</td>
</tr>
<tr>
<td>1.2V, 1.5V and 1.8V EG I/O NFET and EG I/O PFET</td>
<td>Vertical PNP Bipolar</td>
</tr>
<tr>
<td>1.2V, 1.5V and 1.8V EG I/O PFET</td>
<td>MIM</td>
</tr>
</tbody>
</table>

Other devices of Analog Interest (experimental @ this stage): ZVT, ULVT
All the devices supported in a Planar process supported in 14XM
Broad Range of Process Platforms

- Analog, Power & Mixed-Signal
- 180 – 40nm Mixed-technology Solutions
- 28nm Perf/power/cost Optimized
- 20nm Planar Cost-optimized, Unified
- 14XM FinFET eXtreme Mobility

In development

Volume production-proven
Center of Excellence – Analog & Mixed Signal Technologies

Platforms & Technologies

- 0.18um modular platform (Digital/ Analog/ Power/ eNVM)
- 0.13um modular platform (Digital/ Analog/ Power/ RF/ eNVM)
- 65/55nm modular platform (Digital/ Analog/ Power/ DDI/ eNVM)
- 40nm modular platform (Digital/ Analog/ RF)
Acknowledgements

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Summary

- Challenges to Analog/RF Design in Planar Submicron Processes presented.
- Advantages of FinFET over Planar for Analog Performance.
- Analog Benchmarking using real SOC Analog blocks. Simulations results presented.
THANK YOU!