Designing with FinFETs
Evolution or Revolution

GSA meeting

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Jan 23, 2013
Agenda

- FinFET – the device
  - From Planar to FinFET
  - The promises and challenges
  - Bulk vs. SOI

- Designing with FinFETs:
  - General design issues: the transition from planar to FinFET
  - SRAM design

- Reliability Concerns
  - HCI, NBTI, PBTI, and SER

- Summary and conclusions
Key Challenges for Nanometer Technology

**Physical limits in scaling Si planar MOSFET**

1. Decreasing mobility
2. Increasing gate leakage currents
3. Increasing sub-threshold leakage currents
Improving $I_{ON}/I_{OFF}$

• The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.

→ higher $I_{ON}/I_{OFF}$ for fixed $V_{DD}$, or lower $V_{DD}$ to achieve target $I_{ON}/I_{OFF}$

→ reduced short-channel effect and drain-induced barrier lowering:

\[ S \propto \frac{C_{total}}{C_{ox}} \]
FinFET Design Considerations

- **Fin Width**
  - Determines SCE

- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency vs. design flexibility

- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance vs. layout efficiency
Sub-Lithographic Fin Patterning

Spacer Lithography
a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

1. Deposit & pattern sacrificial layer

2. Deposit mask layer (SiO$_2$ or Si$_3$N$_4$)

3. Etch back mask layer to form “spacers”

4. Remove sacrificial layer; etch SOI layer to form fins

Note that fin pitch is 1/2× that of patterned layer
FinFET Lithography

- The first FinFET generations will still be produced using 193nm immersion lithography tools.
- The resolution required for patterning at or beyond 20nm technology may require some form of double patterning for the fin and gate levels.
- The “spacer double patterning” process is preferred for the patterning of the fins.

IBM’s process for fin patterning (top view).
A “mandrel” is a temporary supporting pattern.
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Design Methodology/Tools Impacts

- New SPICE models
- Differences in parasitic RC extraction
- Quantized transistor width
- Exaggerated layout dependency issues (lonely FET)
- New design rules for physical verification
- New design rules for custom IP
3D FinFET Geometry Parasitics

- Complex 3D Parasitics - more challenging to extract
  - Extension Resistance, Contact Resistance, Fringing and Coupling cap

- Coordinated modeling techniques between HSPICE and StarRC
  - StarRC handles layout variant portions
  - HSPICE model handles layout invariant portions
FinFET Modeling With BSIM-CMG

Similar model topology as planar BSIM4
Detailed Capacitance Components

<table>
<thead>
<tr>
<th>Caps</th>
<th>Name</th>
<th>Domain</th>
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<tr>
<td>Gate to top of fin diffusion</td>
<td>Cf</td>
<td>Extraction</td>
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<tr>
<td>Gate to diffusion inside channel</td>
<td>Cc1, Cc2</td>
<td>Spice Model</td>
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<td>Source to drain diffusion</td>
<td>Csd</td>
<td>Spice Model</td>
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<tr>
<td>Gate to substrate inside channel</td>
<td>Cg</td>
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<td>Gate to substrate between fins</td>
<td>Cg2</td>
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<tr>
<td>Gate to diffusion between fins</td>
<td>Cf2</td>
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<tr>
<td>Fin to substrate</td>
<td>Cfin</td>
<td>Spice Model</td>
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<tr>
<td>Bulk diffusion to substrate</td>
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<td>Field poly to diffusion</td>
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</tr>
<tr>
<td>Contact to contact</td>
<td>Ccc</td>
<td>Extraction</td>
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</table>
FinFET Stress Proximity Effects

Nested pFinFETs have strong stress

Isolated pFinFETs relax the stress
(Driving current drops in half!)
Body Bias in FinFETs

• Bottom-line: not useful at all!!

From thesis of Jong-Ho Lee
Seoul National University
How about Analog Design w. FinFET? OPAMP Design With FinFETs

The effect of discrete widths is negligible due to the large multi-fin transistors with non-minimum gate lengths

- Bode plot (gain vs. frequency) configured as a 20dB inverting amplifier.

- The low-frequency open loop gain is $A_0 = 45$dB. This is comparable with typical open loop gains achievable in deep sub-micron planar CMOS technologies.

(Christian Pacha, 23.2, ISSCC, 2006)
FinFET SRAMs – The Good News

• Higher performance and lower leakage compared to planar

• Operates at a lower Vdd than corresponding planar
  – Positive leakage and dynamic power implications

• Good static noise margin (SNM) at low Vdd
  – A decent noise to signal ratio can be achieved (with a $\beta=2$ for example)
  – Good (Low) Variability
    – Even a 10% fin height variation results in a small SNM variation
  – Read Margin (RM) and Write Margin (WM) distribution narrower than in planar technology

N. Lindert et al., DRC paper II.A.6, 2001
FinFET Impact on SRAM Design

- $\beta$ Quantized
- No area penalty / smaller area than planar at $\beta=2$

Advantages
- Lower $V_{\text{min}}$ operation
- Small static noise margin (SNM) variation
- Narrower Read Margin (RM) and Write Margin (WM) distribution

Challenges
FinFET, not SRAM specific
- Body-bias techniques are not efficient
- Self-heating
- No experience with NBTI and PBTI (110 orientation)

Source: Kawasaki et al, 2006 Symposium on VLSI technology Digest of Technical Papers
FinFET Design Challenges - general

• With node scaling, channel area decreases and $\sigma V_t$ increases
  – $V_t$ mismatch issues (challenges stemming from variation of $T_{ox}$, $\varepsilon_{ox}$) and work function along the fin height

• Planar FETs are usually manufactured with (100) surface orientation while FinFETs are manufactured with (110)
  – Concern for embedded memories: carrier mobility impact

• Resistance and capacitance of source/drain regions is a remaining hurdle for good performance in FinFETs

• Availability of mature device models that capture FinFET effects associated with new surface orientation, surface scattering, ballistic transport, corner effects, etc.
FinFET Summary - Pros and Cons

Pros

- Enables additional scaling dimension and continued scaling for some generations
- Improved electrical characteristics
  - Lower leakage
  - Less variability caused by random dopant fluctuations thanks to lower doping levels or no doping in channel
- This enables lower operating voltage

Cons

- Risk: Bigger step than scaling planar technology
- More expensive to manufacture
- Quantized widths
- No body biasing
- Higher parasitics
- The fins are thermally more insulated
  - Self-heating could become problematic
  - Thermal aspects of ESD (electrostatic discharge) protection
- Degradation and aging: New yield loss mechanisms?
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Aging – a new “old” phenomena

- HCl = hot carrier injection
  - Very old phenomena – high drain-gate electric field causes carriers’ (electrons) tunneling and entrapment in the thin gate oxide causing a $V_t$ increase and mobility degradation with time.
  - N-Devices
  - Concept is used intentionally in FLASH memory
  - Not reversible. Well understood since the 2um node. With scaling and increased electric fields it was handled through LDD (lightly doped drain)
NBTI / PBTI

- N/PBTI = Negative / Positive Bias Temperature Instability
- NBTI degradations of PMOS transistor originate from Silicon Hydrogen bond (Si-H) breaking at Silicon-Silicon dioxide (Si-SiO2) interface under negative gate stress (Vgs =Vdd))
- PBTI degrades N-Devices, but the degradation of N-Devices compared to P-Devices is insignificant
  - Thus PBTI is seldom mentioned

![Diagram](image-url)
Aging – a new “old” phenomena

- NBTI is:
  - AC phenomena (partially reversible)
    - In some instances total de-trapping possible
    - Most common is partial de-trapping
    - Pretty hard to model de-trapping
  - Function (highly dependent) of the high-k dielectric stack material(s)
    - Density of traps in the dielectric
    - The gate formation process (PNO, RTNO, ANO)
  - Charge trapped in dielectric is function of bias and of temperature
    - Temperature dependency is severe (example: 5X factor performance degradation between 125 degrees and 25 degrees, all other conditions same)
Impact of NBTI on threshold and delay

Fig. 5. Threshold voltage shift at fixed bias voltage and different operation temperature. The shift increases with increase in temperature.

Fig. 6. Transistor delay degradation at different operation temperature.
A “Sample” equation for NBTI

\[
\Delta Vt = \left( 3.8 \times \sqrt{|Vgs - Vt|} \times e^{\frac{1}{|Vgs - Vt|}} \times T^{-0.25} \times t^{0.25} \right) + \left( 10 \times e^{-\frac{800}{T}} \times t^6 \right)
\]

Where:

- Vgs, Vt are in volts, T is absolute temp, t is in seconds, \( \Delta Vt \) is in mV

- Note: there is no Vds component in the equation. More on that later in the experiments section
Sample NBTI/PBTI simulated DATA

- Most important factor in NBTI / PBTI is “T”
- NBTI >> PBTI
- NBTI/BPTI function of VGS ONLY. NO VDS dependency
- Process corners made little difference
- Load made little difference
- Rise/fall time made little difference
- NBTI/BPTI is sensitive to duration and relaxation time. Toggling is less stressful than always on

<table>
<thead>
<tr>
<th>load</th>
<th>device</th>
<th>δ Vt</th>
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<tr>
<td>N-VDD</td>
<td>N-Device</td>
<td>-3.17 mV</td>
</tr>
<tr>
<td>10ff</td>
<td>N-Device</td>
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<tr>
<td>P-Device</td>
<td>-54 mV</td>
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<tr>
<td>P-VSS</td>
<td>-64.8 mV</td>
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Soft-error rate (SER) – FinFETs vs. Planar

- TCAD simulation indicates that with all variables identical (tech node, channel length, oxide thickness etc..) SER rate in bulk-FinFET based SRAM is better than its planar equivalent.

  "The relative SER of the bulk FinFET SRAM is only 0.06 of that of the planar SRAM since the dimension of the fin structure is small enough to suppress the amount of charge collection from the Si substrate."

- In plain English: charge generation caused by energetic impinging particles is in the substrate. In planar, a lot of it can reach the drain, in FinFET, the conduction is mainly in the channel and, thus most of the charge dissipates in the substrate and NOT in the drain, thus probability of upset is much lower
SER cont’d

(a) Bulk FinFET

(b) Drain current (A/µm)

(b) The ion crossing the drain horizontally

Yi-Pin Fang and Anthony S. Oates
IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 11, NO. 4, DECEMBER 2011
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Summary and conclusions

• Designing with FinFETs is not as disruptive as it might appear
  – More RDR than equivalent bulk, but can learn to live with it
  – Back-end design steps intact
  – Layout dependency effects more severe (lonely FinFET)

• Many advantages of FinFET make a designer’s life easy
  – Low leakage
  – Suppressed SC effects
  – Much lower operating VDD possible and good performance at low VDD
    – Lower retention VDD for SRAMs

• Reliability effects are same or slightly better than BULK
  – Same HCI and NBTI, better SER

• Evolution or revolution? I vote: YES 😊
BACK-UP SLIDES
High-Level FinFET Capacitances

Extracted Caps: (layout dependent)
- C1: S contact to D contact
- C2: Gate to S/D contact

Caps Shared with Spice Model: (layout independent)
- C3: Gate to S/D diffusion
- C4: S diffusion to D diffusion