Challenges Of RF Transceiver Design IC On advanced CMOS Process nodes

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- Summary.
RF transceivers are used everywhere in cell phones, WiFi, broadband devices like WiMax CPE, in Bluetooth, RFID, and other applications.

The price of IC’s is directly proportional to chip size and inversely proportional to the quantity of ICs.

To achieve low cost and high levels of integration, CMOS process technology with fine geometry is utilized.

45nm node is good for digital ICs compared to 130nm node from chip size perspective, is that also true for RF transceiver IC?

The Market size for multiband transceiver is large.

Challenges of power consumption - Both the receiver and transmitter currents need to be reduced, independent power connections as well as a power down pin to reduce power consumption when the chip is in an idle state.
• Meeting electrical parasitic constraints and minimizing signal integrity issues in the interconnect routing while still reaching routing completion, controlling power consumption, staying within the specified die-size and speeding time to market.

• Meeting the SPI interface timing specification.

• Controlling the different modules like LNA, PA, PGA etc across the chip with digital block.
Wireless transceiver applications

Local high throughput delivery
Wired / Wireless

Wired / Wireless

Long range delivery wired & wireless (backbone)
Wired / Wireless

Wired / Wireless

Wired / Wireless
Advantages of SoC Integration

- Increased functionality
- Smaller Size / Form Factor
- Lower Power
  - On-chip interface
- Lower Cost
  - Single package
- Ease of manufacture
  - Minimum RF board tuning
  - Reduced component count
  - Improved reliability
Issues with Direct conversion Rx Architecture

- DC Offsets
- Even-Order Distortion
- I-Q Mismatch
- LO Leakage
- Flicker Noise
Technology choices

- 28 vs 45 vs 130 nm for an RF transceiver IC - design tradeoffs
- Development time line – number of passes – when is the right time to go to 28 nm node
- Is RF and BB on a single chip
- Does RF performance and size get better with 45 vs 130 nm
- Size of RF components in LNA, Mixer, PLL, TIA etc
- Development schedule and cost
- Number of iterations required
- Is it better to go to finer geometry after most of the issues are worked out on a 130 nm node
Key issues with RF transceiver SOC blocks

- Complex BB filter can take up lot of area based on MIM cap available on the process node
- LNA, mixer, PA size does not decrease much with 45 vs 130 nm nodes
- 45 nm gives better NF in LNA but higher leakage currents
- Digital registers and other blocks get smaller in 45 vs 130 nm node
- PA performance is better in 130 vs 45 nm node.
- Digital content in RF blocks is rapidly increasing
- Basebands of multi-standard multi-band RF transceivers could be implemented in advanced process nodes with higher integration capability
## Foundry MIM cap comparison

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Technology/Process</th>
<th>Capacitance/unit area (Ff/um2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>130nm</td>
<td>1 fF/um2 (single)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2fF/um2 (MIM stack)</td>
</tr>
<tr>
<td>B</td>
<td>130/180nm</td>
<td>1fF/um2</td>
</tr>
<tr>
<td>C</td>
<td>Node1</td>
<td>2.8fF/um2 single</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.6fF/um2 (Stack MIM)</td>
</tr>
<tr>
<td></td>
<td>Node2</td>
<td>2fF/um2</td>
</tr>
<tr>
<td>D</td>
<td>180nm</td>
<td>1.35fF/um2</td>
</tr>
</tbody>
</table>
Layout of the digital register and control block
Power Amplifier (Size: 740x472 um2)
Design challenges

User-related issues
- Cost, power consumption
- Form factor

Technical issues
- RX: Noise figure, Blocking behavior
- Synthesizer: Phase noise, sidebands
- TX: Efficiency, Linearity, Noise and spurs
User related Issues

- **Multi-mode radios to support several wireless standards.**
- **RF design in scaled CMOS.**
  - Reduced supply voltage: voltage, current, time…
  - Nanometer transistors: leaky, low gm.ro
  - How to reduce area and power
  - More “digital assistance.”
- **Challenges of Designers**
  - Power consumption / Battery life
  - Range
  - Data rate
  - Cost
CBPF Structure (3rd Order)
TIA Response for Maximum C

M1: 600.0kHz 74.27971dB
When Cf=117.1836pF
Issues with Tx Architecture

- Support for multiple modulation standards
- Power efficiency
- Output signal noise
- Transmit stability
130 nm CMOS 900 MHz transceiver developed by RFIC Solutions
Analog and Mixed Signal: Difficult Challenges

- Signal isolation between digital and analog regions of the chip.

- Integrating analog and high-performance digital functions on a chip (scaling). Difficult to maintain analog performance parameters (mismatch and 1/f noise together with new high-k gate dielectrics). Transition to analog supply voltage of less than 1.8V.

- Integration of analog functions in digital CMOS (depending on new materials or device structures added to digital CMOS process). Problems include SOI, double-gate devices and changes in material choices for passive devices. Transition to analog supply voltage of less than 1.0V.
Digital Assisted Analog/RF Design

- Using digital logic to compensate/correct for imperfections of analog and RF circuits to enable:
  - Lower power,
  - smaller area,
  - improved reliability of analog/RF
- resulting in lower cost and improved performance
Digital Assistance: Calibration Issues

- Desired properties of calibration:
  - Independent of temperature, aging, frequency
  - Inexpensive (in time, area and power) to implement
  - Do not interfere with system performance
Digital Interference: Noise Coupling

- **Power Supply noise coupling**
  - Separate or star-connected power supplies

- **Capacitive or inductive coupling to sensitive signals and bias voltages**
  - Careful routing of signal traces to reduce Parasitic capacitive/inductive coupling
  - Use ground return-path shields

- **Substrate coupling induced VTH modulation**
  - Low-impedance substrate connection
  - Guard rings
  - Physical separation
  - Deep Nwell
Complex Transceiver chip with PLL, LDO & band gap reference developed by RFIC for MIPI standard

Latest mobile standard MIPI complaint

Applications:
- Mobile Phone Camera interface
- Mobile Phone Display interface
SUMMARY

- In an RF transceiver going to advanced process node has benefits if the digital content in the SOC is very high.
- Advanced process nodes pose many challenges related to performance and cost of RF transceivers ICs.

- RFIC Solutions has developed 900 MHz transceiver on 130 nm node using many of the 100 plus RFIC blocks already developed which can be used to build any RF system. We are developing a set of programmable transceivers that can be used many wireless radio system.

- Multi mode multi band RF transceiver may be possible with advanced process nodes and can be useful in cell phones, WIFI, broadband devices like WiMax CPE, in Blue tooth, RFID and other applications.
Thank You