GSA MIXED-SIGNAL/RF SPICE MODEL CHECKLIST

Users Guide
Version 1.2, August 2007

What is the GSA Mixed-Signal/RF SPICE Model Checklist?

The GSA Mixed-Signal/RF SPICE Model Checklist is a document completed by a SPICE modeling engineer/department and delivered with each release of a SPICE model set. The first part of this document contains a process overview, contact information, relevant foundry source document references and a list of supported circuit simulators with versions. The second part includes a classification of the models so you can quickly determine the type of model. It includes general extraction information, model validation procedures, statistical variation, considerations for noise and matching (if applicable), and a summary/inventory of the measured vs. simulated results plots for each device. The third part divides device-specific data into active (MOS and BJT) and passive (diode, varactor, inductor, capacitor and resistor) extraction and models. A separate taxonomy document includes definitions for all the terms used in this document and the Checklist.

Audience

This document is intended for analog/MS/RF design managers as a combination ingredients list and "nutrition facts label" for a MS/RF SPICE model. This document helps users obtain a better understanding of the source data, measured devices, completeness and quality of the model before using it to design ICs. It is also designed to be used by fabless SPICE modeling engineers to make better decisions in choosing to modify/enhance/re-fit/re-extract foundry models to satisfy a company's specific product design requirements. Finally, it can be used by PDK developers to better understand the SPICE models they use to build an accurate and consistent PDK.

Revision History

Version 1.0 (August 2005) – Initial release
Version 1.1 (April 2006) – Added recommendations for Verilog (a compiler version notation - section 4.5) and optional "Op Voltage" columns in Section 5 and 6. Checklist remains unchanged.
Version 1.2 (July 2007) – Added abbreviation decoder to Section 4 in Checklist and Users Guide

Understanding and Using the Sections of the SPICE Model Checklist

Section 1 – Foundry and Support Contact Information

This section describes how to contact the foundry for any questions relating to the model.

1. Foundry – Name of foundry company and fab location, or number if relevant.
2. Process – Process code and modifiers that uniquely define the process, and all process options that could affect the model or differentiate the model from another process derivative.

3. SPICE Model Support Contact – Describes how to contact the foundry for any questions relating to the model. It may contain a Web site URL, name, phone, fax, e-mail or a combination.

Section 2 - Foundry Modeling Documents

This section includes references to: (1) foundry documents used to create the model; (2) documents describing the source of data used in the model; or (3) the methodology and trade-offs used to obtain measured vs. simulated data. Each foundry has a different method of naming and bundling these documents into single- or multiple-subject documents.

1. Document Number & Title – The identifier that is used to link the document, the process and its derivatives.
2. Section – Some foundries put many of the documents described in this section into a single manual. If so, then this field describes which volume or section.
3. Revision – Many foundries use a version numbering system (0.X for pre-production, 1.X for risk production and 2.X for full production) of a model or document.
4. Date – The release date of the document or data file.
5. SPICE Model Library – All model files (.lib or separate model cards).
6. Measured vs. Simulated Data – The document (if separate or if in a single design manual, which section) with data plots.
7. Noise Model - The document (if separate or if in a single design manual, which section) addressing noise model issues.
8. Matching Model - The document (if separate or if in a single design manual, which section) addressing LPVM issues.
9. Design Rules - The document (if separate or if in a single design manual, which section) addressing layout geometry rules for the process. This document (or a separate document) may include electrical rules or the process control monitor (PCM) specification for the process. This may include the DRC/LVS/LPE runset that interprets and verifies the latest design rules (often a separate foundry document).
10. Device Characterization Report - The document (if separate or if in a single design manual, which section) addressing the analysis of the device characterization and may include the measured vs. simulated data.
11. PCM Structure & Test Report - The document (if separate or if in a single design manual, which section) addressing the construction of the PCM and the measurements taken for the purpose of wafer acceptance.
12. Device Parasitic Methods - The document (if separate or if in a single design manual, which section) addressing the methodology of extracting parasitic capacitance, resistance and inductance. It accounts for the difference between the intentional device and the extracted device, and the parasitic elements within the device model and outside of the device model to be accounted in the interconnect model for parasitic extraction software.

Section 3 - Circuit Simulators

This section states the circuit simulators supported and verified for use with the model. Other versions of simulators may or may not operate correctly with the model. The Checklist assumes that the simulators operate the same on all hardware platforms if the software version has the same version number.

1. Type – The foundry name for the class of simulator (e.g., circuit simulator, RF simulator, HB simulator).
2. Vendor and Tool – The known product name for the simulator (e.g., Agilent ADS, Cadence Spectre, Silvaco SmartSpice, Synopsys HSPICE).
3. Level Support – Full support, full support with exceptions or some defined subset of support with a note below if necessary.
4. Version – Many EDA vendors use a version numbering system for their products and product platforms.
5. Version Date – The release date of the simulation tool.

Section 4 - Model Classification, Noise, Matching, Statistical Variation, Results

The model classification section is designed to quickly give you an overview of the devices that are supported in the model set. Part of this information (a few columns) gets copied into the PDK Checklist that includes the model. The model classification section is sorted by the following device types, although specialty devices can be included, such as photo diodes, photo transistors, heaters, SCR, LDMOS or other devices.

Device Type	Subtypes	Typical Attributes
MOS	NMOS, PMOS, Twin/Triple Well, DMOS, LDMOS	Voltage, Range of Lengths, Finger Width, Temperature, Max Frequency, Noise Figure
BJT	NPN, PNP, Lateral, Vertical	Voltage, Range of Sizes, Temperature, Max Frequency, Noise Figure
Diodes	N+/PW, P+/NW	
Capacitors	Poly-Poly, MIM, MOM, Tunnel, Hi-Q	2 Port S Parameters, Sizes of Samples, Empirical and Measured Rules, Resonant Frequency, Q
Resistors	N-diff, P-diff, N-well, Poly0, Poly1, PolyN, Fuse, Metal	2 Port S Parameters, Silicide, Range of Resistance, Sizes, Layers
Inductors	Spiral, Differential	2 Port S Parameters, Inductance, Turns, Size, Square, Octagonal, Size, Metal Width, Stacked, Balanced, Q
Varactors	MOS, Junction, Hyperabrupt	2 Port S Parameters, Range of Capacitances, Sizes, Bias Conditions

Device types are not standardized in the Checklist because of the wide variety of definitions for these devices. The columns in the device table help to judge the completeness of the model. A separate table (Section 5) includes the device-specific types of parameters. The format of the entry is listed and can either be a list (coded words/letters to denote choice of predefined terms as a simple list as in Model Type, or a two dimensional quality as in Statistical Model); a number (#, or #.#); a name (model name/file name); a measurement unit (um, V, A, etc.); or a simple Yes/No (Y/N). The term “[same as PDK]” means this column can be copied directly into the PDK Checklist with the same meaning. The meanings of the columns are as follows:

Model Identification

1. Device Type (list) – See table above. [same as PDK]
2. Device Name (name) – The foundry-defined unique name that invokes the schematic symbol in the PDK, the model card in simulation and the correct Pcell in layout.
3. Model Name (name) – Name of the model card and individual model file if models are not combined into a single library.
4. Model Type (name) – (e.g., BSIM3, BSIM4, EKV, HICUM, GP) A separate chart will be developed and attached to this user manual that will have a matrix of the model level as it is defined in different commercial simulators (e.g., 1, 2, 3, 28, 49, 53).
5. Version (#.#) – (e.g., 3.2, 3.3, 4.4) If the model version references a Verilog-A model that is translated to “C”, include the version of the translator program (e.g., ADMS) used in the comment field, as the translator version can affect the performance of the model and is required here for traceability and version control.
6. Model Style (same as the PDK Checklist column Spice Model) – Means the model is either a C=compact model, B=behavioral model or S= Subcircuit Model.
7. Comments (#)– A reference to a comment field to be found after the device table. Comments can be used for explanations, exceptions or limits of the model. A typical use of this field is to use one row to describe many sizes of discrete (not scalable) devices (e.g., bipolar transistor) that are extracted and modeled in the same manner. [same as PDK]

8. Terminals (#) – Defines the number of terminals on the device. [same as PDK]

General Model Capabilities

9. No of Bins (#) – (e.g., 1, 2, 3, 4, 5 for number of model cards to cover device's full operating range through automatic binning of W, L) Measure of continuity.
10. 1/f Noise (list) – Means the SPICE model was characterized for what is called 1/f, flicker or low-frequency noise by the following methods: M=measured, T=TCAD, E=estimated or blank if not included. If the model is physically measured or TCAD-simulated for noise, then the Noise Model section of the foundry documentation must include the measurement methodology and the noise spectrum density vs. frequency range data. If estimated, that section will contain the applicable assumptions and equations. [same as PDK]
11. HF Noise (list) – Means the SPICE model was characterized for what is called high-frequency or RF noise (M=Measured, T=TCAD, E=Estimated or blank if not included) in the gigahertz range. As the device approaches its limits of operation, the frequency-independent thermal and shot noise (the Noise Floor) dominate due to thermal agitation, collisions and particles moving through energy barriers. The same measurement/estimation requirements of 1/f noise apply to HF noise. [same as PDK]
12. RF Parameters (list) – Means the SPICE model includes any number of the following extracted RF parameters that were verified as per the model documentation: Y=Y-parameters, S=S-parameters, N=NF or noise figure, F=FT or transition frequency, and L=NLE or non-linear effects. If it is not clear in the model documentation table of contents where this information is located, a comment field will point the reader to the appropriate section.
13. High Voltage (list) – Means the model was extracted and characterized for high-voltage applications and includes any number of the following parameters that were verified as per the model documentation: H=self-heating, B=breakdown, S=safe operating area and P=pulsed measurements.

Statistical Model Parameters

14. Statistical Model (list) – Summarizes the SPICE model included for the device (S=statistical Monte Carlo models have been extracted and verified, M=match models documented in matching models document, and C=corner models (four (FF,SS,FS,SF) corners are included)). If the character is upper case (S, M or C), the models are based upon directly measured silicon and the foundry documentation specifies the correlation (e.g., fab-to-fab, lot-to-lot, wafer-to-wafer, die-to-die and/or device-to-device). If the character is lower case (s, m, or c), the model is preliminary based on extrapolated data or from TCAD simulations, and the foundry documentation specifies their source and derivation. [same as PDK]
15. Statistical Method (list) – Describes the method(s) used for the generation of statistical models (C=PCA or primary component analysis, P=PFA or primary factor analysis, B=BPV or backward propagation of variance by Colin McAndrew). Foundries may use a combination of these methods.
16. Samples/Lots (#/#) – A two part number; the first part is the number of sample die that were used to generate the statistical model, and the second part after the "/" is the total number of lots from which those sample die were taken. There is no mandated distribution of those die over the lots, but model users may assume that it is random and reflects the process distribution.

Model Validation Metrics

17. Model Validation (list) – Means the model validation procedures are performed (P = procedure for model validation is described in the model documentation and R = results of the model validation procedure for this device are published in the model documentation). The current thought is that the guidelines for performing these procedures would be in a series of new documents (yet to be specified) that are similar to the 1995 GSA MOS Model Validation Procedure.

18. Corner Validation (list) – Means the corner validation procedures are performed (P = procedure for corner validation is described in the model documentation and R = results of the corner validation procedure for this device are published in the model documentation). Corner validation includes tables or graphs that show how the statistical model corners correlate to the published PCM specification for the process.
19. Max Error (list) – Means the maximum error of simulated vs. measured plots (P = procedure for error calculation is described in the model documentation and R = results of the error calculation for this device are published in the model documentation). Maximum error is the absolute percentage or RMS percentage (as defined in the model documentation) that is acceptable for each type of plot for the device.
20. Number of plots (#) – Means the number of simulated vs. measured plots are included for this device in documentation. These plots may include DC plots, AC plots, RF plots, S-parameter, Y-parameter, W elements and ring oscillator performance.

The following chart should be included in each checklist in section 4 to help readers decode the abbreviations. Foundries may choose not to list irrelevant parameters that are not used in a particular process (e.g., RF parameters in a high-voltage process for power management).

Model Style:	S	Subcircuit Model
	B	Behavioral Model
	C	Compact Model
1/f Noise, HF Noise:	M	Measured
	T	TCAD
	E	Estimated
RF Parameters:	Y	Y-Parameters Included
	S	S-Parameters Included
	N	NF or Noise Figure Included
	F	FT or Transition Frequency Numbers Included
	L	Non-Linear Effects
HV Parameters:	H	Self Heating
	B	Breakdown
	S	Safe Operating Area
	P	Pulsed Measurements
Stat Model:	S	Statistical Parameters Available
	C	Process Corner Models Available
	M	Matching Parameters Available
Model Val:	P	Procedures of Model Validation Available
	R	Results of Model Validation Available

Section 5 - Active Device-Specific Parameters

Separate tables are generated to cover the extraction conditions of the devices used to extract the models, grouped by specific device types. Each would start with the device type, device name, model name and number of geometries for reference. Some method to state the range over which the devices were extracted and the resulting models are interpolations as opposed to extrapolations. Other nomenclature was short, narrow, large, square, etc. The goal of this section will be to measure how scalable the models are with respect to geometry and bias. The tables are broken up into MOS, bipolar (Section 5) and passive (Section 6) so each can have a different number of columns. The passives could be further divided into diode, varactor, inductor, capacitor and resistor. For high-voltage processes, an optional parameter “Op Voltage” may be added for MOS, BJT or passives to help in visually sorting the devices. Op voltage is defined as the maximum recommended applied voltage to the device (e.g.,VDS for MOS or VCE for bipolar). The following parameters are standard in the Checklist:

MOS Specific Parameters

1. Duplicate device type, device name and model name for continuity.
2. Geometries (#) – 10 devices with various W and L.
3. Min Width (um) – Transistor width.
4. Max Width (um) – Transistor width.
5. Min Length (um) – Transistor length.
6. Max Length (um) – Transistor length.
7. Max Fingers (#) – Number of fingers that can be used with M factor.
8. Min Temperature (Degree C) – Extracted temperature.
9. Max Temperature (Degree C) – Extracted temperature.
10. Max Frequency (GHz) – Maximum frequency used for measurement.
11. Op Voltage (V) - Maximum recommended applied voltage to the device.

BJT Specific Parameters

1. Duplicate device type, device name and model name for continuity.
2. Geometries (#) – 10 devices with various W and L.
3. Min Emitter Width (um) – Transistor width.
4. Max Emitter Width (um) – Transistor width.
5. Min Emitter Length (um) – Transistor length.
6. Max Emitter Length (um) – Transistor length.
7. Max Config – Some code TBD for number of configurations of emitters, collectors and bases of the transistor.
8. Min Temperature (Degree C) – Extracted temperature.
9. Max Temperature (Degree C) – Extracted temperature.
10. Max Frequency (GHz) – Maximum frequency used for measurement.
12. Op Voltage (V) - Maximum recommended applied voltage to the device.

JFET Specific Parameters – Same as MOS

Section 6 – Passive Device-Specific Parameters

Diode, Varactor, Inductor, Capacitor and Resistor

1. Duplicate device type, device name and model name for continuity
2. Min Width (um)
3. Max Width (um)
4. Min Length (um)
5. Max Length (um)
6. Min Temperature (Degree C) – Extracted temperature.
7. Max Temperature (Degree C) – Extracted temperature.
8. Max Frequency (GHz) – Maximum frequency used for measurement.
9. Op Voltage (V) - Maximum recommended applied voltage to the device.

Guidelines for Model Validation Procedures and Corner Validation Procedures

Foundry model validation procedures should be included in the foundry modeling documentation. The following MOS Model Validation Procedure is an updated version of the GSA Modeling Subcommittee's 1995 document. This guideline is intended to educate model consumers using consistent terminology about the capabilities and limits of SPICE models used for selected applications (digital, analog/mixed-mode, RF and high voltage). It will be the foundation for Phase 2 of the GSA SPICE Model Checklist that will include model validation for MOS, BJT, capacitor, resistor, varactor and inductor. Corner validation methods will also be addressed. It is anticipated that this Phase 2 Checklist will be complete in October of 2005. Items to be addressed include:

1. Model Validation should be divided into regions (sub-threshold, linear and saturation) for different device types (MOS, BJT, etc.) for recommended sweeps. Sweeps would be

application-specific for processes targeted to digital only (Ids, capacitances, leakage); analog/mixed-mode (Gm/Gds linearity, 1st derivative, etc.); RF (FT, Fmax, NF, etc.); and high voltage (IDS/VDSmax, IDS/VGSmax at bias conditions). Validation includes continuity checks, physical trend checks, capacitance checks, resistance checks, temperature checks, frequency checks and speed checks (ring oscillators).

2. Corner validation will be a correlation of the corner model results for a specific device at a set of specific geometries (e.g., Lmin/Wmax) to the process specification in terms of sigma, mean, etc. for some defined set of process variables. Selected variables may be application specific such as digital (TOX, VTH0, etc.), analog/mixed-mode (Gm, Gds, Rout, etc.), RF (capacitances) and high voltage (Ron, Rd, Rsh, etc.).

MOS Model Validation Procedure

The MOS model validation procedure includes checks of the DC and AC parameters of the extracted model, checks for the process corner models, general checks by simulation of benchmark circuits and checks by comparison with measured data.

STEP 1 – DC Fit of Extracted Models with Measured vs. Simulated Plots

Check DC fit of the extracted models using simulated vs. measured data plots for a combination of long and short channel and narrow and wide width transistor geometries. Check fit on plots done using three or more different temperatures (e.g., -55C, 25C and 125C). Plots must show signed absolute maximum and RMS errors. Obtain scans and do following checks with modifications specified for each model application (digital, analog, RF or high voltage).

Parameter VLO is used in the scans specified below. Accurate CMOS modeling requires decreasing VLO as VDD scales down with technology. If VDD > 3.3V use VLO = 0.1V, If VDD < = 3.3V use VLO = 0.05V. Parameter VT* is a number near VT of the specific geometry device at the specified temperature.

If model is to be qualified for **digital** applications, the following steps/scans or near equivalents must be checked:

1.1 ID vs VGS linear curves at |VDS| = VLO, |VBS| = 0 V,VDD/4, VDD/2, 3/4VDD and VDD
1.2 Log ID vs VGS subthreshold curves at |VDS| = VLO, |VBS| = 0V, VDD/4, VDD/2, 3/4VDD and VDD
1.3 Log ID vs VGS subthreshold curves at |VBS| = 0V, |VDS| = VLO, VDD/2, VDD)
1.4 ID vs VDS saturation curves at |VBS| = 0 and VDD/2, |VGS| = VT*+VLO, VDD/4, VDD/2, 3/4VDD and VDD.

If model is to be qualified for **analog, RF or high-voltage** applications, the following additional steps/scans or near equivalents must be checked:

1.5 ID vs VDS at |VGS| = VT* and VT*+VLO, at |VBS| = 0V
1.6 Log gds vs VDS, at |VBS| = 0V, |VGS| = VLO, VT*, VDD/2 and VDD.
1.7 gm vs VGS, at |VDS| = VLO, VT*, VDD/2 and VDD, |VBS| = 0V, VDD/2 and VDD)
1.8 gmb vs VBS, at |VGS| = 0 V, VT*, VDD/2 and VDD, |VDS| = 0V, VLO, VDD/2 and VDD

RMS and Maximum error results of the curve fits beyond the following limits should be noted as exceptions with explanations in the model documentation:

Error Tolerance	**Range**
R.M.S. error of the ID vs VDS or VGS in linear or saturation region	< 5%
Max error of the ID vs VDS or VGS in linear or saturation region	+/- 10%
R.M.S error of the ID vs VDS or VGS in subthreshold	+/- 15%

Negative resistance over VGS range for each scan and temperature	0

STEP 2 - Check Continuity of all DC Models with Simulation Only

2.1 Sanity Check of TYPICAL and all CORNER Models

Publish a plot of ID versus VDS and ID versus VGS curves that cover each of the model selector regions over temperature extremes. For example, four model regions, three temperatures and four model corners will produce 48 plots. These plots must be visually checked for discontinuity, negative resistance (especially at VGS = VTH) or other non-physical behavior. If the elimination of the non-physical behaviors is not possible due to model limitations, the data for the abnormal behavior should be provided to users as a warning.

2.2. Model Selector Continuity Check

Plot ID vs Leff and ID vs Weff for the entire range of L's and W's, and temperatures (-55C to 125C). This is done separately for linear and saturation regions. Special attention should be paid to the scale of the plots as too large a scale may not provide enough resolution to show the discontinuities. There should be smooth transition from one model region to the next. In the case of models for analog applications, smooth transition from linear to saturation region is desired. No kinks or discontinuity should be observed.

2.3. Drain Current Trend

Publish table of values for drain saturation current, for example ID at VDS = VGS = VDD, for each model corner, several typical transistor sizes (short, narrow, square, and small) and three temperatures: cold, room and hot. Verify that process and temperature variations have proper effect on the transistor current. Repeat the same simulations for IDlinear (e.g., ID at VDS = VLO, VGS near VTH). Correct trend should be observed from fast to slow corners.

2.4. Gm/ID vs VGS Check

Simulate gm/ID versus VGS (or log ID) for various geometries. The plot will clearly show kinks or discontinuities, if any, in the moderate inversion region. This simulation should be done for all model separations.

2.5. Subthreshold Leakage Check

Simulate and review drain current of very large W transistor with minimum L, biased into subthreshold region. Check the worst-case conditions: high voltage, fast corner model and hot conditions, e.g., W/L = 20/0.18, VDS = 3.3V, VGS = 0V and 0.25V. Verify that the model does not produce excessive subthreshold leakage.

STEP 3 - AC Model Check

3.1. Junction Capacitance

Publish overlaying plots of the simulated and measured diffusion capacitance for the junction bottom, field oxide edge and poly gate edge.

3.2. Gate Capacitance

Publish table comparing values of the electrically measured gate oxide thickness with those measured in the fab. The value of the actual gate oxide thickness of the modeled silicon should match with TOX used in the model, to prevent superficial parameter changes in model parameters such as mobility, VTH etc., due to incorrect TOX values.

3.3. Interconnect Capacitances

Publish table showing extracted or simulated interconnect capacitances, including fringing and coupling components.

3.4. Gate Overlap Capacitances

Publish the assumptions for the calculation or simulation of the gate overlap capacitance values.

3.5. Resistor Models

Publish table of sheet resistances for N+, P+, Poly (N+ and P+ doped, Salicided, if applicable), load resistor, metal and well resistors, especially for analog processes. The resistor models should include the sheet resistances, width effects, temperature coefficients, contact resistance effects (if significant) and parasitic capacitances. The information on the specific resistor geometries used in the extraction of model parameters should also be provided.

STEP 4 - AC/DC Model check

4.1. Speed

Publish table to summarize simulated of propagation delay for a few standardized circuits, such as ring oscillators and delay chains with various loads. Compare these delays with simulated results for the previous generation of process, for example 0.13um process vs. 0.18um process. Appropriate scale factor must be used for simulations of the same circuits with previous generation process. As an example, the following simulation conditions may be used:

Corner	Temperature	VDD
NOMINAL	27C	VDD= 3.3 V (VDD)
SLOW	125C	VDD= 2.5 V (VDD – n%)
FAST	-55C	VDD= 4.0 V (VDD + n%)

4.2. Input Level

Publish table to check switching threshold, VIH, VIL, for typical input buffer circuits over all models and temperatures.

Feedback on the GSA Mixed-Signal/RF SPICE Model Checklist

Please send any feedback on the usability and clarity of the Mixed-Signal/RF SPICE Model Checklist, Users Guide, and Taxonomy and Definitions to the GSA Mixed-Signal/RF Modeling Working Group at roberto_tinti@agilent.com or cboone@fsa.org.

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