Physical IP Development On FinFET
– There’s Nothing Planar About It!

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Physical IP

- Logic libraries
- Embedded SRAMS
- Interface IP
  - USB PHY
  - DDR PHY
  - PCI Express PHY
  - HDMI PHY
  - MIPI PHY
  - SERDES

Acronyms

- DIBL = Drain Induced Barrier Lowering
- EM = Electromigration
- SCE = Short Channel Effects
- RDR = Restricted Design Rules
- DPT = Double Patterning Technology
- NBTI / PBTI = Negative (Positive) Bias Temperature Instability
- PODE = Poly Over Diffusion Edge
- PDK = Process Design Kit
**PPA = Power, Performance, Area**
Power, performance & area must be met **regardless** of the semiconductor technology
Agenda

Introducing FinFET Devices
FinFETs On Physical IP
New Design Methodology
Summary
**FinFET Transistor Characteristics**

*Output Curves: Voltage (V), Current (I)*

Control through:
- Gate length
- Number of Fins
**FinFET Advantages & Considerations**

*Improved Characteristics; Impacts Circuit Design*

**Advantages**
- Lower leakage
- Less variability
- Lower voltage
FinFET Advantages & Considerations

*Improved Characteristics; Impacts Circuit Design*

**Considerations**
- Quantized widths
- No body biasing
- Higher parasitics
- Aging
Key Points – FinFET Technology

- Better control of short channel effects
- Improves gate control to suppress leakage current
- Reduces process-induced variability below 32-nm

FinFET technology is now in production
Agenda

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- Design Methodology
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FinFET Impact On Physical IP

*High level view…*

**Physical IP**

- Logic libraries
- Embedded SRAMS
- Interface IP

DPT impacts M2/M3
→ Routing

FinFET impact below M1
→ Circuit optimization
FinFET Logic Libraries → Highlights

• Faster than planar; lower leakage & dynamic power
  – Lower leakage enables lower $V_{TH}$
  – Lower $V_{TH}$ enables lower $V_{DD}$
  – Lower $V_{DD}$ leads to lower dynamic power: $P_d = fCV^2$

• Higher drive for same silicon area
  – Effective transistor width of 9T FinFET cell is close to 12T planar cell
FinFET Challenges

In Logic Libraries

• ‘Quantized width’ challenge
• Lonely FinFETs
  → Degrade performance
  → Increase variability
• EM a concern at chip level
• Further challenges:
  → Layout compaction
  → Routability

Lonely FinFET is not stressed
Driving current drops
New Design Styles

*In Logic Libraries*

- Cell height / width multiple of Fin /gate pitch
- Power rail width and layout dictated by special rules
- DPT rules prevent use of M1 at the chip level
- PODE addresses lonely FinFET effect
FinFET SRAMs → Highlights

- Higher performance, lower leakage
- Good static noise margin at low Vdd
- Operates at lower Vdd
FinFET SRAMS $\rightarrow$ Challenges

**Body Effect**

- $V_{th0} = 0.35 \text{ V}$
- $T_{ox} = 1.5 \text{ nm}$
- $L_g = 50 \text{ nm}$
- $V_{DS} = 0.05 \text{ V}$
- $H_g = 100 \text{ nm}$
- $W_{fin} = 20 \text{ nm}$
- $\Phi_m = 4.51 \text{ eV}$
- $\Phi_m = 4.33 \text{ eV}$

**Quantization**

- Static noise margin or bigger bitcell
- Write margin issues

Source: Jong-Ho Lee Seoul National University Thesis
Solutions: Read/Write Assist Schemes

In Embedded SRAMS

Prashant Dubey et. al., “A 500mV to 1.0V 128Kb SRAM in Sub 20nm Bulk-FinFET using auto-adjustable write assist”, 27th IEEE International VLSI Design Conf. 2014
Detect Defects In FinFET Transistors

In Embedded SRAMs

Resistive shorts between Fins

Resistive opens on Fins

Step 1. Defect injection & fault modeling
Step 2. Test sequence & optimal PVT
Step 3. Test algorithm synthesis
Step 4. FinFET Enhanced SMS 5*

New addressing mechanisms
Fully programmable background patterns
Programmable test operations
Stress conditions

*Synopsys Star Memory System
Impact On Circuit Schematics

Interface IP

• Key parameters: $g_m$, $g_d$, $F_t$, $F_{\text{max}}$, matching, noise
• PMOS/NMOS drive strength
• Device matching better
• W/L mapped to L and # fins
• New designs needed for high speed blocks
• Aging simulation is important

$g_m/g_{ds}$ of bulk and FinFET
Impact On Layout

Interface IP

- Smaller devices get hot
- New tools for EM and IR
- High speed divider causes self heating
- DRC complex
- Metal stack has impact
- Need full RCC simulations
Key Points – FinFETs on Physical IP

Logic Libraries
- Short (7.5T) libraries will be key to achieving highest density, lowest power
- PODE addresses lonely FinFET effect

Embedded SRAMS
- New assist circuitry helps with low Vdd, body bias and $\beta$ quantization
- Synopsys developed flow to detect defects in FinFET cells

Interface IP
- Create optimized FinFET schematics by including process info. (inc. NBTI)
- Start layout earlier in the design process; new modeling in .lib files
- In order to meet PPA, new architectures to be developed
Agenda

Introducing FinFET Devices
FinFETs On Physical IP
Advanced Design Methodology
Summary
The Need → The Solution

**IP Specs**
- DDR4, LPDDR4 → Higher I/O speeds using single-ended interface
- USB 3.0 → Must support all 4 speeds
  → Meet electrical compliance
- PCI Express → 8 Gb/s but support new low power modes

**Market**
- Physical IP → Scales (area, power) without performance degradation
- Aggressive schedules → Supports design on an early PDK
- SOC → Works on first instantiation in SoC

The Solution: Advanced Silicon Design Methodology
Process Qualification Vehicle

Monitor / evaluate speed, leakage, parasitic R, C, random & systematic variability & lithography induced variability effects

- **Timing Structures**
  - Inverter, NAND and NOR Oscillators
  - Multiple capacitive & metal loads, multiple Vts
  - Preferred height, #fingers, P/N ratios, #fins

- **Power Structures (Vt/Channel)**
  → Chains of Inverter for dynamic & static power

- **Layout effects:**
  → Lonely FinFET, WPE, Endcap, Body Effect, NBTI/End of Life
CAD Flow

Example 1: Density Viewer

Actual Max density = 54.2%
Silicon Success: USB 2.0 PHY; 6 Gb/s SERDES

USB passed logo certification; FinFET designed for power, area

### Key USB Test Results

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<th>USB 2.0</th>
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<td>Pass</td>
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<tr>
<td>ATE Tests</td>
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<td>Functional</td>
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USB PHY

<table>
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<tr>
<th></th>
<th>28-nm</th>
<th>FinFET</th>
<th>% savings</th>
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<tbody>
<tr>
<td>2.0 Macro Area</td>
<td>0.38 mm²</td>
<td>0.19 mm²</td>
<td>50% ✓</td>
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<tr>
<td>2.0 HS Power</td>
<td>56 mW</td>
<td>46 mW</td>
<td>18% ✓</td>
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<tr>
<td>3.0 Macro Area</td>
<td>0.77 mm²</td>
<td>0.43 mm²</td>
<td>44% ✓</td>
</tr>
<tr>
<td>3.0 SS Power</td>
<td>84 mW</td>
<td>66 mW</td>
<td>21% ✓</td>
</tr>
</tbody>
</table>

Note: Specific area and power figures are process dependent.
Key Points – Design Methodology

In order to meet:

• Time-to-market requirements
• Early (changing) PDK
• Next protocol generation, improvement in PPA
• Silicon success on first instantiation in SoC

→ Investment in an advanced design methodology is paramount
Agenda

- Introducing FinFET Devices
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- Design Methodology

Summary
Summary

*There’s nothing planar about FinFET’s*

- **FinFET advantages** to Physical IP
  - Improved electrical and technology parameters yielding significant performance advantages
- **New design approaches** can handle limitations:
  - Assist circuits, high voltage tolerance
  - Redesign (when necessary) to meet PPA
- **Advanced design methodology** ensures silicon success on first instantiation
- **Synopsys provides silicon proven FinFET Physical IP**