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JCET Group at a Glance

**CHINA**
- Wirebond, flip chip, bumping
- MIS, SIP, FO-WLP (ECP), discretes

**SINGAPORE**
- Wafer Level Packaging, WLCSP,
- eWLP, eWLCSP, wirebond CSP

**KOREA**
- SIP, advanced Flip Chip,
- hybrid flip chip, memory

**Patents Issued by the US PTO**

<table>
<thead>
<tr>
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<th>JCET Group</th>
<th>Amkor</th>
<th>ASE</th>
<th>SPIL</th>
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*Source: Based on Patent Information Published in USPTO Website and State Intellectual Property Office of China*

**OSAT 3Q17 Revenue**

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</tbody>
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QoQ:
- ASE (ATM): +7%
- AMKOR: +15%
- JCET Group: +27%
- SPIL: +7%

*Source: Company ERs*
Fan-out Wafer Level Packaging (FOWLP)
FOWLP: Innovative Solution based on Wafer Process

- A Wafer Level Packaging technology utilizing well developed wafer bumping infrastructure, with an innovative wafer reconstitution process to package Known Good Die (KGD)
- Using proven materials and a simple structure

**eWLB/Fan-Out WLP**

- Fan-out Interconnects - #, Pitch of Interconnect is INDEPENDENT of chip size
- Single/Multi/3D chip packaging solution
- Improved Yield with KGD

FOWLP expands the application space for Wafer Level Packaging.
“Third wave” of ‘Fan-out Packaging’

1. **Wirebond**
   - Requires a substrate/leadframe
   - 2 interconnection interfaces
   - Strip-based format for processing (typically 70mm x 240mm)
   - x-out bad sites (waste materials)

2. **Flip Chip**
   - Requires a substrate
   - 1 interconnection interface
   - Strip-based format for processing (typically 70mm x 240mm),
   - x-out bad sites

3. **Fan-Out WLP**
   - No substrate
   - No interconnection interface
   - Reconstituted wafer (>12”) or panel (>500x600 mm)
   - Process only good die and no wasted sites

**Advantages of FOWLP:**
Elimination of the laminate and interface with minimized waste

- Total thickness reduced
- No interconnections result in improved reliability
- Significant cost savings
- Superior electrical and thermal performance by significant trace length reduction
Market TAM reach over 3B $ in 2022

STATS ChipPAC’s internal projections indicate even higher demand growth (OSAT industry capacity limited)

(Source: Yole, Adv PKG Report, June 2017)
## FOWLP Products in Mobile and Consumer Applications

- Baseband processors
- RF transceivers
- Power Management Integrated Circuits (PMIC)
- Connectivity
- 77GHz ADAS Radar for automotive
- mmWave-MMIC
- Near field Communication (NFC)
- Audio CODEC
- Security devices
- Microcontrollers (MCU)
- Memory
- NAND memory controllers
- Touchscreen controller
- RF-MEMS Tuner
- Bio/Medical devices
- Application processors (future)

### Sources:
- **TAP Times, September 2016, Vol. 7, No. 9**
- **NXP Radar Module**
  - Source: NXP
- **Qualcomm WCS 9336 Audio CODEC**
  - Source: System Plus Consulting
- **Intel Wireless Division LTE Analog Baseband 5.32x5.04x0.7mm eWLB 197 balls, 0.4mm pitch**
  - Source: TPSS
- **Marvell PMIC & Audio CODEC**
  - Source: Nanium/Marvell
- **Infineon mmWave IC BGT80**
  - Source: Infineon Technology
- **Infineon RRN7745P & RTN7735P eWLB Fan-out Package -77GHz Radar Dies @Bosch MRR1Plus Radar**
  - Source: System Consulting

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*Innovative Integration Solutions*
eWLB: the FOWLP Winner

- eWLB is chip first, die face down FO-WLP without bump and carrier handling
- Proven manufacturing with > 1.5B units shipped
- The smallest form factor fan-out package
- Solid supply chain supported by the Top 3 OSATs
- Enhanced performance for RF & mmWave (5G/Automotive)
- Integration – multi-Die, 3D PoP & SiP
- Cost effective solution with scalability (larger panel size)
- Independent from input wafer size and technology
- Flexibility to produce both fan-in and fan-out on the same production line
- Reliable ELK for advanced Si nodes devices

Solder ball
Cu-RDL
Si Chip
EMC

eWLB Line in STATS ChipPAC Singapore
Highly Flexible Technology Platform

- Many different package configurations with the basic eWLB FOWLP process
- Highly versatile solution platform relevant to many application spaces
- 2D, 2.5D and 3D integration delivers product advantages in terms of higher I/O and thinner profiles in a reliable, cost effective package
Integration Alternative to 2.5D TSV

Flip Chip eWLB

- TSV interposer replaced by multi-layer/fine pitch RLD in eWLB FOWLP
- Extend bump pitch design by eWLB RDL from 40-50um to 80-150um
- Enhanced flip chip bump reliability of advanced node device (7/10nm) with stress compliance of RDL in eWLB
- The most cost effective solution as well as simple supply chain model for multi-die integration

Die-pad pitch: as small as 40um (staggered)
Flip Chip bump pitch: 80um-150um
Interposer: to fan-out small die-pad pitch to large enough ball-pitch for flip-chip assembly
Antenna in Package for mmWave

- Cu trace roughness: 0.3um
- Manufacturing/etch tolerance (L/S): tight (1-2um)

- Cu Trace roughness: 3um
- Manufacturing/etch tolerance (L/S): moderate (5-10um)
System in Package (SIP)
Drivers for SIP/ System Integration

- SiP Definition: *Two or more dissimilar dies PLUS passives in one package*
- Heterogeneous integration for optimized system solutions
- Enables differentiation & specialization

SiP / Module

- Miniaturization
- Higher performance
- Heterogeneous integration
- Si partitioning in advanced nodes
- Customization, platform re-usability & re-configurability
- Modularization – Final assembly simplification
- Design flexibility & Time-to-market
- Lower system level cost
SiP Unit Growth at 5-6% CAGR
32.8B units in 2016 → 42.5B units in 2021

2016 SiP units by Application

- MEMS and Controller SiP: 10 Bu (30%)
- Memory SiP: 7.5 Bu (23%)
- Camera Module: 4.2 Bu (13%)
- PA-centric RF SiP: 4.7 Bu (14%)
- Connectivity SiP: 0.9 Bu (3%)
- PoP: 0.8 Bu (2%)
- Fingerprint Sensor: 0.8 Bu (2%)
- Display Touch Module: 0.2 Bu (1%)
- CPU/GPU/ASIC MCP: 0.2 Bu (1%)

SiP:
Two or more dissimilar die assembled into a standard package; can include MEMS, sensors, passives, filters, antennas; forms a functional block

Source: TechSearch
### SiP and Applications (1/2)

<table>
<thead>
<tr>
<th>SiP Package Types</th>
<th>Features</th>
<th>Target Applications</th>
</tr>
</thead>
</table>
| **Stacked Die SiP**   | • LGA/BGA  
• Thin Stacked Die  
• Passives                                                           | • SSD (Removable & Embedded)  
• Memory modules  
• BB/AP Processors                                              |
| **fcBGA-SiP**         | • SMT Module  
• with/without H/S  
• Large body                                                      | • Hardware platform module  
• Automotive  
• Networking                                                     |
| **BGA/LGA –SiP**      | • Bare Die (FC/WB) +SMT  
• Coreless or cored substrates  
• Embedded die  
• IPD, Filter  
• Single sided/double sided  
• Conformal/compartmental Shielding                               | • RF FEM  
• Controller Modules  
• WiFi  
• Connectivity                                                    |
## SiP and Applications (2/2)

<table>
<thead>
<tr>
<th><strong>SiP Package Types</strong></th>
<th><strong>Features</strong></th>
<th><strong>Target Applications</strong></th>
</tr>
</thead>
</table>
| **AIP-SIP**           | • Embedded antenna  
                      | • Discrete antenna  
                      | • POP antenna  
                      | • mmWave and 5G  
                      | • Networking/mobile  |
| **eWLB SiP**          | • Multi-die embedded  
                      | • Multi-layer RDL (1-3L)  
                      | • Passives Integration  
                      | • Inductor with RDL for higher Q  
                      | • Connectivity  
                      | • RF, PMIC module  
                      | • RF MEMS  
                      | • mmWave /radar  |
| **Leadframe SIP**     | • QFN or bare die + passives on leadframe  
                      | • Molded  
                      | • Power modules  |
| **Specialty SIP**     | • ASIC/MCU + MEMS sensor  
                      | • IR transparent molding/shielding  
                      | • Optical isolation  
                      | • Fitness monitoring/WE  
                      | • Automotive LIDAR  |
Summary

1. eWLB is the best approach of FO packages for its cost effectiveness, supply chain readiness and manufacturing maturity as well as extendable platform.

2. Product miniaturization and the modularization of functionality is accelerating growth in system level integration (SiP).

3. Increasing I/O density and complex integration requirements in a smaller form factor are leading to a wide range of 2.5D and 3D SiP FOWLP solutions.