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The unique strategy of outsourcing—the act of engaging external resources to accomplish certain goals—has been increasingly used by managers of successful corporations. There are two scenarios that push companies towards outsourcing. First, as an industry matures, there is the natural growth of a support ecosystem, and product manufacturers depend more and more on this ecosystem to stay competitive. Secondly, companies tend to build their internal resources at a rapid pace during strong business growth, and then go through the unwanted and painful process of reduction in force during slow times.

The semiconductor industry has seen these two scenarios play out over the last three decades, further contributing to the maturation process. It has experienced exuberant growth of the worldwide “supplier” ecosystem. By establishing themselves as strong core competency centers, suppliers have enforced an increasing dependence of the product supplier on this ecosystem. The semiconductor industry has also gone through several economic cycles of successive boom and bust. All these events have made semiconductor companies more dependent on outsourcing for critical resources and core competencies.

Each economic slowdown has opened the door for a new, critical part of the business process to be outsourced by semiconductor companies. It first started with integrated, vertical companies having everything under one roof. During the first major downturn, the notion of outsourcing wafer processing to a pure-play foundry to augment capacity took shape. Even industry leaders who publicly proclaimed “real men have fabs” started using foundries to manage the cyclical nature of their business. It is easy to forget how resistant the industry was to outsourcing the most critical step in manufacturing—wafer processing. But in time, newly established semiconductor companies did not even plan to build or own any fabs, thus giving birth to the fabless era.

The development of electronic design automation (EDA) tools then gave rise to a new group of design service companies. Initially, semiconductor companies outsourced only segments of their design flow activities such as place and routing. But during the next downturn, design service companies became an integral part of semiconductor companies’ product design flows, and, eventually, critical intellectual property (IP) and block design activities were outsourced.

Some current-generation fabless companies have started outsourcing the entire process: design, productization and manufacturing. These companies market their products and hold ownership of their products’ IP, and the actual design and manufacture of product is outsourced. However, many executives are still reluctant towards outsourcing for fear they will lose control if they do not keep these operations in-house.

Business dynamics in the fabless sector have changed drastically in recent years and have become even more daunting during the current economic downturn. Gone are the days when the venture capital community created strong investment momentum for semiconductor start-ups and the rate of initial public offerings (IPOs) was high, giving investors excellent returns. Now, investment in semiconductor start-ups is much more limited, and market environments are not encouraging to IPOs. Most of the recent exits have been via acquisitions/mergers.

In this business environment, it is extremely critical to keep fixed costs low and use variable cost structures wherever possible—especially for functions that do not directly contribute to a company’s core competency. It is important to understand that similar to the industry’s adaptation of the fabless business model, which allowed companies to become more cost-effective and competitive during previous downturns, a similar adaptation of an extreme fabless business model (without a fab and a full in-house operation team) would make companies even more cost-effective and competitive during the current downturn.
During the early stages of product development, operations personnel are not fully utilized, yet their expertise and experience are needed in making critical product planning and product definition decisions. Even during productization (post-design) the utilization of these personnel is low. Only after the product is successfully launched into high-volume manufacturing are operations personnel fully utilized. Many companies carry a fixed cost structure for a long period of time by building an in-house operations team, and add to their burn rate before getting actual market traction. This situation is not deemed suitable for the current environment wherein the most likely exit strategy is via an acquisition/merger. In most cases, operations personnel are stripped following an acquisition/merger as they do not contribute to the acquiring company’s core competency.

The sentiment of losing control when outsourcing product development and manufacturing should be examined in the same light as past sentiments held about foundries. The adaptation of the foundry by a semiconductor company was one of the most important turning points in the industry. It allowed for the proliferation of solution providers without having to carry the enormous financial burden of owning a fab. The continuous growth of the semiconductor industry over the last two decades would not have been possible without foundries. There are several hundred fabless companies worldwide supported by only a few foundries, thereby making it an extremely efficient and successful business model.

Outsourcing packaging and testing services, as well as important services provided by analytical labs, is now standard. The outsourcing trend can also extend to outsourcing product development and manufacturing to an external “operations contractor” who delivers a company’s products by leveraging the supplier world. The right operations contractor can reduce costs and increase a semiconductor company’s chance of success.

**Selection of an Operations Contractor**

Outsourcing IC development and manufacturing to an operations contractor is actually not new, as illustrated by the application-specific IC (ASIC) industry. The ASIC business model was designed to serve the systems industry. Systems companies build their system products utilizing standard and custom ICs. As they tend to not have in-house resources (as it is not their core competency), they outsource the development and manufacture of their custom ICs. Large integrated device manufacturers (IDMs) (e.g., Philips, STMicroelectronics, Fujitsu and IBM) offered these services as they had the development and manufacturing resources, and, more importantly, they had their own fabs to fill. In the ASIC business model, a supplier sells ICs at a unit price that includes manufacturing costs as well as margins. From the systems companies’ point of view, it is still cost-effective because they get their margins from the total systems they sell to their own markets.

The ASIC business model has now been applied to serve the fabless industry. Fabless ASIC suppliers do not own fabs and apply the fabless business model to provide ASIC services to fabless companies. And some new fabless ASIC companies have outsourced product development and manufacturing to fabless ASIC companies for the last few years. Mirroring their predecessors, these fabless ASIC companies also sell units to their semiconductor customers at a price that includes manufacturing costs and some margins. This is not the most cost-effective option for the fabless customer as they themselves resell the same product to their customers and must give a good portion of their own margin to its ASIC supplier.

A new business model is now emerging in which a semiconductor operations contractor offers the same services using a customer-owned tooling (COT) approach wherein semiconductor customers can procure their products at the raw cost of manufacturing. The contractor is paid a service fee for managing product development and manufacturing. The fee is much lower than it would be if development and manufacturing was managed with internal resource build-up. This is particularly more cost-effective in the early stages of a start-up or in the early stages of product development at a more established company. Furthermore, companies can preserve the margins they demand in the markets they serve.

This new approach seems to be in demand during this period of economic slowdown as it allows semiconductor companies to continue to do their product development at a much lower cost and keep it variable at the same time. It is also the desirable strategy for a potential acquisition/merger when economic conditions improve.

**Conclusion**

In summary, every economic downturn which has affected the semiconductor industry has given legitimacy to a new sector of services to be outsourced. The outsourcing of these services then gradually becomes the norm for semiconductor companies to remain cost-effective and competitive, and, in turn, feeds the sustained growth of the industry.

The current downturn has necessitated a serious look at outsourcing product development and manufacturing to an operations contractor. A COT-based outsourced model is preferred over the ASIC model for obvious financial reasons. A properly leveraged outsourcing operations strategy can better prepare an emerging company for the inevitable up-turn, and thus make it more attractive for an eventual merger/acquisition or IPO.

**About the Author**

Ron has 25 years of experience in the semiconductor industry in product development and silicon operations with both established, large companies and fabless start-ups. Prior to founding Siliconaire Inc., Ron was vice president of operations at Atheros Communications, a leader in the wireless local area network (WLAN) market. Ron joined Atheros at a very early stage and built a operations technical capability, infrastructure and strong relationship with suppliers to take the world’s first CMOS 802.11a radio frequency (RF) transceivers into high-volume manufacturing with perfect quality records. This helped in growing the company’s revenue rapidly from $0 to a $180 million per year run rate, leading to a successful IPO.

Before Atheros, Ron was vice president of operations at Newport Communications. As one of its first employees, Ron was responsible for developing the successful OC-192 SONET products into manufacturing volumes, leading to an acquisition of the company. Previously, Ron held director-level positions at Cirrus Logic and AMD. At Cirrus, Ron managed two operations joint ventures—one with IBM and the other with Lucent Technologies—among various other foundries to support the company’s $0.5 – $1.0B revenue. At AMD, Ron was responsible for outsourced operations, including a venture with Fujitsu supporting $400 million in revenue. Ron was also one of the key contributors in transitioning AMD from Bipolar to CMOS by developing several generations of products and technologies.

Ron has been very active in fabless industry panels and conferences. Ron’s leadership was acknowledged by industry peers by electing him to serve as a Board member of the Fabless Semiconductor Association (now Global Semiconductor Alliance) during 2001–2004. He holds a Ph.D. in electrical engineering from University of California, Santa Barbara, California. You can reach Ron Das at 408-524-2600.
Actel (NASDAQ: ACTL) released its free Mixed-Signal Power Manager (MPM). A reference design and graphical user interface (GUI) tool included in the recently announced Fusion Advanced Development Kit, MPM enables designers to control and reduce power at the system level, offering fully-verified, timing-closed, proven-in-hardware power supervision and management capabilities. This latest offering highlights the significant integration benefits of Actel’s Fusion device, the industry’s first mixed-signal field-programmable gate array (FPGA).

Bringing its acclaimed 45nm technology to new high-volume processor designs, Advanced Micro Devices (NYSE: AMD) released two new dual-core desktop processors. Building on 10 years of AMD Athlon™ processor innovation, the new 45nm AMD Athlon™ II X2 250 processor gives mainstream consumers exceptional performance, efficiency and value.

Alereon demonstrated an Apple iPhone/iPod peripheral reference design based on its new worldwide, low-power 90nm-LP AL5301 chip built at Samsung’s 12-inch wafer fabrication facility in Korea.

Analog Devices (NYSE: ADI) introduced the industry’s smallest four-channel digital isolators. Housed in a small 5mm x 6mm quarter-size small outline package (QSOP), ADI’s ADuM744x digital isolators can isolate four channels of data and power while reducing board space up to 70 percent and cutting costs by 20 percent.

Broadcom (NASDAQ: BRCM) will introduce a new family of gigabit passive optical network (GPON) integrated access device (IAD) semiconductors to telecommunications providers and original equipment manufacturers (OEMs) in China this year. The Broadcom BCM6800 family of GPON gateway processors is designed to enable more cost-effective optical network terminals (ONTs) or optical network units (ONUs) used in conjunction with service provider networks.

BroadLogic Network Technologies released the TeraQAM BL85000, the industry’s first ultra-dense quadrature amplitude modulation (QAM) chip for systems that transport video, voice and amplitude modulation (QAM) chip. The XR21V1410/V1412/V1414 have differentiated features which include the smallest packaging options and optimized software drivers, and support large first in, first out (FIFO) sizes delivering flexible and proven design options to system architects.

Fresco Microchip added FM1050, a worldwide legacy audio/video demodulator for cable and terrestrial broadcast television reception to its line of breakthrough solutions. The new FM1050 provides optimum flexibility with universal support for National Television System Committee (NTSC), Phase Alternating Line (PAL) and Sequential Color with Memory (SECAM) analog broadcast standards. The new demodulator addresses the strong demand for analog-only television in Asia, including China and India, as well as many parts of Eastern Europe.

Leveraging its high-speed serial interface and digital systems expertise, Gennum’s (TSX: GND) Snow Bush intellectual property (IP) group has developed the industry’s first available integrated PCI Express™ (PCIe) 3.0 physical layer (PHY) and controller IP solution. The new PCIe 3.0 cores can be licensed immediately by SOC and system companies, enabling early deployment of PCIe 3.0 in systems requiring the 8.0 GT/s performance of this new Peripheral Component Interconnect-Special Interest Group (PCI-SIG) standard.

One of Himax Technologies’ (NASDAQ: HIMX) liquid-crystal-on-silicon (LCOS) microdisplays, HX7027, received the 2009 Outstanding Photonics Product Award by the Photonics Industry and Technology Development Association (PIDA). The HX7027 is a color-filter LCOS microdisplay with video graphics array (VGA) resolution (640x480) developed by Himax Display.

IBM (NYSE: IBM) introduced new systems software for managing virtualized servers, designed to help clients plan, build and maintain data centers while reducing costs. IBM is also helping clients protect their long-term investments in Power Systems™ by announcing an upgraded path to its next-generation servers that will include POWER7 microprocessors.

Intel (NASDAQ: INTC) is moving to a more advanced 32nm manufacturing process for its leading NAND Flash-based solid state drive (SSD) products, which are an alternative to a computer’s hard drive. The move to 34nm will help lower prices of the SSDs by up to 60 percent for PC and laptop makers and consumers who buy them due to the reduced die size and advanced engineering design.

Jennic released a demonstration platform that successfully harvests thermal, solar, radio frequency (RF) and vibrational energy to power wireless sensor networks based on the Institute of Electrical and Electronics Engineers (IEEE) 802.15.4 standard such as ZigBee PRO and 6LoWPAN. The platform demonstrates how wireless sensor networks based on the IEEE802.15.4 standard can eliminate the potential maintenance overheads of conventional battery power by harvesting energy from sustainable sources.

Key ASIC now offers IBM’s semiconductor technology to its
customers. As a part of the relationship with IBM, Key ASIC will sell IBM-produced wafers, which contain design content and services from Key ASIC, to its customers.

L-3 Communications, Infrared Products launched its much-anticipated "Thermal-Eye" Renegade-320 thermal imaging system, the ideal multi-use tool for force protection, border patrol officers, law enforcement professionals, special weapons and tactics (SWAT) units, and special operations forces. The "Thermal-Eye" Renegade-320 is designed for the operator that needs a single thermal imaging device that can multi-task as a handheld, a tripod-mounted surveillance system and a thermal weapon sight.

LSI (NYSE: LSI) released real-time, on-demand multimedia transcoding software for the award-winning family of LSI™ Pro multicores media processors that enables flexible, cost-effective solutions for any-to-any video communications and real-time collaboration through next-generation media gateways.

MagnaChip Semiconductor released two new light-emitting diode (LED) driver models for constant current-based portable applications, the MAP1040 and MAP1042. In the wake of its first launch of LED drivers for portable applications, MagnaChip plans to reinforce its presence in the power semiconductor market by further expanding to the LED driver markets for notebooks and TVs down the road. The newly launched models can drive up to four LEDs for displays on portable applications with only one LED driver, and MAP1042 has a stronger power control function with a dual low-dropout regulator (LDO) built-in than the other model.

Micronas (SWX: MASN) launched the new HAL 36xy family with its HAL 3625 Hall-effect sensor based on Micronas’ 3D-Hall technology and equipped with vertical Hall elements. This technology allows rotation angles from 0° to 360° to be detected directly with minimum measuring efforts.

Microsemi (NASDAQ: MSCC) introduced a new line of standard rectifier diode power modules with 21 standard dual-diode modules and six three-phase bridge rectifier diode power modules for industrial, uninterruptible power supply (UPS), switched-mode power supply (SMPS) and motor drive applications. The new standard rectifier diode modules are rated at 1600 volts with a low forward voltage rating.

NEC Electronics (TSE: 6723) successfully developed new architecture that provides both miniaturization and high accuracy to analog circuits, including analog-to-digital (AD) and digital-to-analog (DA) converters. To achieve miniaturization and high accuracy in analog circuits, NEC Electronics’ new architecture possesses a folding technique and a built-in self-calibrating feature that can realize high-accuracy processing of the analog signals.

ON Semiconductor (NASDAQ: ONNN) introduced the NCPS680 supercapacitor-optimized LED flash driver, which is capable of delivering up to 10 amperes for photo flash and video light in ultra-slim camera phones and compact digital cameras.

PLX Technology (NASDAQ: PLXT) sampled four of its newest high-performance PCIe switches that target the server, enterprise storage, control plane and high-end gaming markets. These devices include the highest PCIe switch lane counts in the industry at 96 and 80 lanes.

Powerpervision released the PV3002, the company's inaugural product and the industry's first Auto-control™ digital power conversion IC. The new chip is aimed at electronic systems used in computing, netcomms and storage applications where it brings fully automatic adaptive control to DC-DC conversion for the first time.

Qualcomm (NASDAQ: QCOM) introduced the WCN1312™, a single-chip, high-performance, 802.11n-compliant wireless local area networking (WLAN) solution for handsets and mobile devices. This highly integrated device supports data rates of up to 72Mbps, which is significantly higher than previous 802.11a, b and g Wi-Fi solutions, for a better user experience when downloading data, watching streaming video or surfing the Internet.

Redpine Signals and Ascom Wireless Solutions partnered to create next-generation voice-over-Wi-Fi (VoWiFi) phones with 802.11n wireless connectivity. The new VoWiFi phone designs are built upon Ascom's long experience of offering state-of-the-art purpose-built handsets, wireless voice and message transmission systems, and customized alarm and positioning applications.

RF Micro Devices (NASDAQ: RFMD) entered into a cooperative agreement with the U.S. Department of Energy's National Renewable Energy Laboratory (NREL) to develop a commercially viable and high volume-capable compound semiconductor-based process for high-performance photovoltaic (PV) cells.

Sandisk (NASDAQ: SNDK) introduced the fastest 32GB Secure Digital High Capacity (SDHC™) card on the market. The 32GB Sandisk Extreme™ SDHC™ card at up to 30MB/s read and write speeds combine industry-leading performance with massive storage capacity, helping digital photography enthusiasts utilize the advanced features of today's digital single-lens reflex (DSLR) cameras.

Skyworks Solutions (NASDAQ: SWKS) partnered with several of the energy industry's top solution providers to meet the growing worldwide demand for smart water, gas and electric meter readers. These strategic partnerships enable Skyworks to develop and ramp low-cost solutions for remote meter reading applications and smart grid technologies.

Standard Microsystems (NASDAQ: SMSC) released the OS85650 input/output (I/O) companion chip for MOST™ intelligent network interface controllers (INICs). With its multiple interfaces, powerful routing engine and the Digital Transmission Content Protection (DTCP) co-processor, the OS85650 can be used for various audio and video applications such as head units, rear seat entertainment, amplifiers, TV tuners and video displays.

Summit Microelectronics introduced two more members of its third-generation programmable battery charger IC family: the SMB136 and SMB137B employ CurrentPath technology, providing dual input source (USB or AC/DC) with arbitration, dual output for system and battery, and system operation with a dead or missing battery.

Teradici launched a comprehensive new partner program for value-added resellers (VARs), system integrators (SI)s and OEMs who want to deliver superior remote computing and virtual desktop solutions to their customers. The new PC-over-IP™ (PCoIP) partner program provides VARs, SI's and OEMs with everything they need to sell and deploy PCoIP-based solutions, including product education, marketing collateral, competitive information, sales leads, product discounts, and both marketing and technical assistance.

Teranetics showcased Arista Networks’ high-density, auto-negotiating 1/10GBASE-T 7100T switches. The Arista 7100T switches, featuring both 48- and 24-port models, take advantage of the Teranetics TN2022 dual-port PHY to deliver the highest port density possible in an Ethernet system, 48 ports in a one rack unit form factor.

Eurocompost will sell a selection of VIA Technologies’ (TSEC: 2388) comprehensive range of innovative products, including VIA’s unique range of highly integrated processors, chipsets and companion chips, as well as a variety of ultra-compact form factor boards and application-specific systems.

Vitesse Semiconductor (OTC: VTSS.PK) expanded its next-generation fiber-to-the-home (FTTH) technology ecosystem with the addition of three industry-leading companies—ZTE, the Electronics and Telecommunications Research Institute (ETRI) and CyOptics. Brought together to accelerate the deployment of next-generation 10G passive optical network (PON) systems, Vitesse’s industry-leading effort will accelerate innovation, supply key components and enhance service delivery.

Wolfson Microelectronics (LSE: WFL) released the WM8994, the second device in a new family of highly integrated, ultra low-power audio hub coder/decoders (CODECs) for smart phones and other feature-rich portable audio applications. The WM8994 takes the highly flexible signal routing and processing of previous Wolfson audio hubs to a whole new level with the addition of an innovative, new HexCore™ digital baseband interface, giving great audio performance at a lower system BOM cost than even the most integrated single-package, cellular-based architectures.

Zilog (NASDAQ: ZILG) released a new enhanced low-voltage serial communications controller (SCC) for a variety of computing applications requiring increased performance and lower power consumption. The Zilog Z8523L enhanced SCC builds on Zilog's popular and original discrete SCC, providing a low-power solution that reduces the voltage from 5 volts to 3.3 volts. The enhanced SCC also features performance improvements that allow applications, including computer peripherals, networking equipment and routers, to experience faster data rates and increased processor bandwidth.
Innovation has been and continues to be the cornerstone of semiconductor companies. Until the year 2000, companies were focused on product innovation, but for over eight years, companies have focused on supply chain process innovation in addition to product innovation. This change in focus is not surprising, as it is the response to the changing semiconductor manufacturing landscape.

Today, most integrated device manufacturers (IDMs) use external partners for many of the business functions they previously performed in-house. Many of the newer semiconductor companies formed in the last decade began their journey as a fab-lite company. And almost all semiconductor companies formed today are purely fabless. The underlying driver of this outsourcing trend is the cost of manufacturing. Hence, the initial focus of semiconductor companies is on foundries and outsourced assembly and test (OSAT) partners. Semiconductor companies have benefited from the location of these partners' facilities in lower cost countries, and pure-play foundries and OSAT providers have achieved economies of scale by providing the same service to multiple semiconductor companies, which has lowered the overall cost of manufacturing.

Semiconductor companies have undertaken continuous business process improvements, outsourcing business functions beyond manufacturing operations. In response, suppliers and service providers have mushroomed around the world to provide specific business functions to these companies. These functions include: product/feature design; manufacturing operations, such as wafer fabrication, bump, probe/sort, assembly and test; warehouse and outbound logistics (through third-party logistics (TPL) service providers); human resources; and managing planning functions. It suffices to say that in today's world, a semiconductor company depends on a number of partners to get their product to market.

The Challenge
The new world order of the semiconductor industry involves working in collaboration with multiple partners in multiple countries. A closed-loop business process, which was once contained within an organization, now expands beyond the walls of a legal corporation. A control that was easy to maintain within an organization now takes a different form in the new era.

Cross-company collaboration leads to various forms of risk:

- Process risk.
- People risk.
- Technology risk.
- Government and regulation risk.

There are a number of risks under each of these categories, and each risk has different levels of impact and probability. Companies need to understand the risks involved to put in the right level of controls and mitigation plan. This is critical because if risk control is not calibrated correctly, it can thwart innovation embarked upon by those in the collaboration, and instead foster mistrust between partners.

Process Risk
Process risks are related to managing business processes that extend beyond the enterprise. Companies working with design, planning, manufacturing, distribution and customer service providers will require a process that has controls across the supply chain; however, all these providers should be able to operate independently as separate entities.

An example of a process risk is a new product introduction. A semiconductor company working with a design partner will have to put a design review process in place that involves participants from design, manufacturing and customer services. This process must be a virtual collaborative process that is efficient and effective. This is important because any delays caused by exchanging ideas and designs with multiple partners could lead to the wrong design being introduced at the wrong place and at the wrong time, defeating the very purpose of having specialized companies manage specific

Figure 1. Risk Categories

- Process
- Government & Regulation
- People
- Technology

Santhosh Kumar M, Client Partner, Bristlecone Inc.
business functions.

Similar risks can be identified across all business processes. When developing a process control to mitigate process risks, one needs to also consider people, technology and government risks. The solution is built upon trust and involves designing review and control processes that are virtual and collaborative. As simple as this may sound, there are enormous challenges involved. Even when all business functions are within the same enterprise, there is mistrust between departments, and this mistrust magnifies when departments are geographically separated. Egos become greater and it becomes difficult to align business processes with one collective company objective. Success can be achieved when semiconductor companies collaborate with service providers that have a common objective. Objectives must be set at the network level to mitigate the risk introduced by having multiple partners in the process.

**People Risk**

The best business process has the right people in place to manage and execute. People, in general, introduce a high degree of variability to the process because of cultural, national, generational, educational, communication and experience differences. However, many of these differences have been abated to a large degree with the migration of people around the world and with organizations becoming truly global.

Of all the differences listed above, the single-most important factor that introduces variability is communication. With business functions spread across different organizations, it is vital to have close communication between partners. For example, if the customer service provider does not voice customer concerns or needs to the semiconductor company, then a faulty design will result and not produce any real value to the customer.

Various tools, such as conference calls, Web meetings and video conferencing, are used to improve and speed communication. The dependability of these tools is so high that any malfunction or non-availability of these resources can delay decisions and impact the process. However, even with all tools working properly, there is still the chance of miscommunication, so it is always good practice to confirm all major decisions made during a meeting.

Information shared between companies that are managed as separate entities in different countries that are governed differently also increases risk. For effective intellectual property (IP) protection, an agreement must be signed by all partners and backed by their countries of origin.

When all business functions were performed in-house, hiring for various departments was within the control of human resources. However, in the new model, semiconductor companies have practically no say in the recruitment of individuals that will be working on the company's design or other functions at their partner's location. The concept of having an unknown team working on the most critical functions of a company's business process can be unnerving. This creates a huge risk in terms of IP protection, loyalty and dependability. Success will depend on the due diligence conducted before any partners are chosen to understand their recruitment policies, training policies, treatment towards employees and culture.

**Technology Risk**

A company becomes highly dependent on technology to manage business functions across the supply chain and improve communication. But the use of technology comes with risk of its own. Technologies used by a semiconductor company's partners are not within its control. Each company stores data differently using different systems, and has internal security policies that are not controlled or governed by the semiconductor company.

The collaboration tools used to share information over the Internet are subject to information leakages. There are technologies which allow information sharing in a secure manner, but the data is never as secure as it is when within the firewalls of a corporation.

The use of e-mail to share information is even more unsecure as partners could mistakenly send e-mails to the wrong company and release confidential information.

Systems and technologies used for managing business functions need to be audited by the internal control organization to ensure a proper level of security and control. Semiconductor companies may need to review their partners’ policies and periodically audit their data access and confidentiality processes. This needs to be done to build trust and confidence in the partnership and to mitigate technology-related risks between partner companies.

**Government and Regulation Risk**

Government- and regulation-related risks probably have the most impact of all the risk categories. With semiconductor companies working with partners who are based in different countries and with unrest arising around many parts of the world, country/political stability needs to be monitored from time to time to ensure continuity of business without interference. Research institutes such as Harvard have recognized the importance of these risks and have instituted a measurement for stability. The factors considered are:

- Government (i.e., strength of current government, rule of the law and level of corruption).
- Society (i.e., social tension, youth disaffection, health, education and other services).
- Security (i.e., level of globalization, geostrategic condition, emergencies and disasters).
- Economy (i.e., fiscal condition, growth, investment, external sector and debt).1

See Risk Management page 47
American Semiconductor demonstrated flexible CMOS using Flex™ Silicon-on-Polymer (SOP™) technology. The unique Flex process is a post-fab, low-cost method for production of single-crystalline, <2000-angstrom, thin-body CMOS on polymer. The process is in late-stage development and may be a possible CMOS solution for flexible electronic and display applications.

American Semiconductor is a U.S. foundry offering pure-play, on-shore foundry services to suit customers’ needs. Services include Flex™ SOP™ technology; Flexfet™ advanced CMOS technology; and custom fabrication for non-standard wafer processing, novel process integration or copy smart process replication.

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austriamicrosystems’ business unit Full Service Foundry announced its patented through-silicon via (TSV) technology for foundry customers. With TSV technology, two 8-inch wafers can be electrically connected. With typical TSV depths of 200μm to 300μm, it is especially targeting three-dimensional (3D) integration of CMOS ICs and sensor components. Due to its flexible manufacturing concept, customer-specific modifications as well as varying wafer thicknesses can be supported.

The patented TSV technology addresses a variety of markets demanding 3D integration of CMOS ICs, photo sensors, gas sensors, power devices or microelectromechanical systems (MEMS) components such as automotive, industrial and consumer applications. Foundry customers using austriamicrosystems’ TSV concept immediately benefit from a significantly reduced form factor, systems cost reduction as well as performance improvements due to shortened interconnect lengths. A proprietary back-side re-distribution layer concept enables various front- and back-side input/output (I/O) pad connections and provides customers with the utmost flexibility in IC and sensor arrangement.

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Chartered Semiconductor Manufacturing is delivering an enhanced version of its 65nm low-power process called 65nm LPe. The new 65nm LPe process utilizes innovative leakage reduction techniques to significantly improve system-on-chip (SOC) standby power consumption by up to 50 percent. A full suite of intellectual property (IP) is available for the new process. Chartered has also worked with several of its partners to offer a robust 65nm radio frequency (RF) platform specifically geared for development of single-chip RF products. The Chartered offering, jointly developed with IBM, is based on Chartered’s enhanced 65nm LPe process and includes an IBM RF physical design kit.

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Pioneering the open foundry business model in China since 1997, CSMC Technologies is a leading pure-play specialty analog foundry providing fabless design houses and integrated device manufacturers (IDMs) with 6-inch and 8-inch manufacturing services.

CSMC’s Fab 2 commenced 8-inch wafer production with emphasis on high-voltage analog, mixed-signal and power processes in 2008. Potential analog products can be utilized in a broad range of end market applications, including consumer electronics, communications devices, computer peripheral equipment and automotive. The target capacity of Fab 2 is 30,000 8-inch wafers per month in early 2010, with process technologies advancing to the 0.13μm node.

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Fujitsu Microelectronics America (FMA), a leading wafer foundry and application-specific IC (ASIC) service provider, offers world-class semiconductor solutions to fabless and system companies. Based on its advanced CMOS processes and application-optimized design IP, Fujitsu’s technology platforms are available from the 180nm to 65nm nodes to customer-owned tooling (COT) customers.

For customers who prefer a full-service engagement model, FMA provides complete turn-key ASIC services for quick time-to-revenue. Fujitsu’s technical experience, design expertise and complex packaging capabilities are keys to its long track record of consistently delivering first-pass success in SOC development and production.

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Jazz Semiconductor, a Tower Group Company, attained quality automotive certification and announced that all Tower/Jazz facilities have now achieved world-class quality standards in the automotive, environmental management, health and safety, and information security markets.

Jazz and Xceive announced volume production of silicon tuners for flat-panel TVs. These silicon tuners have been adopted by LG
for its liquid crystal display (LCD) and plasma TVs.

The University of California, San Diego (UCSD) announced it leveraged Jazz's high-speed SiGe process to develop a two-antenna, quad-beam, 11–15GHz phased array RFIC targeted for satellite systems and advanced radars, replacing eight GaAs chips while lowering cost and increasing integration.

Jazz released its DIRECT multi-project wafer (MPW) program to enable rapid design verification and faster time-to-market. In addition, Jazz joined the Cool Planet project to increase the efforts of the company's “green” operations, reducing its carbon footprint and energy use.

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Peregrine Semiconductor, a leading supplier of high-performance RF CMOS and mixed-signal communications ICs, and MagnaChip Semiconductor, a leading Asia-based designer and manufacturer of analog and mixed-signal semiconductor products for high-volume consumer applications, completed the final qualification phase in the process technology transfer of Peregrine's UltraCMOS silicon-on-sapphire (SOS) technology to MagnaChip's Cheongju wafer manufacturing facility. Peregrine and MagnaChip began the final qualification phase of the technology transfer in July 2008 and released it to production recently. The 10-month qualification cycle of UltraCMOS technology is exceptionally short due to its standard CMOS foundation.

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SilTerra Malaysia Sdn. Bhd. partnered with Hong Kong-based South Sea Semiconductor to develop a new breed of power metal-oxide semiconductor field-effect transistor (MOSFET) technology for highly efficient low RDS(on) devices used in Li-ion battery pack direct current-direct current (DC-DC) converters for notebooks. The V-Tr FET technology features a narrow trench gate electrode with a cell density of 488 million per inch square. The technology is realized using an existing production-ready 0.16μm toolset. Both 20V P-channel and 20V N-channel devices are developed using this V-Tr FET technology which delivers competitive low RDS(on) at 3.4A with a small outline transistor (SOT)-23 package and 6.0A with a thin-shrink small outline package (TSSOP)-8 package, respectively. The technology is currently in mass production and has already been offered to several power management customers.

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The U.S. photovoltaic (PV) market (i.e., solar cells) is ready to expand, with emerging opportunities plus access to economic stimulus funding. However, to enter production with new PV products, both start-ups and established companies need access to capital equipment and cost-effective, complete development solutions. SVTC Technologies, in a newly expanded partnership with Roth & Rau, a world-leading solar equipment manufacturer based in Germany, is establishing the Silicon Valley Photovoltaic Development Center. This center will offer a world-class 30MW PV production line and a full range of low-cost development services designed to accelerate the commercialization of new PV technologies.

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Taiwan Semiconductor Manufacturing (TSMC) unveiled two unified electronic design automation (EDA) data for 40nm process technology—interoperable design rule check (iDRC) and layout-versus-schematic (iLVS). Along with this, TSMC also released the semiconductor industry's first interoperable process design kit (IPDK) for advanced technology. The kit is fully validated on TSMC's 65nm process and focuses on enhancing innovation in custom/analog/mixed-signal/RF designs.

These initiatives are part of TSMC's Open Innovation Platform™ (OIP), a platform that promotes the speedy implementation of innovation among TSMC customers and ecosystem partners.

Established in 1987, TSMC is the world's largest dedicated semiconductor foundry. As the founder and leader of the dedicated foundry business, TSMC has built its reputation on providing advanced wafer production processes and unparalleled manufacturing efficiency. From its inception, TSMC has consistently offered the foundry segment's leading technologies and TSMC-compatible design services to its customers. The company's total managed capacity exceeds eight million 8-inch equivalent wafers, while its revenues represent approximately 50 percent of the dedicated foundry segment. TSMC became the first semiconductor foundry seven years ago to enter the ranks of the top 10 IC companies in worldwide sales. According to an IC Insights report, TSMC ranked number five in worldwide sales in 2008.

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Tower Semiconductor announced it is the first foundry with magnetoresistive random access memory (MRAM) capability and will manufacture next-generation MRAM from Crocus Technology. Tower will also hold an equity position in Crocus.

In addition, Tower announced an industry-first scalable RDS(on) versus breakdown voltage design kit technology (TS18PM) to enable 10–40 percent smaller die sizes and faster design cycle times targeted at the growing power management market.

Tower also collaborated with Panavision to produce the world's fastest single-port reconfigurable linear image sensors to address many applications in the consumer, industrial, automotive and scientific markets.

Tower and its subsidiary Jazz Semiconductor announced the call for papers for its 2009 Analog-Intensive Mixed-Signal Circuits, Applications and Technology (AIMS-CAT) conference on November 5, focusing on the latest advances in SiGe, RF CMOS, bipolar/CMOS/D MOS (BCD) and CMOS image sensor (CIS) process technologies.

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United Microelectronics (UMC) and Magma Design Automation introduced an integrated low-power IC reference flow for the foundry's advanced 40nm process. Based on the Magma Talus IC implementation system and fully compliant with the Unified Power Format (UPF), it allows designers to address low-power nanometer design considerations during implementation and within a single environment, maximizing quality of results (QoR) while reducing turnaround time.

UMC has also worked with SpringSoft to introduce a Laker PDK for UMC's 65nm technology. The PDK includes device symbols, highly optimized parameterized cells (i.e., Laker MCells), pre-validated design rules and the latest technology files.

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Faking It: Why Counterfeiting is the Symptom, Not the Disease

Frank Cavallaro, Chief Executive Officer, Converge

Distributors can’t stop chip counterfeiting from occurring, but they can take better steps at achieving excellence and protecting the integrity of the electronics supply chain. Working together, the industry can raise the baseline of quality processes and reduce, if not eliminate, the majority of sub-standard parts, making it a lot harder for counterfeiters in the process.

Counterfeiting gets a lot of attention—and rightfully so; it’s a topic that fuels media headlines and puts everyone on edge. Researchers estimate that between 5–20 percent of components in distributors’ supply chains are sub-standard devices, costing the electronics industry up to $100 billion per year—so a little sensationalism is in order. One police raid in China’s Guangdong province found $1.2 million in counterfeit computer parts and documents which were labeled with the logo of a big-name U.S. computer company. And now there are threats that go beyond monetary loss. Recently, the U.S. government reported that fraudulent chips are being found in national defense networks.

However, while counterfeiting is a serious issue, the real problem is a lack of quality in the distribution system. As an industry, when it comes to ensuring quality in the modern global supply chain, it is a victim of its own economics. There are inherent monetary pressures to skim on people, processes and technologies that can make the system more air tight.

Underlying market forces create overly ripe conditions for counterfeiting to flourish.

- Insatiable Demand for New Products: Even in a down economy, the right products marketed the right way will fly off the shelves, as seen with Apple’s record sales of its iPhone. Strong demand puts pressure on supply, which unto itself is good, but it further exposes weak links in the supply chain.

- Speed: Time-to-market pressure, just-in-time inventories and product upgrade cycles all contribute to “quality evaporation,” as the amount of time allotted to check and monitor the integrity of many parts moving through a large system at a rapid pace is cut.

- Globalization: The more dispersed a marketplace becomes the more difficult it is to control throughput. With outsourcing and “midnight fabs,” the nodes of production and distribution multiply and almost disappear into the fog of the global economy.

The result: a planet-sized marketplace fed by a supply chain in a state of perpetual motion, governed by an almost infinite set of variables and whose primary mantra is “faster and cheaper”—not exactly a formula for a patient, thoughtful approach to quality.

The Monkey is in the Middle

Electronics distributors cannot eliminate the motive for counterfeiting, but they can cauterize entry points for imitation products through vigorous quality control. Like any complex ecosystem, the weakest links are the links themselves—the hand-offs. The very nature of a distributor’s business model is that no parts are made by the distributor, only the manufacturer. Some might argue that this creates a “get out of jail free card,” a kind of genetic excuse
for allowing the occasional rogue part into the system. “It’s not our fault, we don’t have the capability or experience in hardware quality the way the manufacturer does.” One should have zero sympathy for that argument. The service sector has learned as much, if not more, about total quality than the manufacturing sector over the past decade or two. It is suggested that some in the distribution arena have a different problem: They don’t know they’re in the service business! Distributors have a responsibility for quality that is at least as great, if not greater, than original equipment manufacturers (OEMs).

Global law enforcement agencies are vigilant and do find counterfeiters and shut them down. But such scrutiny does nothing to pinpoint where the corrupt part(s) became viable in the supply chain.

**Credentials and Certifications**

A lack of quality discipline turns suppliers into involuntary peddlers of sub-standard products—that’s the harsh truth. This is why distributor organizations, such as the Independent Distributors of Electronics Association (IDEA), have recently issued more stringent standards for membership; it’s an effort to systemically raise the quality bar. These organizations are evolving from networking clubs into standard bearers for best practices. As they move to a model of earning membership, they help put the entire industry on a more quality-conscious track. A number of these groups offer more than membership. For example, IDEA puts forth specific standards that every distributor should adopt and even exceed. Here’s an overview of those initiatives/organizations/resources that are absolutely essential for a global semiconductor distributor to get involved in or use to remain quality-conscious:

- Customs-Trade Partnership Against Terrorism (C-TPAT): a voluntary government-business initiative to build cooperative relationships that strengthen and improve the overall international supply chain and U.S. border security.
- IDEA: IDEA-STD-1010-A is the first inspection standard addressing the need for the inspection of electronic components traded in the open market.
- ERAI: a resource for risk assessment information and insight, enabling companies to analyze risk mitigation on vendors, customers and parts.

The following are “must-have” certifications to international standards that apply to a distributor’s facilities and personnel:

- International Organization for Standardization (ISO) 9001: a quality management system standard.
- ISO 14001: an environmental management system standard.

These certifications do require an investment of money, time and, perhaps more challenging, endurance. ISO, for example, requires that an organization be able to document its business practices and demonstrate continual improvement. ISO is an example of how true quality requires a behavior change and commitment, not only lip service.

**Quality Starts at Home**

A company should not only meet all these external criteria, but also have its own inspection process that exceeds any program in the market. Quality should be taken very seriously, even fanatically. A company should approach quality with a philosophy of “zero tolerance” which pervades the various types of evaluations performed across the procurement business, including:

- Vendor-Managed Programs: Research, pre-qualify and continuously maintain vendor sources around the globe to ensure that products received are procured from safe and reputable sources.
- Systems Controls: Monitor and grade suppliers on an ongoing basis. This helps identify any potential problems or concerns early in the product procurement process.
- Rigorous Inspection Process: Products received must pass an extensive inspection process before being received and prepared for shipment. This includes visual inspection, engineering review and sampling, and product testing.
- Continual Training: Having a strict regimen is one thing, but having the people who can execute it flawlessly is another challenge altogether. With the constant changes in technology and product manufacturing, provide continual training to inspectors to keep them up-to-date with the latest manufacturing trends, industry best practices and counterfeiting techniques. IDEA offers a certification program for inspectors.
- Spot Quality Control Testing: Continually improve quality control processes by conducting self audits, systemic testing of product samples and sending materials to an independent third-party testing vendor to verify findings.

Sourcing, supplying and guaranteeing quality for millions of semiconductors and electronic sub-systems to meet the demands of a tech-powered global economy is serious business. Tentative organizations do not manage risk very well. Sustainable quality requires commitment and bold action. It’s what should be demanded from any organization because it’s what customers demand. Distributors can do better and should always strive to do so. A distributor’s mindset of a devotion to total quality is this industry’s best defense against counterfeiting. Quality as an antidote to counterfeiting has a very rewarding side effect—better products. If the industry is using excellence to eliminate phony chips, then it is also using excellence to increase the quality of products reaching its customers. That is a true win-win situation.

**About the Author**

Mr. Cavallaro has more than 20 years experience in electronic component distribution and supply chain services. His market insight and financial discipline have helped Converge become the largest independent distributor of electronics. Recently, he has led the company’s diversification into strategic services for IT asset disposition and reverse logistics. Prior to his appointment as chief executive officer, Frank held several key management roles at Converge, including chief operating officer, vice president and general manager, and vice president of global sales. Frank holds a bachelor’s degree in economics and legal studies from the University of Massachusetts Amherst. He is a member of the Young Presidents Organization and currently sits on the board of IDEA.

**References**

**AccelerATE Solutions** is a multi-platform test engineering service provider located in San Jose, California. The company’s mission is to leverage its extensive experience and contacts within the semiconductor test arena to expedite its customers’ time-to-market. AccelerATE provides the following services to reduce production costs: test pattern conversion, test interface development, test program development, device characterization, failure analysis (if required), test program optimization, sample production, deployment to volume manufacturing, and test program conversion.

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Advantest’s new T5385 memory test system for dynamic random access memory (DRAM) wafer test delivers an unrivaled 768-device under test (DUT) parallel test capacity and 533Mbps capability for increased throughput and lowered cost of test. Ideal for high-volume wafer fabs, the new tester is also equipped with a flexible pin configuration that supports diverse DRAM devices, allowing tester pin resources to be optimally allocated for efficiency, reduced touchdowns and improved throughput. Achieving improved efficiency per device while scaling even higher in parallelism, the T5385 also delivers known good die (KGD) for consumer devices to greatly reduce test time.

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Frost & Sullivan is presenting Amkor with the 2009 Global Advanced Electronic Packaging Technology Innovation of the Year Award at their Growth, Innovation and Leadership conference in Scottsdale, Arizona. The award is based on Frost & Sullivan’s analysis of the advanced electronic packaging market, where Amkor’s innovative, new products, such as through-mold via package-on-package (TMV™ PoP), FusionQuad® and flip-chip molded ball grid array (FCMBGA), were recognized for technical innovation and electronic packaging leadership. Each year, Frost & Sullivan presents awards to the company (or individual) that has carried out new research which results in innovation that has or is expected to bring significant contributions to the industry in terms of adoption, change and competitive posture.

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BroadPak, a premier provider of semiconductor package substrate design and signal integrity services, introduced a revolutionary design methodology for packaging the emerging 40nm node. With its core expertise in advanced, high-performance substrate design and test, BroadPak is the only independent substrate design center dedicated to silicon-package co-design methodology for demanding applications where cost reduction and increase in performance matters. Through unique miniaturization techniques, BroadPak provides an unprecedented level of miniaturization for system-in-package (SiP) used in very low-profile (VLP) applications.

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In response to customer demand for independent, flexible IC development and supply engineering services, DA-Test expanded its offering to include IC design, strategic production test, product engineering and supply management. The expanded offering also includes a new name and a head office, doubling the size of the automatic test equipment (ATE) lab and allowing room for future growth.

DA-Integrated is the semiconductor industry’s first and leading provider of comprehensive IC development services, helping customers optimize time-to-market, development cost, cost of goods sold and product quality. Their highly experienced team has provided solutions for a broad range of applications and device characteristics. DA-Integrated focuses on customer requirements and offers flexibility in technical scope and commercial terms.

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**Evans Analytical Group’s (EAG) release-to-production (RTP) team provides engineering service and support from early chip design to volume production in the areas of test program development and product engineering; test time rental on all major ATE platforms; reliability and environmental qualification; electrostatic discharge (ESD) and latch-up testing; printed circuit board (PCB) layout and hardware design; failure.
analysis; focused ion beam (FIB) circuit edit and debug; electron microscopy; and equipment calibration and repair services. EAG also has over 30 years of experience in bulk materials characterization and surface analysis.

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ISE Labs is dedicated to the growth of failure analysis capabilities to meet the needs of customers. The company’s failure analysis lab has recently brought in a new team led by Dr. Dan Sullivan, formerly of Phillips and LSI. As well, ISE Labs upgraded most of its equipment, including the installation of a new Hitachi S-4800 scanning electron microscope.

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Maser Engineering offers fabless IC manufacturers and integrated device manufacturers’ (IDM) design groups first silicon circuit edit using the latest FIB systems. This service is now available with the most advanced system for single-die consumer electronic (CE) work, DCG Systems’ OptiFIB-IV. This latest generation of CE FIB systems is capable of front and backside modification. It has a unique coaxial FIB/near infrared (NIR) optics column and a Graphic Data System II (GDSII) data-controlled piezo table for backside navigation to features in the first metal layers of 40nm technology devices. Advanced endpoint techniques as well as accurate copper metal layer removal and deposition of low-ohmic molybdenum and platinum conductors and silicon oxide isolation layers give design groups the possibility to avoid multiple re-spins and the increasing costs for sub-100nm masks. Time-to-market for new, advanced ICs can be shortened when using this new facility.

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Mfg Vision specializes in low-cost, straightforward yield management and data analysis for large and small companies.

The company’s FloorVision product helps customers achieve higher yields and more efficient manufacturing using a very attractive Web-based tool. What distinguishes FloorVision is its ease-of-use, speed and collaborative attributes, taking advantage of Web 2.0. Fabless companies can also now provide a revolutionary third-party FloorVision license to their foundries to help resolve fab-related issues more quickly. Round-the-clock support and regular seamless upgrades are part of the package when companies purchase licenses for FloorVision.

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Recruiters can also now provide a revolutionary third-party FloorVision license to their foundries to help resolve fab-related issues more quickly. Round-the-clock support and regular seamless upgrades are part of the package when companies purchase licenses for FloorVision.

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Using an industry-standard cost of ownership model, Scanimetrics has saved 54 percent of semiconductor test costs. Scanimetrics’ Wireless Test Access Port (WiTAP™) test technology can test many times and at any time during the fabrication process, making it ideal for wafer-level and SiP testing. On top of the 54 percent test savings, Scanimetrics has shown that using WiTAP™ also increases product revenue by improving yield, saving on discarded product, reducing chip size, steepening yield ramps and increasing time-to-market.

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MTVS Technologies’ business model includes partnering with original equipment manufacturers (OEMs) of ATE to provide a transition plan for the support and availability of legacy and discontinued equipment. While each OEM relationship is different, all provide ATE users with a resource for capacity expansion and support for maturing ATE.

Specifically, MTVS provides services such as parts repair, labor and field service, tester maintenance agreement support, tester rental, application services and regional facilities to make newer generation testers available for engineering and product development. MTVS also purchases idle or surplus equipment for inventory to support resale of these out-of-production equipment and parts. Utilizing the extensive internal inventory expertise, MTVS offers users of this equipment a turn-key OEM-like buying experience. The equipment is configured to match the needed requirement, packaged with warranty, training, applications, installation and an extended service contract.

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RoodMicrotec is the first independent test house in Europe with fully automated monitored burn-in service. By investing in a fully automatic loading/unloading system, RoodMicrotec is now able to execute the burn-in process automatically. This increases quality and shortens processing time, and no manual steps are necessary which optimizes process safety. The process can now handle high-volume burn-in as well as safe launch activities. The automatic system has a throughput of up to 5,000 devices per hour, which is 10x faster than manual operation. The reduction in processing time leads to a significant reduction in total cost. Amid the current market situation, this is essential and results in a clear competitive advantage for the customer.

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Stats ChipPAC has introduced a new flip-chip technology that offers significant cost savings over standard flip-chip packages, with price points well below wire bond packages. STATS ChipPAC’s low-cost flip-chip technology features an innovative, routing-efficient interconnection structure and a simplified substrate technology design coupled with improvements in assembly technology such as a cost-effective mold underfill process. The low-cost flip-chip technology also features a true lead-free bump composition which has proven to be effective with the mold underfill process. The first phase of low-cost flip-chip technology was qualified in 2008 and is in high-volume production today.

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Driving technology forward at semiconductor manufacturers requires companies to have equipment and process expertise in multiple areas. Shorter product life cycles put increasing pressure on companies to maintain or even accelerate research and development (R&D) efforts. Many companies are choosing to push these efforts down to the original equipment manufacturers (OEMs) and supplier base to get the most out of their R&D investment. The complexity and costs involved with chemical mechanical planarization (CMP) require a unique skill set to address the diverse integration schemes that continue to drive the semiconductor industry. Mainstream CMOS processing continues to advance with the introduction of new materials and shrinking geometries. Additionally, technologies such as microelectromechanical systems (MEMS), optoelectronics and other nanotechnologies are using a number of different materials and manufacturing techniques. Their choice of materials depends on the device being created and the market sector in which it is intended to operate. Planarization requirements continue to emerge with each new opportunity. Specialized outsource partners can be complementary to R&D groups to reduce risks, accelerate prototypes and bring products to market faster. By virtue of a broad exposure to multiple technology development activities, outsource service companies focused on individual process modules can navigate efficiently through many cycles of learning in a shorter period of time.

What is Driving Technology Forward and What Hinders Development?

The semiconductor manufacturing industry is constantly striving to maintain the path of Moore’s Law. While there are ongoing discussions about how realistic that is, or how relevant Moore’s Law remains, the fact that manufacturers will continue to push for smaller linewidths and higher performance (at lower costs) is indisputable. The consistent push for smaller, faster chips has historically driven technology advancements in terms of process tools and manufacturing processes, and is increasingly calling for the examination and qualification of a huge variety of potential materials to enable future generations of devices.

However, the question remains: Who is best positioned to perform these R&D activities? Should it rest with the chipmakers or OEMs? Each might say the other, but, increasingly, both are turning to outsource service providers who can fill this essential role. While on the surface it is counterintuitive to look to an outside entity to develop in-house manufacturing processes, these outsource service providers offer a significant and highly focused resource that alleviates the burden both on fab equipment and personnel, and, in large part, can allow IC manufacturers and OEMs to pursue advanced R&D research without impacting active manufacturing projects. By stepping outside of one’s internal organization and working with process experts with a huge library of focused knowledge, development becomes greatly simplified and accelerated.

While the industry has always been cyclical in nature, current economic conditions have placed even more stress on manufacturers and equipment suppliers. The same requirements are in place to continue to develop advanced technologies, but with both internal (hiring) and capital equipment budgets often restricted, if not outright frozen, moving new projects forward presents a purely tactical problem for the industry. This is another factor that drives manufacturers to move towards outsourcing specific process modules where comprehensive knowledge is available that can drive technology forward and do it efficiently.

R&D Investments

In general, R&D costs average 15–17 percent of semiconductor revenue. IC device complexity, the introduction of new materials and shorter product cycles continue to increase R&D costs exponentially. Outsourcing appropriate portions of R&D is a means of lowering the cost of developing and deploying new technology. Driving innovation forward must continue in downturns, so the ratio of R&D to revenue can increase significantly.
Outsourcing CMP

CMP is one semiconductor manufacturing process that lends itself extremely well to being developed and manufactured using an outsourcing model. Between the considerable process complexity and the fact that surface topography from underlying layers can cause yield-limiting problems for the next process step, it highlights where dedicated resources and expertise can enable manufacturers to accelerate R&D, ramp manufacturing and, ultimately, get product to market considerably faster than by exclusively relying on in-house resources.

So why does CMP lend itself so well to outsourcing? Since the development of CMP, the number of materials polished in various CMOS process flows has steadily grown, as shown in Figure 1. Further, each material also requires a unique slurry, a properly designed pad, optimized process settings for both polish and post-CMP clean, and other factors that must be individually tailored to the application. Between the number of materials that require CMP and the associated consumables sets, the advantage of being able to utilize the knowledge base and resources of an outsource provider is fairly straightforward.

Figure 1. CMP Materials Roadmap

<table>
<thead>
<tr>
<th>1995 - Qty ≤ 2</th>
<th>2001 - Qty ≤ 5</th>
<th>2009 - Qty ≤ 36</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
<tr>
<td>Glass (oxide)</td>
<td>Glass (oxide)</td>
<td>Glass (oxide)</td>
</tr>
<tr>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Doped Oxides</td>
</tr>
<tr>
<td>Copper</td>
<td>Copper</td>
<td>NiFe &amp; NiFeCo</td>
</tr>
<tr>
<td>Shallow Trench</td>
<td>Shallow Trench</td>
<td>Noble Metals</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Al &amp; Stainless</td>
</tr>
<tr>
<td>Low k</td>
<td>Low k</td>
<td>Polymers</td>
</tr>
<tr>
<td>Cap Ultra Low k</td>
<td>Ultra Thin Wafers</td>
<td>Diamond &amp; DLC</td>
</tr>
<tr>
<td>Metal Gates</td>
<td>Direct Wafer Bond</td>
<td>Si &amp; Reclain</td>
</tr>
<tr>
<td>Gate Insulators</td>
<td>Through Si Yos</td>
<td>SiO2</td>
</tr>
<tr>
<td>High k Dielectrics</td>
<td>3-D Packaging</td>
<td>Quartz</td>
</tr>
<tr>
<td>H &amp; Pi Electrodes</td>
<td>MEMS</td>
<td>Titanium</td>
</tr>
<tr>
<td>Magnetics</td>
<td>Nanodevices</td>
<td>Integrated Optics</td>
</tr>
</tbody>
</table>

Figure 2. Factors to Consider When Performing CMP

In addition to the general concerns with CMP process control, each of the following CMP processes has unique issues.

Copper CMP

Copper CMP is arguably the most complex because copper is highly reactive with a tendency to scratch, corrode, etch or form a galvanic cell with other metals in many aqueous chemistries. During copper CMP, the surface goes from first being pure copper, to a blend of two metals and finally to a composite surface with both metals and the underlying dielectric exposed; and all factors with the potential to damage copper must be controlled throughout the sequence.

Tungsten CMP

Tungsten CMP is usually run at fairly aggressive settings, which creates high pad surface temperatures and associated thermal gradients, resulting in risks to process stability. Other failure mechanisms on device structures in tungsten CMP are erosion and plug coring. With erosion, array thinning of densely spaced plugs can easily be driven by mechanical wear of the thin regions of the oxide stop layer separating the plugs. With coring, undesired etching of weak plug centers by slurry chemistry takes place, which causes high contact resistance and/or electrical opens that can impact yield and the potential reliability of the devices manufactured.

Oxide CMP

During oxide CMP, polishing starts and ends in the same material, making repeatability and control extremely important since variations in polish rate or uniformity impact oxide thickness. Having the proper pad surface texture is required for optimal removal rate and uniformity, but every cycle wears down the high points, and polishing by-products form a “glazing layer” on the pad. Pad conditioning counteracts these effects, but too much conditioning artificially shortens pad life.

STI CMP

During shallow trench isolation (STI) CMP, the goal is to fully remove oxide from all the active areas (nitride features) without breaking through nitride. The difficulty is that nitride layers are typically only a few hundred Angstroms thick, and traditional oxide slurries with steps can lead to significant yield and reliability issues.
Chingis Technology’s pFusion™ technology is now fully qualified for mass production in Semiconductor Manufacturing International’s (SMIC) 0.18μm embedded Flash memory process technology and intellectual property (IP) portfolio. The third generation of Chingis’ patented two-transistor (2T) P-channel metal-oxide semiconductor (PMOS) Flash (pFLASH™) architecture, the pFusion™ embedded Flash process offers customers a high-performance, cost-effective non-volatile memory (NVM) solution exceeding Joint Electron Device Engineering Council (JEDEC) standard endurance (up to 100K cycles) and data retention (up to 10 years), with proven yield and quality in volume production at SMIC. With its low-power consumption, small area and configuration flexibility, pFusion™ is optimized for a wide range of applications such as microcontrollers (MCUs), Universal Serial Bus (USB) keys, smartcards and devices for the automotive entertainment market.

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Cosmic Circuits is a leading provider of differentiated and silicon-proven analog/mixed-signal silicon IP for system-on-chip (SOC) integration. Recently, the company expanded its portfolio with: a high-performance audio analog front end in 65nm comprised of sigma-delta converters and class-AB and class-D drivers; a Mobile Industry Processor Interface (MIPI) standards-based D-physical layer (PHY) mixed-signal core silicon-proven in 80nm; and several new phase-locked loop (PLL) cores in 65nm, 40nm and 180nm. In addition, its WiMo analog front-end platform for wireless local area network (WLAN)/Worldwide Interoperability for Microwave Access (WiMAX)/Long-Term Evolution (LTE) is now silicon-proven in five flavors of 65nm/90nm nodes from leading foundries and is available in 40nm. Also, the company’s industry-leading, silicon-proven power regulator portfolio in 65nm/90nm/130nm/180nm has been expanded to 40nm.

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Dolphin Integration focuses on the design of virtual components of IP to enable low-power SOCs. The company recently introduced the logic circuit Motu Uta, which is the standard representative of complex logic designs. With Motu Uta, the benchmarking process of standard-cell libraries is not only objective, but fast. In addition, the company released a family of audio converters with low-power consumption, strategic for nomad audio applications. Due to its helium architecture, the converters rely on robust circuitry and offer high-quality sound. They are supported from 130nm general purpose (GP) down to 65nm low power (LP), pending the 55nm variant.

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EquipIC, a Netherlands-based company founded in 2002, provides key IC services, manages the supply chain of third parties, and compiles competitive sourcing solutions of wafers, IP, design, assembly and test services for digital, analog and radio frequency (RF) circuits. The company is foundry-independent and has partnerships with Chartered, Tower, TSMC, NXP, XFab, UMC and others. EquipIC serves customers that need help in accessing foundries, desire supply chain management support or choose to outsource the time-consuming process of selecting adequate IP vendors and service companies.

With locations in the United Kingdom, France, Israel and the U.S., EquipIC has a track record of greater than 41 ICs in full production or delivered as prototypes.

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ICsense is an IC design house offering high-quality IC design services and supplying turnkey application-specific IC (ASIC) solutions. The core business of ICsense is the design of low-power, low-voltage and high-voltage analog and mixed-signal building blocks and systems for the automotive, industrial and medical markets. In particular, ICsense has key competence in the design of high-voltage drivers, power management, energy harvesting, sensor-and-actuator interface and data acquisition ASICs. Through the expertise of its customer-dedicated senior-level engineering team, structured design methodology and stringent quality procedures, ICsense supplies its customers with leading-edge custom blocks and full systems in short time-to-market.

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Mixel released its third-generation Mobile Display Digital Interface (MDDI) solution, the MXL-PHY-MDDI. In addition, Mixel also introduced its 32KHz input frequency PLL synthesizer, the MXL-PHY-SYN-LIF-DC, which complements Mixel’s silicon-proven MIPI and MDDI PHY. The mixed-signal IP is available in multiple foundry nodes. Mixel’s mixed-signal portfolio includes serializer/deserializer (SerDes) (suitable for Peripheral Component Interconnect (PCI) Express, Serial ATA (SATA), Gigabit Passive Optical Network (GPON), 10-Gigabit Attachment Unit Interface (XAUI), Fiber Channel); mobile transceivers (MIPI D-PHY, M-PHY, MDDI); GP transceivers (low-voltage differential signaling (LVDS); double data rate two (DDR2), PCI-X, Stub Series Terminated
Logic (SSTL), High-Speed Transceiver Logic (HSTL), Consumer Electronics (CE)-ATA, CardBus, Parallel ATA; and high-performance PLL, delay-locked loop (DLL) and analog-to-digital converter (ADC) IP.

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Novocell Semiconductor is releasing a new memory product based on its patented and silicon-proven NovoBlox™ one-time programmable (OTP) memory IP at GSA’s Emerging Opportunities Expo & Conference in October 2009. Novocell’s NovoBlox is a NVM block which can be embedded in standard logic CMOS without additional process steps or post processing. NovoBlox is available in read-only memory (ROM) and serial architectures and configurable from 32bits to 8Kbits in 180nm and 130nm technologies, with scalability to 90nm, 65nm and beyond. NovoBlox is silicon-proven at Jazz Semiconductor, Tower, TSMC, UMC, Silterra and Chartered. NovoBlox serves the industrial, consumer electronics and communications markets.

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Oracle provides industry-leading business solutions for the semiconductor industry based on best-of-breed applications, middleware and open, standards-based technology. Oracle’s supply chain solution helps semiconductor companies achieve accurate consensus forecasts, optimized inventory leveling and postponement strategies, faster planning cycles and superior on-time delivery.

While Oracle’s acquisitions have certainly added value to their comprehensive solution capabilities, few have recognized the continual innovation of new functionality which stems from their annual R&D efforts, worth $3 billion annually. This fall Oracle will release a newly developed standalone product, Oracle Rapid Planning. The product will answer the “what if” questions that arise and will allow supply chain planners to react in minutes to rapidly changing conditions and exceptions in a semiconductor company’s complex, multi-tiered supply chain. Using an intuitive, new user interface (UI) and an event-based, scalable, incremental planning engine, Oracle Rapid Planning enables a real-time planning paradigm providing capabilities to simulate the impact of events and use embedded analytics to gain predictive and actionable insight. Please contact Oracle to request a demo of the new Oracle Rapid Planning.

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(W) www.oracle.com/industries/semiconductor

Fabless chip companies want faster access to yield and reliability data from their outsourced assembly and test (OSAT) providers. They also want this data to look the same, regardless of what tester or OSAT it is coming from. With the high complexity of modern ICs, the amount of data necessary to keep the supply chain running without interruption is huge. Original equipment manufacturers (OEMs) can no longer wait 24 hours for massive data logs to be transferred from the test floors.

Pintell Technologies’ TestScape™ data management system delivers these capabilities today along with continuous analysis of variance (ANOVA) data mining, early warning alerts, comprehensive data analysis, and point and click ease-of-use.

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Rapid Bridge is a technology company with a unique approach to addressing the industry’s issues of cost, performance and time-to-market. Rapid Bridge’s patented technology is integrated into three products: LiquidIP, LiquidASIC and LiquidSoC. LiquidIP is a high-performing IP portfolio that includes the smallest and highest performing IP in the industry. LiquidASIC lowers cost barriers and includes a complete collection of pre-defined ASIC platforms, interface subsystems and foundations IP. LiquidSoC provides the industry’s most cost-efficient SOCs with customer-defined die size and IP resources, regular layout structures and full programmability. With customer-focused pricing plans available, Rapid Bridge is easy to do business with.

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Committed to design quality closure with fast return on investment, Sathip IP Technologies delivers software solutions for fact-based design quality monitoring. Working within customers’ design flows, VIP Lane™ turns customers’ design practices for IP blocks or SOCs into a robust set of quality criteria and automates the implementation and documentation of design quality metrics at no extra cost in engineering time or resources. VIP Lane™ shortens time-to-market by delivering effective flow integration and on-the-fly quality monitoring at zero overhead to design teams.

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Sidense provides secure, low-cost, dense and reliable OTP memory IP for use in standard logic CMOS processes, with no additional masks or process steps. Sidense’s patented one-transistor (1T)-Fuse™ architecture (U.S. Patent #7,402,855 and others) provides the industry’s smallest footprint and lowest power logic NVM solution.

Sidense’s foundry-friendly OTP memory IP is available from 180nm to 55nm and is scalable to 32nm and below. It is available from all top-tier silicon foundries and selected integrated device manufacturers (IDMs). Customers use Sidense’s OTP memory for analog trimming, code storage, encryption keys such as High-Bandwidth Digital Content Protection (HDCP), radio frequency identification (RFID) and chip ID, medical, automotive, and configurable processors and logic.

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Solido Design Automation provides software for eliminating design loss caused by process variation in analog/mixed-signal and custom ICs. Variation Designer, a scalable and extensible solution, is used in conjunction with applications that are targeted to solve specific process variation problems. Process, Voltage and Temperature (PVT) Corner and Statistical applications packages enable designers to account for global, local and environmental variation, thereby avoiding over/under design without sacrificing efficiency and productivity. The Solve Well Proximity application enables designers to proactively solve for well proximity effects at the circuit design stage, saving design time and reducing area.

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Tensoft’s Fabless Semiconductor Management (FSM) Supplier Gateway now integrates with over 45 back-end subcontractors via multiple, flexible integration models. Tensoft FSM allows companies to simplify integration challenges across the semiconductor lifecycle by automating communication with subcontractor and supply chain vendors and to gain visibility into real-time production activity. In addition, companies can easily and more accurately track product progress from inception, production and delivery with built-in processes for data cleansing and upload validation through an always-running, always-available system. Successfully deployed at most first-tier and many second-tier subcontractors, Tensoft’s proven methodology provides a solution for enhanced data cleansing and data management, supporting the realities of supply chain integration.

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Semiconductor Equipment Service Supply Chain—Anticipating the Upturn

John Nunes, Vice President, Strategic Consulting, MCA Solutions Inc.

The technology sector took a big hit this year, with industry veterans calling this the worst recession in history. The downturn, coupled with an inventory correction across the electronics supply chain, drove a “bull whip” effect that struck semiconductor equipment manufacturers and their suppliers particularly hard.

Traditionally, the aftermarket has managed to sustain equipment manufacturers through a downturn. In previous downturns, equipment sales fell, but utilization of existing equipment remained at reasonable levels, and revenue from service contracts, consumables and other support activities remained strong. But this downturn has been significantly worse than others. As utilization and output have fallen dramatically, some chipmakers have taken drastic measures to reduce operating costs—idling machines, stretching maintenance intervals and cannibalizing existing equipment for maintenance parts.

In the short term, increasing fab utilization is likely to drive a spike in service parts demand to which equipment suppliers may be unable to respond.

However, there are actions equipment manufacturers can take now to prepare for an upturn and position themselves for long-term growth. Based on interviews with semiconductor equipment service executives and leading companies in other industries, here are four focus areas that will help equipment manufacturers position their service supply chain for short-term flexibility and build capabilities for long-term aftermarket revenue growth as the semiconductor business moves into an upturn.

▪ Use leading indicators and causal-based forecasting tools to react to changes in business.
▪ Assess the service supply chain to understand risks and develop contingency plans.
▪ Develop new service products that are suited to the changing business cycle.
▪ Develop performance-based contracts as a way to redefine your relationship with both customers and suppliers.

Apply Enhanced Forecasting Tools to Respond to Dynamic Business Fluctuations

The service executives interviewed emphasized the need for more responsive forecasting methods to enhance their ability to respond to rapid shifts in demand. They recognize that advanced planning and optimization tools are critical to building a forward-looking forecasting capability using a blend of historical time series and forward-looking, economic-causal analysis.

But most companies rely heavily on a backward-looking view to forecast, and when business levels shift, long lead times make it difficult to respond quickly. That’s certainly the story for many suppliers in the electronics industry. Now, the service supply chain presents a unique opportunity where demand is mostly driven by installed base operating levels rather than buying patterns, and operating data is often available from customers via remote data collection tools.

To be successful coming out of the downturn, equipment manufacturers need to work closely with customers to understand changes to equipment utilization, throughput levels and operating conditions, and use this information to manage their service supply chain. Unfortunately, looking out the rearview mirror at the downturn is not going to be helpful. This kind of forward-looking forecasting and planning requires more sophisticated tools that make use of...
relevant, causal data, such as laser pulses, radio frequency (RF) hours, beam hours and wafer passes, to predict ongoing demand levels. It also requires a higher level of collaboration and communication with both customers and suppliers, and the elimination of buffer stocks between customer and supplier that can make it difficult to assess true operating levels.

Several of the semiconductor companies interviewed are already using advanced planning solutions to develop causal forecasts based on operating data collected at the equipment level. While they were caught off guard by the sudden drop in demand, they were able to react quickly to minimize the impact. With a forward-looking approach to planning and frequent communications with customers, they are also in a position to react quickly when business picks back up.

If a forward-looking forecasting capability is to be effective for ongoing service supply chain management, it must rely on both customer operating data and installed base forecasts from product marketing. A number of leading companies have established formal sales and operations planning (S&OP) processes for both manufacturing and service to obtain a consensus view on expected demand and to develop a coordinated supply plan. While not commonly applied to the service supply chain, S&OP is extremely valuable, especially in highly cyclical businesses.

Assessing Supplier Risk

The ability to react to a sudden increase in service demand will hinge on the capabilities of hundreds of small suppliers. Many of those suppliers made deep cuts in personnel and capacity during the downturn, and, more importantly, competitors are probably using many of the same suppliers. Now is the time to assess the supply base’s ability to respond to an upturn and begin making contingency plans. Looking at past demand levels against fab output will provide an indication of how demand might increase with utilization. A supply chain risk assessment of critical products and processes will help identify maximum capacity levels, strategic material shortages and bottleneck suppliers. With many equipment manufacturers pursuing a single-source strategy, supplier capability is a key factor in the ability to respond to increasing demand. While it will take time to rebuild capacity, assessing the damage is the first step to recovery.

Nevertheless, understanding the capability of your suppliers is only half the problem. There is also the need to assess supplier lead times and capacity against various business scenarios and design a service supply network suited to the dynamic nature of the semiconductor industry. There has been significant consolidation across the industry, and as business levels begin to increase, companies can expect changes in customer demands for support and their willingness to pay for different levels of responsiveness. These changes may require significant restructuring of the service supply chain network and an analysis of logistics suppliers’ capabilities to deliver the required levels of customer service.

As with causal-based forecasting, advanced modeling and simulation tools are necessary to redesign and optimize a service supply chain to deal with an increased level of risk beyond what has been seen in historical cyclical variations in the semiconductor industry.

Provide Flexible Service Products Suited to the Business Cycle

If experts are right and demand exceeds capacity in 2010, there will be extreme pressure on the service supply chain to deliver spare parts and service that keeps fabs running at maximum capacity. With limited capacity for rapid growth, there are bound to be supply chain shortages as demand increases. As fab utilization increases, industry leaders must find opportunities to develop and deploy new contract offerings to suit the business cycle.

A number of the executives interviewed discussed new contract offerings suited for the downturn. These executives recognized the importance of keeping tools on contract while acknowledging that business levels demanded a dramatic change to contract terms.

To be successful in the upturn, equipment manufacturers need to design and deploy service products suited to increasing business levels. The downturn has driven massive changes to both the customer landscape and the global service infrastructure. Large semiconductor manufacturers, such as TSMC and Samsung, will look to capitalize on increased demand and response time for support services, which will be critical to this strategy. New service products and contract terms should be developed to meet this need.

![Figure 2. Designing and Pricing Service Products](image)

The key here is to engage with customers now in advance of the upturn to prepare to react to their needs with service products that add value and strengthen the relationship as partners.

Develop Performance-Based Contracts to Redefine the Relationship with Customers and Suppliers

In traditional customer-supplier relationships, customers want to lower their total cost of ownership by increasing product performance, ultimately putting more demand on the support infrastructure necessary to deliver performance and drive higher costs for original equipment manufacturers (OEMs). Alternatively, OEMs want to lower their costs and increase revenue and profits through increased service revenues and future equipment purchases. Customers are interested in seeing increased product performance and are not interested in paying for more resources and services needed to provide that service. Suppliers want to increase their profits from services (and repeat business) and lower their cost in providing support. This misalignment of incentives creates an ongoing conflict
GLOBAL MARKET TRENDS

ASIA

$180 million – Forecasted value of the Asia-Pacific’s radio-frequency identification (RFID) market in 2015. – Frost & Sullivan

$107.6 billion – Estimated value of the Asia-Pacific semiconductor market in 2010, growing at a rate of 8.2% year-over-year (YoY). This region is expected to continue to be the fastest growing in the industry. – World Semiconductor Trade Statistics (WSTS)

$209.4 million – Value of electronic design automation (EDA) products and services purchased by the Asia-Pacific region in Q1 2009, an 11.5% YoY increase. – EDA Consortium (EDAC)

$3.2 billion – Forecasted shipment value of Taiwan’s wireless communications equipment industry in 2009, down approximately 14.4% compared to 2008. – Market Intelligence & Consulting Institute (MIC)

10.2 million – Number of basic handset shipments in Taiwan in Q1 2009. – MIC

$1.4 billion – Estimated amount the Taiwan government will invest in the island’s clean-tech or green energy industry over the next five years. – EE Times Asia Article

264,000 – Number of Worldwide Interoperability for Microwave Access (WiMAX) customer premises equipment (CPE) shipments in Taiwan in Q1 2009. – MIC

$14.5 billion – Estimated production value of Taiwan’s IC design industry in 2012. – Taiwan Government

13.7 million – Number of optical disc drives (ODDs) Taiwan shipped in Q1 2009, a 28.6% YoY decrease. – Digitimes

138.8 million – Number of mobile Internet access subscribers in China in Q1 2009. – Analysys International

43% – China’s semiconductor fab utilization rate in Q1 2009, a direct result of low demand due to the global economic downturn. – iSuppli

>20% – Current percentage of China’s energy generated from hydroelectric plants. – China Daily

238.9 million – Predicted number of domestic handset unit shipments in China this year, a 7.9% increase from 2008. – iSuppli

38% – Percentage of venture capitalists who believe China has the most to gain from the current economic crisis. – National Venture Capital Association (NVCA)

23.6 million – Forecasted number of liquid crystal display (LCD) TV shipments in China in 2009. – DisplaySearch

15% – Forecasted percentage of China’s energy produced from renewable resources such as solar and wind by 2020. – China Daily

$3.4 billion – Estimated amount South Korea will spend to make its information technology (IT) industry eco-friendly over the next five years. – Agence France-Presse

62% – Expected percentage decrease of South Korea’s semiconductor equipment market in 2009. – Semiconductor Equipment and Materials International (SEMI)

$265.5 million – Value of EDA products and services purchased by Japan in Q1 2009, a 17.7% YoY decrease. – EDAC

>100 million – Number of 3G Code Division Multiple Access (CDMA) subscribers in Japan as of April 2009, making the country one of world’s leading markets for wireless data services. – Telecommunications Carriers Association

76 million – Number of mobile phone subscribers in Vietnam as of May 2009. – RNCOS

INDIA

$30 billion – Estimated revenue to be generated by India’s telecom market in 2013. – Gartner

>771 million – Projected number of mobile connections in India by 2013, growing at a compound annual growth rate (CAGR) of 14.3% from 452 million connections this year. – Gartner

49.1% – Projected percentage of India’s television shipments attributed to LCD TV shipments in 2012. The rise of LCD TV shipments in India is due to declining prices, increased consumer awareness and adoption, and an ongoing effort to promote the product by brands and retailers. – iSuppli
>100 million – Current number of CDMA subscribers in India, making it the world’s second-largest CDMA market. – CDMA Development Group (CDG)

17% – Forecasted CAGR of mobile handset sales in rural India from 2009 to 2012. – RNCOS

800 million – Estimated number of mobile subscribers in India in 2014, outperforming all other segments of the industry in terms of growth. – RNCOS

9 – Number of solar cell manufacturers currently located in India. The country has about 20 module manufacturers. – EETimes Article

EUROPE, THE MIDDLE EAST AND AFRICA (EMEA)

6.3% – Forecasted percentage increase of semiconductor shipments in Europe in 2010, reaching $30.1 billion in revenue. – WSTS

1.2 million – Predicted number of industry robots in Europe in 2011. – The European Robotics Technology Platform (EUROP)

$21.1 billion – Estimated value of East Europe’s electronics manufacturing services (EMS) market in 2013. – Frost & Sullivan

0.4% – Month-over-month (MoM) percentage increase of Europe’s semiconductor market in May 2009, following a 0.9% MoM decline in April 2009. – WSTS

5% – YoY percentage decrease of Europe’s automotive market in May 2009. – VDA

$350 million – Russian investment in European X-ray laser research. Russia and Germany contributed the most funding to the research. – EE Times Europe Article

$223.2 million – Value of EDA products and services purchased by the EMEA region in Q1 2009, a 15.9% YoY decrease. – EDAC

$219 million – Amount of funding Israeli venture capitalists invested in Israeli companies in 1H 2009, a 48% decrease from $423 million in 1H 2008. – Israel Venture Capital (IVC) Research Center

122 – Number of Israeli high-tech companies that raised a total of $279 million from local and foreign venture capitalists in Q2 2009, a 40% decrease from $465 million raised by 115 companies in Q2 2008. – IVC Research Center

$544 million – Amount of funding raised by 215 Israeli high-tech companies in 1H 2009, a 50% decrease from $1.1 billion in 1H 2008. – IVC Research Center

THE AMERICAS

$494 million – Value of EDA products and services purchased by the Americas in Q1 2009, an 11.6% YoY decrease. – EDAC

37% – Percentage decrease of the U.S. automotive market over the first five months of 2009. In May 2009, sales for light vehicles in the U.S. declined by nearly 34% to 923,000 units. – VDA

$288.5 million – Value of orders posted by North America-based manufacturers of semiconductor equipment in May 2009. – SEMI

137% – Current growth rate of the netbook market in North America. The netbook market’s growth rates in Latin America and the EMEA region are 88% and 81%, respectively. – DisplaySearch

8.6% – Unemployment rate of U.S. electronic engineers in Q2 2009, nearly doubling when compared to the previous quarter. – Institute of Electrical and Electronics Engineers (IEEE)

$3.6 billion – Forecasted value of North America’s semiconductor equipment market in 2009. Japan and Taiwan will follow with $3.0 billion and $2.4 billion, respectively. – SEMI

$1.0 billion – Estimated amount invested in North American fabs in Q2 2009, showing increasing investment compared to other regions. – SEMI

67% – Projected percentage of the U.S. that will have achieved grid parity, the point at which electricity generated from photovoltaics is equal in cost or less expensive than grid power, by 2015. – The Prometheus Institute for Sustainable Development

$34.2 billion – Forecasted value of the Americas’ semiconductor market in 2010, a 5.9% YoY increase. – WSTS

270,000–335,000 – Projected range of electric cars in the U.S. within the next five years. – CNW Research

6.4% – Forecasted percentage decrease of North America’s telecommunications revenue in the next two years; revenue growth is expected to rebound by 14.4% during 2011 to 2012. – Telecommunications Industry Association (TIA)

11% – Annual growth of the amount U.S. families will spend on consumer electronic devices for students returning to school. – National Retail Federation (NRF)

20% – Expected percentage of U.S.-generated electricity to be supplied by wind power by 2030. – U.S. Department of Energy (DoE)

$5.27 billion – Amount of funding invested in 595 deals in the U.S. in Q2 2009, a dollar amount increase of 32% from Q1 2009. – Dow Jones VentureSource

300,157 – Number of motor vehicles sold in Brazil in June 2009, an increase of 21.5% from May 2009. – RNCOS

$210 million – Amount invested by Brazil’s government in the country’s first chip design center. – Electronic Design Article

19.8% – YoY growth rate of Latin America’s notebook PC market in 2009, which is expected to reach $5.4 million. – DisplaySearch
Improving ASIC Design Schedule Estimates

Jim Bailey, Chief Operating Officer, Alchip Technologies Inc.
Bob Eisenstadt, Principal Engineer, Alchip Technologies Inc.

Application-specific IC (ASIC) design schedule estimates are often inaccurate, which impacts projections of design costs, product release dates and product revenues. Many ASIC suppliers have program management databases that are used to help estimate future ASIC design schedules. Most ASIC design schedule estimates assume there is a strong correlation between time to completion and design complexity, as measured by gate count, memory bit count and clock frequency. An internal study of ASIC design projects completed by a fabless ASIC supplier in 2008 has also revealed a strong correlation between the time from final netlist to Graphic Design System II (GDSII) release and the maturity of the company that is providing the netlist. For example, it took almost twice as long for Tier 3 companies' designs to progress from final netlist acceptance to GDSII release than it did for designs of similar complexity that were provided by Tier 1 companies. This article will present project and schedule data, discuss reasons for Tier 1 versus Tier 3 schedule variations, and propose heuristic rules to help improve schedule estimation.

The ASIC project schedule data presented in this article is based on final netlist-to-GDSII database release for projects completed by a single fabless ASIC supplier during 2008. The ASIC supplier's 2008 project database included 28 projects, of which 19 were from Tier 1 companies, four from Tier 2 companies and five from Tier 3 companies. Tier 1 companies are classified as large, well-established companies with major divisions and/or product groups providing supporting multiple product lines of varying maturities. Tier 3 companies are classified as small start-up companies that are focused on developing and introducing new technologies and products. Tier 2 companies lie somewhere between Tier 1 and Tier 3, in terms of size, product maturity, product line breadth and so forth. Please refer to Table 1, which provides design and schedule data that has been averaged across companies in each tier.

Table 1. Time for Designs from Final Netlist to GDSII

<table>
<thead>
<tr>
<th>Tier</th>
<th>Number of Companies</th>
<th>Process Technology</th>
<th>Average Gate Count</th>
<th>Average Frequency</th>
<th>Average Bit Count</th>
<th>Average Final Netlist-to-GDSII Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 1 Projects</td>
<td>19</td>
<td>65nm (10), 90nm (9)</td>
<td>3.5 Million</td>
<td>219MHz</td>
<td>2.8Mbit</td>
<td>31 Days</td>
</tr>
<tr>
<td>Tier 2 Projects</td>
<td>4</td>
<td>90nm (3), 180nm (1)</td>
<td>2.1 Million</td>
<td>132MHz</td>
<td>1.2Mbit</td>
<td>45 Days</td>
</tr>
<tr>
<td>Tier 3 Projects</td>
<td>5</td>
<td>90nm (4), 130nm (1)</td>
<td>3.9 Million</td>
<td>203MHz</td>
<td>76Mbit</td>
<td>61 Days</td>
</tr>
</tbody>
</table>

The average final netlist acceptance-to-tapeout time for Tier 1, Tier 2 and Tier 3 companies was 31 days, 45 days and 61 days, respectively. The differences between Tier 1 and Tier 3 companies, including schedule delays, are more pronounced than differences involving Tier 2 companies. Therefore, this article will largely focus on analysis and comparison of Tier 1 and Tier 3 companies, as their differences are more instructive.

The data in Table 1 shows that design complexity, which is largely based on average gate count, average memory bit count and average clock frequency, is reasonably consistent across the different company tiers. The average Tier 3 gate count is 11 percent higher than the average Tier 1 gate count. If one assumes linear scaling, this would account for about three days of additional schedule delay. The average memory bit counts in Table 1 show substantial variation across the different company tiers. However, memory instance counts are relatively small, so memories have a large impact on the floor plan and die area, but would only add a few more days to the average Tier 3 schedule due to increased floor planning efforts and tool run times. The average Tier 1 clock frequency is only 8 percent greater than the average Tier 3 clock frequency, which is too small to have a significant impact on design turn times. On average, Tier 1 designs use more advanced process nodes than Tier 3 designs. This may result in minor increases in Tier 1 design cycle times due to more extensive design verification requirements, and minor increases in Tier 3 cycle times due to greater timing closure challenges with older process nodes. Overall, the differences between average Tier 1 and Tier 3 designs are too small to explain the 30-day gap between Tier 1 and Tier 3 final netlist-to-GDSII release times.

All the data in Table 1 comes from the same fabless ASIC supplier; therefore, all projects used the same design methodology and design flow with similar gate utilization and routing density targets. Furthermore, the design implementations were done with similar design teams and staffing levels that were led by the same program management team. It follows that all major design complexity and design implementation variables for Tier 1 and Tier 3 companies are too similar to explain the differences in final netlist-to-GDSII release schedules. The only remaining major variable that can explain the scheduling differences is the tier of the company releasing the final netlist. The next step is to explore the differences between Tier 1 and Tier 3 companies and their engineering teams to understand the underlying causes for the large differences in final netlist-to-GDSII release times.

There are countless major differences between Tier 1 and Tier 3 companies, including their design teams, so this article will focus on the differences that influence netlist stability and quality, which has a huge impact on netlist-to-GDSII schedules. Many Tier 1 companies' projects are based on earlier versions of existing projects plus enhancements and upgrades, which provides a stable project baseline and path to develop a high-quality netlist. Tier 1 companies often have internal physical design teams, which enables them to choose which
design projects should be supported in-house and which should be outsourced to ASIC suppliers. Tier 1 internal physical design teams are much more likely to support the development of their company’s most advanced design projects since these require tight engineering feedback loops. Projects that involve enhancements and/or upgrades of existing designs are more suitable for outsourcing, which means Tier 1 companies are often positioned to outsource designs that have relatively clean, stable netlists. Most Tier 1 companies also have comprehensive project definition and acceptance criteria, where project features, specifications and target market requirements are carefully reviewed and approved. Once a Tier 1 project is approved, it is very difficult to make major design changes. This results in a more stable set of design objectives, which further improves the stability and quality of Tier 1 netlists. As previously stated, most Tier 3 companies are start-ups that develop and deploy new products and technologies. By definition, new products and technologies can’t rely heavily on pre-existing products and solutions. Therefore, unlike many Tier 1 companies, most Tier 3 companies don’t have the luxury of leveraging existing design projects. Most Tier 3 companies also can’t justify the investment in internal physical design teams and electronic design automation (EDA) place-and-route tools. Thus, the physical design work from most Tier 3 projects is outsourced regardless of design and technology maturity. To develop the customer base for their new products and technologies, small Tier 3 companies need to be nimble and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs?

For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible. For example, what would happen if critical customer XYZ agrees to sign a contract to purchase major quantities of ASICs from start-up ABC, but only if ABC’s ASIC targets a different XYZ agrees to sign a contract to purchase major quantities of ASICs? and flexible.
Though new to the industry, GLOBALFOUNDRIES is already striving to revolutionize the foundry industry and shape the future of the supply chain with its innovations in leading-edge technology, global presence and strong financial backing. In my interview with industry veteran Doug Grose, chief executive officer of GLOBALFOUNDRIES, we discussed how GLOBALFOUNDRIES’ advanced technologies and fab locations give the company a unique, competitive edge; how the company will prevail in tough economic times; why its supply chain model benefits its customers; the significance of its partnership with IBM; and much more.

— Jodi Shelton, President, GSA

Q: GLOBALFOUNDRIES was only established in March 2009, but industry pundits already forecast GLOBALFOUNDRIES to be a strong competitor to established foundries. However, it is becoming increasingly difficult for even established foundries to entice fabless companies that sell large volumes of product and have instituted a partnership on process technology development to switch foundry providers. While it may be easy to attract small fabless companies, as they cannot afford to do their own process technology development, how does the company plan to draw large customers who are already loyal to their current foundries?

A: Since launching GLOBALFOUNDRIES, we’ve had the opportunity to engage with many of the world’s largest fabless and fab-lite companies; and it is very clear that these companies desire more choice at the leading edge. GLOBALFOUNDRIES will be able to offer a strong alternative for advanced technologies. Our past experience as an integrated device manufacturer (IDM) gives us a unique set of capabilities in understanding how to operate as an extension of our customers’ operations, and as GLOBALFOUNDRIES, we can now harness this for the entire market. The microprocessor segment is typically the first to utilize the world’s most advanced process technology. Our experience ramping these technologies in high volumes and at mature yields gives us a tremendous advantage over our competitors at the leading edge.

In addition to our leading-edge technology, the talent we possess will also attract customers, large and small. GLOBALFOUNDRIES believes that talent is critical to technology innovation, manufacturing and the future of the foundry business model to effectively serve customers. Our company will be able to unleash our manufacturing excellence into the foundry market for our customers because we are well positioned to leverage global talent and connected to patient capital.

Q: Many IDMs, such as former IDM AMD, are switching to an outsourced business model to cut costs. How will GLOBALFOUNDRIES’ supply chain ease this transition for these companies? What benefits has AMD reaped from the spin-off?

A: GLOBALFOUNDRIES has taken steps to build our own independent supply chain infrastructure optimized for a multi-client environment. This unique infrastructure integrates with our customers’ environments, becoming an extension of their supply chain. We have more work to do as we finish our infrastructure build-out in 2H 2009, but I am pleased to say that we’re off to a strong start.

AMD’s “asset smart” strategy has allowed the company to increase its focus on silicon design, and its execution continues to improve. The company brought its recent six-core server central processing unit (CPU) “Istanbul” to market ahead of schedule and has a strong product and platform line-up for 2H 2009.

Q: When GLOBALFOUNDRIES established itself in March 2009, the recession was well underway. Did GLOBALFOUNDRIES have any reserves about entering a struggling market, or did you see it as an opportunity? How will the company continue to build its business in this challenging climate?

A: We saw 2009 as an optimal time to launch the company and invest in the market. Creating a joint venture like GLOBALFOUNDRIES is not a short-term decision. In fact, it is the result of years of strategic planning based on a long-range view of the challenges and opportunities in the industry. Because of that strategic planning, and with the help of our investors, we have been able to find advantages in the current economic environment to build our business by investing in talent, tools and technology—at a time when most companies are not able to. For example, GLOBALFOUNDRIES is investing in capacity with a new state-of-the-art $4.2 billion manufacturing facility in upstate New York; increasing capabilities at our Dresden, Germany facility; and pursuing an aggressive process technology roadmap that will lead the foundry industry.

As a committed investor and customer, AMD will drive high-volume manufacturing at the leading edge. And with ATIC, we have a savvy investor with the capital resources necessary to ensure we can make long-term investments in capacity and technology to stay on the leading edge and serve our customers for years to come.

Q: With the world’s top foundries primarily based in Asia, GLOBALFOUNDRIES’ fab locations in Dresden, Germany and Saratoga County, New York have set a new precedent in the pure-play foundry industry. Compared to its Asian rivals, what advantages do the fab locations...
Q: In Q1 2009, Magma Design Automation regained its momentum, registering 11 percent quarter-over-quarter (QoQ) revenue growth. In the second half of 2009, what initiatives will Magma implement to sustain its profitability, set the company apart from its competitors and improve its performance within its supply chain? What benefit does participating in the analog/mixed-signal market provide the company?

A: Magma Design Automation expects to be profitable during the next three to four quarters. Even if today’s difficult economic climate continues, we have already positioned ourselves to remain stable and lucrative in 2H 2009. However, if the economy worsens, we will need to take the necessary actions to sustain our profitability. Over the past year, Magma has developed software tools that have great usability and require the effort of fewer engineers, thus enhancing the productivity of our customers’ design processes. This technology achievement has allowed us to gain many customers and differentiate from competitors as we strive to provide the most user-friendly tools that produce profitable chips for our customers. During the next few months, we plan to interact with many more companies to further promote the performance advantages of our products.

Magma views the analog/mixed-signal market as the future of chip design as it is necessary in emerging semiconductor applications such as smart grid technology. The big chips that the industry typically produces cannot be used in these new applications which require that designs be combined with diodes, analog circuitry, etc. We actually first discovered the demand for the analog/mixed-signal market when our key customer, Texas Instruments, moved to analog/mixed-signal. In the past, Magma centered its efforts on wired and wireless communication to support Texas Instruments in this market. Similarly, when Texas Instruments voiced a few years ago that they would be getting involved in the analog/mixed-signal space, Magma heavily invested in it. We have already developed key analog/mixed-signal design solutions and aim to be a technology leader in this market.

Q: As companies continue to expand their global operations (e.g., nearly 50 percent of Magma’s employees are located in Asia, Europe and India), their supply chains become increasingly complex to manage. How does Magma streamline its global operations to produce quality products and minimize risk? What global markets are currently proving profitable for Magma?

A: When Magma started implementing company changes to reduce costs, one significant task we undertook was reassessing our global operations. We previously had employees located in multiple countries, such as China, India and the U.S., working together on one product. However, communication amongst the employees in these regions was somewhat disconnected. Now, we have realigned our product development model to have only one region focus on a project, and have moved some of our technology leads from the U.S. to different countries to facilitate product development. For example, our Titan platform is now completely developed by a team in India instead of having portions of the product developed by U.S.- and Europe-based employees, as was the case prior to the reassessment. In addition, if a team does not have the leadership required to execute a superior product, we will pull the project out of that region. With focused teams, we have better control over technical and economic aspects of product development, which is especially important in today’s economy.

Although the U.S. has been a tough market, it has always been our most profitable. My current focus is to build our business in Asia, specifically Japan. So I will be spending a great deal of time in Japan to increase our presence. And we are happy to see our market share in Europe improving.

Q: In Q4 2008, the EDA industry experienced a 17.7 percent year-over-year (YoY) revenue decrease according to the EDA Consortium. Industry experts attributed the revenue decline to: (1) vendors shifting from term licensing to time-based licensing and (2) the misguided attempt to transform Cadence into a dominant vendor. With the industry looking to bounce back, what structural changes must the EDA industry undergo to re-establish growth? Do you see the industry transitioning from its current business model to a traditional software-based business model?

A: The decline of the EDA industry is not solely a result of the licensing shift and Cadence failing to become a dominant vendor. The current practice of the large EDA companies engaging in “primary vendor” deals is greatly responsible for the market downturn. These vendors are shooting themselves in the foot...
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onsider the revenue “hockey stick.” Unfortunately, it has been widely accepted as a way of doing business, and many businesspeople go to ridiculous lengths as the end of each quarter approaches to find a way—any way—to ship promised revenue. It’s not unheard of to ship a third or more of a quarter’s total revenue in the last two or three weeks. Sadly, although executives typically understand the grim realities of demand uncertainty, many still insist on driving to short-term financial results that are disconnected from the realities of their markets and their customers. The hockey stick may be a part of the conventional wisdom, but it’s time executives come to recognize its negative impact on internal operations and their organization’s long-term performance. It’s time for a new wisdom.

The Laws of Linearity

When it comes to the customer-supplier relationship, some accepted views of “linearity” have become ingrained. These hold that: linearity is a measure of how steady-state your internal operations run; such a steady operating rate is good, regardless of customer product consumption; and your customers are on the hook to help you achieve this kind of linearity. These views would be fine except: it’s not; it’s not; and they’re not.

Instead, here are some—perhaps heretical—revised “laws of linearity” that you should consider when planning your performance strategy:

▪ The First Law of Linearity: Your linearity is the degree to which product delivery exactly matches customer product consumption. As in analog electronics, linear means a proportional response, not a flat line. Your customers’ product usage can be steady from day to day, or it can be a wild wiggle—it doesn’t matter.

▪ The Second Law of Linearity: If you want to improve linearity, operations need to be aligned with customer product consumption as precisely as possible.

▪ The Third Law of Linearity: Stability, which reflects how steadily you can run operations, depends on your customers’ lineairies, their customers’ lineairies and so on.

Meeting the Numbers at Any Price

Following the hockey stick approach—essentially anything you do to “meet your numbers” when linearity says the natural outcome is otherwise—tends to make things worse in the long haul.

For example, say you planned and publicly announced to sell $13 million in product this quarter, and now stockholders and analysts are waiting in ambush. Meanwhile, the people you sell to aren’t helping you meet your numbers. With two weeks to go in the quarter, you’re only at $9 million. At this late stage, if you’re to nail it, you have to figure out how to take what was to have been a $1 million a week run rate and double it.

At this point, you possibly don’t care why you are not tracking to projections in the first place. The sole remaining objective—in this example—is to hit your numbers. Essentially, your position is that as long as you can nail your announced target by pushing your goods across the financial line between you and your customers, it doesn’t matter what happens with these goods on the other side.

But, it does matter. In the long run, what happens to your products when they leave your warehouse matters more than almost anything else. As we examine why, let’s agree on some working assumptions:

▪ Your customers can do basic math.

▪ Your customers try to operate their concerns in response to their customers’ demands.

▪ Whatever your customers are doing to position you against your competitors, the competitors feel the effects just as much.

▪ If your customers have inventory, then they have more choices than when they actually need your product to keep their lines going.

Whatever you sell or ship beyond your customers’ actual product usage accumulates over time. When facing their own customers, your customers’ realities do not change as a result of the excess stock you manage to push to them. If they bought something from you that they didn’t need right away, then you must assume they won’t sell it to their customers any faster than they were prior to the sell.

So, let’s say you were successful in grabbing those last-minute sales to meet your quarterly numbers. Congratulations on an illusory victory; you may feel you have won a battle, but perhaps you have lost ground in the war. If you’ve pushed more inventory over to your customers than they actually need, then your problems have only started.

For one thing, your customers have moved cash, which earns interest, into inventory, which doesn’t (and, of course, costs money to own). It’s also a zero-sum game; your asset picture improved in the opposite direction. And everybody knows what happened; both you
and your customers can calculate how much interest and holding cost benefit was transferred to your side.

So what did you give up to get what you needed? Your math-savvy customers would not have agreed to a last-minute buy without some compensating financial concession. You probably capitulated on pricing. Most likely, you accelerated your forward-pricing roadmap to give them next quarter’s pricing early.

What kind of dollars are we talking about? Well, when only looking at weighted average cost of capital (WACC)—usually around 12–15 percent—and ignoring other holding costs, let’s say you moved an extra $1 million into your customers’ warehouses that they will let sit for an extra three weeks. At 15 percent WACC, they incurred a cash expense of almost $9,000; and your premature access to revenue earned you similar interest income. Your quid pro quo was probably to knock down your prices by nearly 2 percent. In fact, considering that holding costs are substantially higher than WACC, it’s probably a fair bit worse than that. Your margins took a whack they probably didn’t need. Worse, you also accelerated the forward erosion for coming quarters.

And now, because it took more units to meet the revenue number at the reduced price, you further amplified the quarter-end fire drill in your factories and warehouses. Additionally, you blinded yourself as the next quarter begins. Your customers’ demands may be keeping pace, slowing or accelerating, but you’ll have no idea what’s happening until they burn through the inventory you essentially paid them to take.

You don’t know what your customers’ actual demands are, so your production is now even more based on speculation rather than triggered by actual pull signals from your customers. Since you don’t have the surge capacity to wait, you have to keep your lines running to support next quarter’s projection. You may build the right stuff, you may not. Welcome to next quarter’s hockey stick—you created it.

The Fourth Law of Linearity: Linearity is Cumulative

When you take the long view of your customer relationships, it should become instantly clear that, over time, your customers will not cumulatively buy more than they use. Therefore, the short-term manipulation done to dress up your numbers only degrades long-term performance. The hockey stick will never be a true friend.

If you begin the quarter with inventories in equilibrium (pacing your customers’ consumption in a way their natural operating models require for reasonable operation), then you’re going to be in good shape. If you’re either above or below that level, then you’re exposed to misleading signals from your customers.

Pushing inventory is certainly bad for you, but what does it mean for your customers? Some make the argument that your customers benefit from sitting back and letting you do this, and are in fact encouraging it. Perhaps that’s true, but the net effect of the hockey stick mentality is to exacerbate both oversupply and shortage events in the supply chain. The presence of “push” inventory in the supply chain amplifies the bullwhip effect, increases the tie up of overall working capital, and degrades the financial health and operating performance of all participants. Whether your customers exhibit this behavior or not, it remains true that it’s in their long-term best interests to promote linearity throughout the supply chain.

It’s traditional to bewail your customers’ role in this relationship, as if they’re gaming you rather than the other way around. It is, of course, true that they have played along—but only because you made it attractive. The dynamics of your relationship have been based on fiction that was introduced in previous quarters, and now that fiction is going to have to be excised. Turning this around is going to involve some discomfort on both sides, as does any change in the dynamics of an important relationship. You’re going to have a tough quarter, and maybe more than one.

Axing the Hockey Stick

It is possible to kill your hockey stick, and companies have done it successfully. It can be grueling, but the benefits are plainly evident. You can:

▪ Free up large sums of working capital while writing down less inventory.
▪ Mitigate price erosion and put extra support under your margins.
▪ Operate your supply chain with more clarity and finally be able to implement pull methods that simplify the process.
▪ Improve performance to match your customers’ needs and all the while provide more reliable information to your own suppliers.

The basic model for working your way out of the hockey stick quagmire is simple, but admittedly hard:

▪ Engage your customers. When you are trying to change the game, you have to articulate to your customers clearly and tenaciously how you propose to improve the value proposition from their perspective, not degrade it. If necessary, you have to help them do their own metrics on: the effect the status quo is having on their working capital and holding costs, impacts on warehouse and factory performance from unnecessary stock fluctuations, and the cost of non-value-added activities that transpire between you and them.

▪ Address the addiction within. Somewhere in the C-suite is the mindset that, once established, expectations must be met or beat. One of the most frequent byproducts of this is the “top down forecast”: when the normal demand planning process fails to roll up to a suitable number, the mandate comes from on high to find a place to put the subtract answer. This can occur at any time, but gets progressively more manic and unrealistic as quarter end looms. There is no getting around this—fixing the hockey stick means letting demand speak for itself.

▪ Save yourself from yourself. Implement consignment or vendor-managed inventory (VMI) programs with your customers so you know you’re getting your demand signals from their factory floors. Implement internal processes around optimizing the supply chain to support the pull behavior, not the “build this now because we may need to build that later” mentality. Aggressively pursue cycle time reduction and product postponement/rationalization so you are better positioned to execute just-in-time. Get ruthless about inventory.

▪ Become the model of consistency. Present a stable face to your customers so their behavior towards you, over time, is based on firm expectations. If the best lead times your operating model can support are four weeks or longer, then don’t send a mixed message by moving them in or out constantly. Make sure your external face matches your true capabilities, and hold the line.
Economic events of the past year have led many high-technology companies to examine their assumptions about growth in their own industries. Total market size, growth rates as well as product and pricing strategies are all under revision as individuals and enterprises adapt to a new set of economic realities. Global manufacturing strategies in support of an enterprise’s larger objectives should be examined and revised, if necessary, at the same time. The means and mechanisms necessary to provide support to corporate objectives should be identified and quantified wherever possible. Risk mitigation from possible adverse but foreseeable events should be a key element of this analysis as well.

A well thought out strategy for a global high-technology company to mitigate risk in its manufacturing environment includes geographical diversification of manufacturing sites. This diversification needs to be more than multiple sites in a single area; the strategy should look broadly enough at potential risk to expand the scope to locations that span multiple continents. For many high-technology companies with a concentration of manufacturing capacity in Asia, diversification must include examining other low-cost venues around the world.

In any review of low-cost manufacturing environments outside of Asia, Mexico should be considered as a viable alternative. There are a variety of reasons that make Mexico an attractive location for high-technology manufacturing: talent, educational infrastructure, preferred tax structures, physical infrastructure, intellectual property, labor costs, free trade agreements (FTAs) and exchange rate risk.

**Educational Infrastructure**

To meet the needs of high-technology manufacturing in industries as diverse as aerospace, automotive, medical device and semiconductor, Mexico has devoted significant financial resources to the development of world-class universities and technical training programs, encouraged and subsidized by state and federal government, to improve the human infrastructure in Mexico. International companies worldwide now recruit engineers and technicians from Mexico. With a very young population (65 percent under age 30), Mexico provides both the quantity and quality of workforce essential for prosperity in the coming decades.

**Preferred Tax Structures**

Mexico has long provided foreign-owned enterprises with preferential tax structures. The Maquiladora tax program has been responsible...
for reducing the tax profile of foreign-owned companies operating in Mexico, making it very competitive with Asian countries offering “Pioneer Status.” The net result is that capital-intensive operations can be profitable here. More profitability repatriated to the parent organization can provide capital for the development of new products, programs and processes to improve the enterprise’s competitive position.

Physical Infrastructure
Until recently, Mexico had little to recommend it in the way of effective, world-class physical infrastructure. Today, Mexico has privately financed and constructed science parks with world-class physical infrastructure. State-of-the-art roads, power, water and telecommunication utilities are available at prices competitive with any worldwide to support high-technology facilities. Abundant, clean power and water are also provided at competitive rates for companies using a semiconductor-based process.

Intellectual Property
Intellectual property theft has long been an issue with high-technology companies. One of the conditions of the North American Free Trade Agreement (NAFTA) required Mexico to both strengthen and enforce their laws regarding intellectual property rights. Mexico now provides a secure intellectual property environment that rivals the U.S., Canada and Western Europe.

Labor Costs
Since 2005, Mexico has become one of the most cost-effective countries in the world for U.S. companies to conduct manufacturing operations. Devaluation of the Mexican Peso by 20 percent relative to the U.S. Dollar in the past year has more than offset any wage growth that occurred over the past 3–4 years. Simply, labor costs in Mexico are at historic lows when denominated in dollars. And the productivity of the high-technology labor force in Mexico is equal to that of any in the world. A company can receive all these benefits with no requirement for a labor union.

And it isn’t only direct labor costs that have fallen to historical lows. Indirect labor costs for process improvement engineering and research and development are significantly lower than they ever have been before. With Mexico’s manufacturing and engineering talent located in the U.S. Central, Mountain and Pacific time zones, an additional advantage becomes apparent: Communication between the U.S. headquarters and/or market and the “near-sourced” manufacturing facility can be conducted in real time. No longer do designers, engineers and managers have to deal with 12- to 16-hour time differentials. When an issue arises that must be dealt with promptly by the factory, one can rest assured their management team is on the same schedule. And travel between the U.S. and Mexico can be done in hours rather than days.

Over the past two or three years, labor rates in many parts of Asia have begun to increase at 8–10 percent annually. Asian governments that once downplayed the role of the labor union are becoming more union-friendly. As a result, labor costs, fringe benefits and the resulting regulation of the labor market have driven labor rates up in Asian markets at close to double-digit rates for the past few years. With Asian governments focusing on growing a larger middle class, policy in Asian countries will continue to support wage growth and more restrictive work rules in the foreseeable future.

Free Trade Agreements
Most individuals are aware of NAFTA, the FTA eliminating duties between Mexico, Canada and the United States. What most people don’t realize is that Mexico has FTAs with 43 nations worldwide. In addition to North America, Mexico has FTAs with the nations of the European Union, most of Latin and South America as well as Japan. An FTA is also in process with Korea.

As a result of Mexico’s leadership in negotiating FTAs, it is uniquely positioned to be a location for low-cost manufacturing and duty-free distribution for the world’s products to the U.S. and for U.S. products to the remainder of the world. In addition, to bolster their position as a key venue for high technology, Mexico has begun to emphasize the enforcement of intellectual property rights whether domestic or foreign-owned. Their position on intellectual property protection is in stark contrast to much of Asia.

Exchange Rate Risk
The economies of the U.S. and Mexico are strongly linked. Mexico is the United States’ third-largest trading partner only behind Canada and China. The United States is Mexico’s largest international trading partner. The Mexican economy is highly dependent upon the health of U.S. businesses. Historically, the peso and the dollar have moved together within a relatively small range. This makes labor and services denominated and paid in pesos very stable in terms of dollar cost.

Contrast this experience to exchange rates in Asia. Many Asian currencies have appreciated relative to the dollar at 15–20 percent over the past three years. Leading economic predictions call for continued devaluation of the dollar relative to Asian currencies. Partly due to anticipated domestic strength in these economies as they recover from the world-wide recession and in part due to U.S. domestic monetary policy that has added significant cash to the system with the anticipation of U.S. inflation and resulting devaluation of the dollar, these trends seem unlikely to reverse themselves in the short term. In fact, the greater likelihood is that devaluation of the dollar against major world currencies will occur at an increasing rate as U.S. monetary policy continues to provide stimulus to the domestic economy.

Conclusion
Combine all the attributes previously listed with governmental agencies at both the state and federal level that understand and appreciate the importance of business in driving economic well-being for their constituents and you have what could be considered an ideal environment for high-technology companies. State and federal governments are willing to back their commitment to recruiting new opportunities to Mexico by providing a variety of cash grants and other incentives. All in all, the combination of quality, cost and location is hard to beat.

About the Author
DJ Hill is the co-founder of Silicon Border and serves as the company’s chief executive officer and co-chairman of the board. His past industry experience includes serving as a division vice president and general manager for National Semiconductor, and as a C-level executive with Cerprobe, InterConnect and MCT. He spent 12 years transferring semiconductor technology to Asia, and eight of those years living in Asia. Hill has served internationally on several industry boards, is a public speaker and published author on semiconductor industry issues. Hill earned his bachelor’s of science degree in industrial engineering from New Mexico State University.
Valuable and sensitive information is stored on carriers, such as discs, memory devices and embedded devices (e.g., bank passes, smart cards and radio frequency identification (RFID) tags), or is transported over a network to the end user. To protect this information, cryptographic techniques, such as encryption and signing algorithms, are used. The algorithms used are often made public, but use a secret key that is stored securely in the system.

If the secret key is leaked, the system cannot guarantee protection. Encryption with today's state-of-the-art cryptographic algorithms works well. However, since the secret keys are stored in everyday objects, such as smart cards, attackers can easily subject such objects to physical attacks with various tools to gain access to the secret keys. Although these tools (e.g., optical, atomic force, scanning electron, laser scanning and confocal microscopes, focused ion beams and laser cutters) are sophisticated, they have become more and more widespread and affordable for many parties.

The traditional methods of protecting secret keys are approaching their limits and increase both cost and time-to-market. A low-cost but strong secret key storage technology is a critical link in an affordable but strong security system. It is a necessary requirement for ICs in smart cards, defense and governmental applications, e-health systems, passports, etc. that protect valuable and sensitive data and upon failure would cause not only huge financial losses, but also brand and reputation damage.

Limitations of Current Key Storage Mechanisms

Off-chip storage of a secret key is vulnerable to an attack that taps the bus between the external memory and the chip. Therefore, current key storage mechanisms store secret keys on the device that carries out security operations.

A number of approaches exist to permanently store keys in a device: read-only memory (ROM) storage; fuse-based storage mechanisms (e.g., poly fuses, laser fuses, e-fuses and antifuses); floating gate-based storage mechanisms (e.g., Flash, electrically erasable programmable read-only memory (EEPROM) and erasable programmable read-only memory (EPROM) storage cells); and battery-backed volatile memory mechanisms (e.g., battery-backed random access memory (RAM)). Each of these approaches has strengths and weaknesses in terms of security, cost, time-to-market, flexibility, reliability and trust throughout the supply chain.

Security

The fundamental security flaw of all the approaches previously mentioned is the permanent presence of a key in digital form within the device. Even when the device is powered down, a determined attacker has a range of physical tools available to gain access to the key.

Cost

Floating gate-based technologies require six to 10 additional mask steps, adding significant cost. These technologies as well as antifuse-based techniques require a charge pump, which also adds to the cost of a device. Many non-volatile memory (NVM) technologies have a potentially negative impact on yield, which may only become apparent late in the supply chain for one-time programmable (OTP) memory.

Time-to-Market

With the exception of battery-backed RAM and ROM, the memory technologies previously mentioned are non-standard components and are options only in later generations of a new process node. This can cause a substantial delay in time-to-market.

Flexibility

ROM and EEPROM, as well as fuse-based memories, are OTP and hence do not allow for updates in the field.

Reliability

Battery-backed RAM is limited by the battery; when the battery is no longer functional, the key is lost. Flash, on the other hand, has reliability problems at high temperatures due to charge leakage.

Supply Chain Trust

While all the existing key storage approaches seek to protect against one aspect of counterfeiting—making a copy or clone of a device—they do nothing to address the other aspect of counterfeiting: manufacturing overproduction.

A New Approach Needed: Hardware Intrinsic Security

There is clearly a gap in hardware security that is playing into the hands of determined attackers. To counter this increasing threat, a radical new approach to key storage is needed, in which:

- The key is not stored in digital form on the device.
- The key is extracted from the device only when required.
- The key, once used, can be removed from all internal registers and memories.

A new approach that extracts the key from a device’s intrinsic properties without being stored fulfills these criteria and overcomes many of the current approaches’ limitations. The implementation of such an approach—called hardware intrinsic security (HIS)—eliminates the need for technology-dependent components or embedded NVM.

HIS has the following advantages in terms of security, cost, time-to-market, flexibility, reliability and trust throughout the supply chain:
Security
An approach centered on the device’s intrinsic properties offers an unparalleled security level since the key is not present when the device is switched off. HIS provides key storage without storing the key.

Cost
HIS does not require additional mask steps or additional analog components, reducing cost.

Time-to-Market
HIS is ready to use with the newest process nodes and without extensive supply chain qualifications needed to implement options such as NVM. Some HIS implementations use standard components which do not require test silicon to qualify the solution on specific process nodes.

Flexibility
HIS keys are field-upgradeable.

Reliability
The HIS approach offers reliability against a wide range of external influences such as temperature and voltage variations and humidity.

Supply Chain Trust
The device-unique nature of the HIS approach enables a chip activation step to make the chip functional in its system environment. Reporting capabilities can protect against overproduction and provide secure relationships throughout the supply chain.

The Key to HIS: Physical Unclonable Functions
A physical unclonable function (PUF) is a physical structure embedded in an IC that is very hard to clone due to its unique micro- or nano-scale properties that originate from inherent, deep-submicron manufacturing process variations. PUFs enable the new HIS approach, as PUFs are used as the hardware from which the key is extracted.

PUFs have been extensively investigated and recognized as a powerful, new security primitive. Originally, PUFs were added to a device to make it unclonable. The fact that the hardware’s intrinsic properties can be used as a PUF is an important and powerful insight that makes secure and low-cost HIS implementations possible.

Hardware “Biometrics”
There is a striking similarity between intrinsic PUFs and biometrics. An intrinsic PUF can be seen as the electronic fingerprint of an IC. The ways of working with PUFs and biometrics are also very similar. Both require a registration phase, during which attributes are measured, processed and stored so that either the biometric or electronic fingerprint can then be used for authentication and/or key storage purposes.

Using PUFs in an HIS System
To use a PUF in an HIS system, three functional modules are needed: a PUF measurement circuit, an activation code constructor and a key extractor.

PUF Measurement Circuit
A PUF measurement circuit is able to read out the device-unique characteristics of the PUF. This measured value is also known as the PUF response.

To be used in an HIS system, a PUF measurement circuit must meet the following requirements:

Low Cost
The measurement circuit should be low cost and easy to implement (i.e., with standard components).

Resistant to Physical Attack
During a physical attack meant to find the behavior of the structure, the functional behavior of the PUF should change such that tampering is detectable.

Not Based on a Secret
The PUF measurement circuit should not be based on a closely guarded secret. If there is no secret, even the manufacturer does not have an advantage in making a clone of the PUF.

Reliable
The PUF responses created by the measurement circuit should exhibit a low amount of noise in a wide range of temperature environments, in environments with electromagnetic radiation, or in environments that cause the device’s operating voltage to change. The noise level must be sufficiently low even after years in service.

Example: SRAM PUF
The static random access memory (SRAM) PUF is the best-known PUF based on standard components.

When a voltage is applied to a memory cell, it chooses its logical preference state—1 or 0—based on a complex interaction between several physical variables. The string determined by all the preference start-up values of the memory cells of an SRAM array forms a random identifier that uniquely identifies the SRAM. This identifier is the PUF response.

In the case of an SRAM PUF, the PUF measurement circuit is simply a circuit that reads out the start-up values of a specific range of SRAM that is exclusively reserved for this purpose.

Activation Code Constructor
The activation code constructor module computes the activation code that is needed by the key extractor module. The activation code contains error correction data needed to remove the noise from the PUF data and information about the compression function needed to extract randomness. This module can be implemented on the same IC where the key extractor is located, or as part of an external device or service.

Key Extractor
The key extractor module converts noisy PUF responses into a robust secret key by implementing noise cancellation and randomness extraction algorithms using the error correction data provided by the activation code constructor module.

Noise Cancellation
Secret keys must always be the same. Physical measurements are typically noisy, which introduces variation that must be removed before the measurements can be used to create secret keys.

Randomness Extraction
Secret keys offer security, based on the fact that they are completely random. Physical measurements have a high degree of randomness, but are usually not uniformly random. The key extractor processes the physical data and extracts the randomness with some compression functions, generating a uniformly random key.

The key extractor module can be implemented on an IC, or as a software module that runs on an embedded processor.
nanometer system-on-chip (SOC) designs are like an “extreme sport.” With each move to the next process node, designers try to incorporate more functionality and performance than ever before. However, as feature sizes shrink, interactions among transistors, cells and interconnects result in greater sensitivity to normal process variations (referred to as “manufacturing variability”), which can cause low yield for a specific design, as well as large variations in performance and yield from one design to the next at a given node.

Despite the increasing challenge of variability, no one can afford to compensate by budgeting more time in the design or verification schedules. Even as manufacturing variability becomes a critical issue for design teams, time-to-market continues to shrink as consumer devices drive an ever-larger share of the IC industry. To keep the wheels from coming off, companies need a design-for-manufacturing (DFM) discipline to help designers pick the right path through all these hazards.

Slow out of the Gate, but Moving into the Lead
Like most new technologies, DFM has had its ups and downs on the path to widespread adoption. Early DFM tools could identify potential problems, but couldn’t provide much useful information about how to fix them. At the same time, the transition to a foundry model meant that fabless companies no longer had detailed knowledge of manufacturing processes. All designers could do was implement wider design margins to ensure required yield—in the same way that 20th century engineers over-designed bridges for safety before finite element analysis allowed them to calculate the forces involved.

The 45/40-nanometer node appears to be the threshold of necessity for DFM, and early indications are that consistent success at 32-nanometer and beyond will be difficult or impossible without model-based DFM. That view is supported by recent foundry announcements that DFM techniques, such as lithographic and planarity checking and compensation, will be required for 45/40-nanometer designs and beyond.

Figure 1. Change in Yield Loss Factors

Today, designers and foundries finally have a way to address manufacturing issues at the earliest stages of implementation, before they become costly re-spins or manufacturing failures. DFM tools are providing foundries with the means to deliver detailed process data to designers without compromising their competitive process intellectual property (IP), while giving fabless designers the ability to identify and prioritize problematic areas and constructs, and to make automated corrections during the design and verification process.

Going forward, DFM will continue to be more tightly integrated into the design flow (e.g., as a key element of place-and-route (P&R) and custom design environments), so designers will see DFM less as a separate practice than as a standard part of doing business. DFM tools for each stage of the development process will become more complementary, giving designers a coherent and consistent view of the tradeoffs between performance and manufacturability. This will help designers reduce guardbands to get the most out of advanced manufacturing processes. In this way, the perception of DFM will evolve from an optional remedial exercise into a true source of competitive advantage.

Let's take a closer look at today’s state-of-the-art processes and where DFM may be heading.
Avoiding Crashes in the First Lap

The best place to eliminate variability issues from a design is at the beginning. IP used in a design must be created with manufacturing variability in mind. In the case of several major foundries, this means that all IP must be certified to meet DFM criteria. Fabless companies using externally purchased IP must apply similar DFM criteria to their own IP to ensure a common level of quality is delivered to the SOC design team for P&R.

There are two ways to consider the manufacturing variability problem during P&R. In one sense, DFM introduces a new set of design rules that various P&R engines must observe while placing cells and connecting the logic. In this “DFM-aware” P&R, every time a placement or routing decision is made, the P&R engine must consider not only timing, signal integrity, power and die size, but also whether there are random, lithographic, planarity and other variability and reliability issues that must be considered. In addition, to ensure that an optimal decision is made, these variability rules must be evaluated for all the different operational and process corners over which the IC must operate to meet its performance specifications.

The complexity of applying DFM rules over many corners points to the other more fundamental issue involved in addressing variability during implementation. To be effective at optimizing performance and variability, the P&R system must be capable of native multi-corner, multi-mode (MCMM) analysis and optimization. Otherwise, designers will be forced to engage in many iterations in an attempt to converge on a solution. With designs that are already complex due to multiple operating modes (sleep, standby, normal, etc.), and complicated signal integrity (SI) issues due to smaller dimensions, this repetition rapidly becomes an untenable flow, resulting in a frustrating and lengthy design closure phase. With MCMM, the P&R engine can use all the design drivers—timing, power, SI, die size and DFM models—to concurrently converge on an optimal solution.

Enhance While You Verify

Once the design is completed and moved to the verification process, a number of DFM techniques can assist engineers in optimizing the design for both performance and area. Three key areas that should be evaluated include critical area analysis (CAA), litho process checking (LPC) and three-dimensional (3D) variability (or planarity) analysis.

CAA reduces the probability of random defects due to particulates in the manufacturing process by maximizing space between interconnects without increasing overall die size. This is achieved by small adjustments to wire locations to optimize the use of “white space” in the layout.

LPC uses models of the foundry’s lithography process, including optical proximity corrections (OPCs) to the mask, the imaging capability of the stepper, etch characteristics and other factors, to predict how the specified layout will actually print onto the silicon wafer. It then identifies specific locations where distortions will likely cause a defect, such as a short or open, or a potential timing issue due to altered device or interconnect shapes. A “litho-friendly” tool employs LPC and interacts with the P&R or physical verification system by altering layout locations and shapes slightly to counteract the lithographic effects. Obviously, the value of a litho-friendly tool depends on the accuracy of its manufacturing models, so alignment with and validation by the foundry is critical.

Get Your Fill without the Boat

The third major area of DFM is compensation for 3D variability, which is the variation in planarity (flatness) of an IC resulting from the chemical mechanical planarization (CMP) process. Although metal fill has been used to minimize 3D variability for many nodes by making interconnect density more uniform, the solution becomes more challenging at each smaller node because ICs become more sensitive to layout variability, both manufacturing and electrical, caused by the fill. For example, fill itself alters parasitics, which changes critical signal propagation delays.

At nodes above 65-nanometer, traditional “dummy fill” was used to simply add metal to any unused space in the layout. But ICs manufactured at 45-nanometer and below require sophisticated algorithms to accurately answer the three fundamental fill questions: What shapes do I use, how many do I need and where do I put them?

Two methods are available to give designers some choice in how to achieve more effective planarity control. The first improvement for many will be equation-based fill, or “smart fill.” In this approach, the amount and location of fill are determined by user-defined constraints driven by measurements of layout geometry and metal density. The equations are essentially heuristics that predict how the CMP process will respond to a given set of shapes.

Achieving the highest level of fill accuracy and precision requires model-based fill. Model-based fill simulates the actual CMP process for a specific foundry and a specific design, resulting in an expected thickness at each point of the layout. The smart filling facility uses the predicted thickness data to not only determine how many fill shapes to use and where to place them, but also to determine the optimum shape of the fill metal and how much the fill will impact parasitics and timing. CMP models are supplied by most foundries, and there are tools and services available for companies that want to modify the foundry models, or build their own custom models.

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Ask set cost at 65-nanometer and below is limiting design starts. E-beam direct write (EbDW) technology has the potential to jump start design starts by virtually eliminating the need of photomasks for designs such as prototypes, derivatives and low-volume/high-value designs. However, throughput concerns have curtailed the use of EbDW for critical—and expensive—design data mask layers. Design for e-beam (DFEB) is a new design-for-manufacturing (DFM) approach that uses character or cell projection (CP) technology, combined with design and software techniques, to enhance the throughput of EbDW lithographic exposure. When applied to a 65-nanometer test chip design, DFEB can produce a design with an improved EbDW shot count, and thus improved throughput, without sacrificing the quality of design results.

E-beam: The Opportunity for a New Bridge

Traditionally, the mask has served as the bridge between design and manufacturing. However, if the goal is to reduce mask costs, another bridge is needed. EbDW machines, which can now project characters directly onto wafers, represent an opportunity to create a new, less costly bridge between design and manufacturing.

E-beam’s strength is accuracy. Even at 65-nanometer and 45-nanometer, no optical proximity correction (OPC) or reticle enhancement technology (RET) is required.1 However, e-beam’s historic challenge has been its throughput time; it is orders-of-magnitude slower than standard optical lithography.

Variable-shaped beam (VSB) and CP capabilities help to address this limitation. VSB fractures the complex shapes of design features into multiple rectangles, each of which requires a separate exposure or shot from the e-beam. CP uses stencils to project a larger character in one shot rather than in many shots, as would be the case in conventional VSB writing. Dozens to hundreds of characters can fit on each stencil. A CP machine may also have multiple character groups on a stencil mask; each character group can be exposed on the wafer by moving the e-beam without a time-consuming physical move of the stencil mask.

To achieve a 10–25X shot count reduction, DFEB changes the process of converting design features to characters from an inefficient “search and find” process for each design to a streamlined “take and optimize” operation with a stencil mask pre-manufactured per standard cell library instead of per design.

Advanced, CP-capable EbDW machines write directly on wafers without the need of a mask. At 65- and 45-nanometer, entire standard cells can fit within the projection area of these EbDW machines. Standard cells and random access memory (RAM), which can be converted to characters easily, now dominate system-on-chip (SOC) designs. These advances have resulted in a 2–5X improvement in throughput—a major step forward, but not enough to enable EbDW to be used for all critical design layers.

Recently, DFEB technologies and design techniques have been developed that speed up e-beam production a total of 10–25X over the traditional VSB method, depending on layer and design, making it practical for use on all critical layers of a SOC.

Design for E-beam

DFEB is a combination of software and design technologies that optimizes the design process to take maximum advantage of today’s most advanced CP EbDW equipment to reduce shot count and, in turn, make virtually maskless EbDW production feasible.

Because they represent over 80 percent of the cost of a typical SOC mask set, DFEB is aimed at eliminating the complex computer-aided design (CAD) layers of the mask set. These layers contain design data that defines the function and performance of the SOC.

Using CP EbDW, characters are laid out in a stencil mask design that acts as a “mini reticle.” Each cell’s orientation that has a corresponding character on the stencil mask can be projected in one shot rather than in many shots, as would be the case in conventional VSB writing. Dozens to hundreds of characters can fit on each stencil. A CP machine may also have multiple character groups on a stencil mask; each character group can be exposed on the wafer by moving the e-beam without a time-consuming physical move of the stencil mask.

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The EbDW process for any design can start only when the stencil mask is available. Currently, a taped-out design’s features are converted to characters. The design is searched to look for the most commonly occurring patterns per layer. A stencil mask is then produced with those patterns.
Using DFEB, the standard cell design library is co-optimized with the stencil mask design. This DFEB overlay library contains shot count information and DFEB-optimized cell layouts. Co-design minimizes the shot count of designs using the library while maximizing use of the limited space that is available on the stencil mask. The stencil mask thus produced can be used for any design using that cell library, and therefore is ready before tape-out and even before logic synthesis.

Designers use the DFEB overlay library with the original design library. The DFEB design methodology uses shot count as an optimization criterion along with area, timing, power and yield during the synthesis process, employing currently available commercial synthesis products without modification.

DFEB impacts only the implementation phase of the design process. A systems designer operating above the unchanged register-transfer level (RTL) is unaware of any differences in designing for EbDW.

The DFEB methodology retains a design’s “downward compatibility” for later processing with masks and standard optical lithography for large-volume production, if desired. Only the DFM/RET/OPC steps must be performed on the DFEB design to complete the design for mask production.

What Designs Benefit Most?
The designs that benefit most from DFEB are those that are most sensitive to reticle cost and manufacturing turnaround time: derivatives, prototypes and low-volume/high-value designs.

Derivative designs, which leverage existing design intellectual property (IP) to create multiple, differentiated versions of a single design platform, represent one of the most promising areas for the SOC market. With minimal additional design investment required, derivative designs can create a “long tail” of low-volume products that greatly increase the overall market for a given SOC platform. However, derivative designs can only provide this long tail if production costs are reduced.

The accelerated manufacturing cycle offered by EbDW and DFEB—without OPC, mask making, mask inspection and mask repair in the critical path—is especially attractive for prototypes. The faster a prototype can be plugged into the system, the sooner the debug process can start and the faster the product can get to market. DFEB also provides an ability to demonstrate (e.g., at a trade show) a working, battery-operated prototype system without the ribbon cables that attach to a field-programmable gate array (FPGA) prototype board.

Prototypes also often change to correct mistakes, reflect changes in the netlist, or respond to changes in the specifications or market requirements. Usually, the second mask set is limited to less-expensive, metal-only changes; but an EbDW-based, maskless prototype need not be limited to metal-only fixes. Because of cost, in a typical mask-based cycle, necessary changes and potential improvements to a design tend to “accumulate” waiting for the next mask set. This tendency significantly delays revisions. In contrast, an EbDW-based prototype can be turned immediately because there is no fixed non-recurring engineering (NRE) cost for the mask.

Finally, low-volume/high-value designs, such as those for supercomputing applications or very specialized equipment, benefit from the drastically lower DFEB manufacturing costs. By eliminating the majority of mask layers required to produce these designs, the total cost of these traditionally very expensive chips can be cut significantly.

Ecosystem Collaboration to Validate DFEB Design Flow
A group of industry leaders collaborated to create a DFEB design methodology and prove that it could reduce EbDW shot count and thus improve throughput.

The subject design was a three-million-plus-gate 65-nanometer test chip containing 188 memory macros and one phase-locked loop (PLL) macro. The area spec for the design was a fixed floorplan footprint of 4.2 x 8.4mm². The design used a 65-nanometer low-power seven-metal layer process. The core had a frequency of 166MHz, and the external interface used for testing with an FPGA had a frequency of 162MHz.

The DFEB methodology (Figure 2) employed an industry-standard synthesis tool to re-target and optimize the test chip to the DFEB 65-nanometer overlay library. Other commercially available electronic design automation (EDA) tools were used for physical implementation, timing closure, final verification and tape-out.

DFEB Design Flow
The DFEB design flow is very similar to established flows for advanced process nodes. The collaboration identified three areas where DFEB and standard design flows vary: DFEB overlay library preparation, floorplanning and synthesis/post-synthesis timing optimization.
The semiconductor industry—like virtually every other—is not immune to the challenges of the current economic climate. In April 2009, All American Semiconductor Inc., a leading distributor of semiconductors, obtained court approval of a chapter 11 plan of liquidation. More recent months have seen the bankruptcy filings of Aviza Technology Inc., a supplier of advanced semiconductor capital equipment and process technologies, and Magnachip Semiconductor Ltd, which sells and manufactures wafers designed and used by other semiconductor companies.

Even healthy companies, however, can be affected by a bankruptcy filing. The bankruptcy of a key customer or vendor can disrupt a company’s supply chain and, in the case of a bankrupt customer, create the potential for significant receivables to go uncollected. Perhaps more critically, licensing rights in intellectual property can be affected by a bankruptcy filing where the bankrupt entity seeks to terminate its rights and obligations under license agreements.

While the current outlook may be grim for the economy at large, the prospects of individual companies vary significantly, and some companies will continue to perform well despite the larger trends. For example, the designer retailer’s loss may become Walmart’s gain as consumers shop more closely for bargains. As car manufacturers frequently say, “your mileage may vary.” For some companies, this means finding new strategies to survive in a world of tightening credit markets and shrinking revenue. For others, the global crisis presents the chance to capitalize on opportunities that the current economy provides.

Asset Sales in Bankruptcy

One such area where one company’s crisis may be another’s opportunity is in the asset sales that frequently accompany chapter 11 cases.

Traditionally, chapter 11 of the Bankruptcy Code was designed to facilitate management’s rehabilitation of a troubled company, while chapter 7 offered a streamlined process for the liquidation of a business under the supervision of an appointed trustee. In the modern day, however, companies with every intention of selling all or substantially all of their assets are filing for bankruptcy protection in chapter 11 too. The advantage to a company of liquidating in chapter 11 is that it offers management the ability to continue operating the business in bankruptcy. This, in turn, frequently translates to a more orderly liquidation process in which the troubled company can be marketed and sold as an ongoing (and presumably more valuable) enterprise, rather than as a lifeless assortment of inventory, equipment and receivables.

Asset sales in chapter 11 have become more commonplace as companies have resorted to bankruptcy as a means to liquidate, rather than reorganize, the corporate entity. Commonly referred to eponymously as “Section 363 sales” (named for the Bankruptcy Code section from which they arise), they enable the trustee in a bankruptcy case to sell anything, ranging from a single piece of equipment to the entire ongoing business enterprise. Under the terms of the Bankruptcy Code, proposed sales are subject to approval by the bankruptcy court and generally (though not always) conducted through an auction process in which entities may bid for the assets offered for sale by a bankrupt debtor.

Most potential buyers fall into two categories: strategic buyers and financial buyers. A strategic buyer, most typically, is a company engaged in the same or similar business as the target company. The strategic buyer will view the acquisition as an opportunity to add to an existing industry presence or vertically integrate the target company into its supply chain. A financial buyer, on the other hand, views the acquisition as an investment. The acquisition may be a one-off transaction, or the buyer may add it to a portfolio of companies in a particular industry. Of course, the difference between the two types of buyers is not always well-defined; for example, a private equity fund seeking to add a target company to a portfolio of companies in a similar industry may exhibit attributes of both strategic and financial buyers.

In the recent semiconductor cases, both Aviza and Magnachip...
filed their chapter 11 cases with proposed buyers already lined up. The proposed acquirer of Aviza, Sumitomo Precision Products Co. Ltd., is a diversified equipment manufacturer that makes a semiconductor manufacturing system that competes with an Aviza system—in other words, a strategic buyer. In this situation, therefore, the acquisition will add to Sumitomo’s semiconductor business unit and consolidate competing systems under a single banner.

The proposed buyer of Magnachip’s assets, on the other hand, is a financial buyer. KTB 2007 Private Equity Fund, a Korean venture capital firm, will add Magnachip’s operation to its portfolio of technology companies, which includes Siltron, a manufacturer of silicon wafers. As other companies in the semiconductor and related industries contemplate their options, more opportunities like these are bound to emerge.

For those companies with available liquidity, Section 363 sales provide an excellent opportunity to strengthen existing operations through the strategic acquisition of individual assets or entire business units. These sales provide the added benefit of having received the “blessing” of the bankruptcy court, without which a Section 363 sale cannot be concluded. Bankruptcy court approval, which typically carries with it findings that the sale was for reasonable value, frequently also heads off the later possibility that the sale might be challenged as having been for less than fair value. Such approval also affords the purchaser the benefit of the safe harbor provisions of Section 363, which protects the integrity of the sale to a good faith purchaser in the event the order approving the sale is subsequently appealed. Of particular value to buyers seeking to acquire entire business units, such sale orders may also contain provisions limiting or extinguishing any potential successor liability associated with the acquisition.

Intellectual Property Rights in Bankruptcy

Another key area of concern (and opportunity) arises in connection with the license of intellectual property rights by or to a bankrupt entity. Among other powers granted to a debtor in bankruptcy is the ability to elect whether to “assume” (i.e., retain) or “reject” (i.e., terminate) contracts (including licenses) under which substantial performance remains due by both parties such that termination of the contract would constitute a material breach excusing performance by the other party. Such contracts are referred to in Section 365 of the Bankruptcy Code as “executory contracts,” and the Bankruptcy Code sets forth at length the respective rights of both the debtor and the nondebtor counterparty based upon whether the debtor elects to assume or reject the contract.

Brieﬂy stated, when a debtor elects to assume an executory contract, it cures all outstanding defaults (including payment defaults, but excluding nonmonetary defaults) and agrees to be bound by the contract going forward as though the bankruptcy had never occurred. When a debtor rejects an executory contract, the rejection is treated as a breach of the contract as of the commencement of the bankruptcy case, following which the contract may be terminated and the nondebtor counterparty may assert a claim against the bankruptcy estate for damages arising from the rejection and resulting breach. The decision to assume or reject an executory contract is one that lies within the exercise of a debtor’s reasonable business judgment, and provides a debtor with the ability to divest itself of unproﬁtable contracts while preserving proﬁtable relationships and those essential to the continued operation of the debtor’s business. Notably, the debtor may elect whether to assume or reject the contract even over objection of the nondebtor counterparty except in limited circumstances where, for example, either applicable law excuses the nondebtor party from accepting performance from a third party (e.g., franchise agreements) or the contract is a financial accommodation (e.g., loan, promissory note).

Licenses, including licenses of intellectual property, are generally considered to be executory contracts and therefore subject to a debtor’s right to assume or reject them subject to the requirements of the Bankruptcy Code. When a licensee ﬁles bankruptcy, therefore, the licensor (i.e., the nondebtor counterparty) can anticipate that the debtor licensee will seek either to retain or divest its rights under the license agreement. Upon the former, assumption of the license will return the parties essentially to the status quo ante; and upon the latter, rejection will entitle the licensor to file a claim for damages, if any, arising from the termination. In many instances, it may reﬂect the loss of a royalty stream, but is unlikely to represent a catastrophic event for the licensor.

More complicated, however, is what happens when the licensor ﬁles bankruptcy and seeks to reject license agreements between itself and its licensees. From the licensee’s perspective, termination of a license has the potential to be catastrophic, as a licensee’s entire business model may be built around access to the intellectual property obtained through the license agreement. To protect the licensee in these situations, the Bankruptcy Code grants the licensee the power to partially override the debtor licensor’s decision to reject the license and preserve its rights in the underlying intellectual property.

Section 365(n) of the Bankruptcy Code sets forth the rights of a licensee of intellectual property when the debtor elects to reject an executory contract under which the debtor is a licensor of intellectual property. The Bankruptcy Code deﬁnes “intellectual property” to mean—

(A) trade secret,
(B) invention, process, design or plan protected under title 35,
(C) patent invention,
(D) plant variety,
(E) work of authorship protected under title 17,
(F) mask work protected under chapter 9 of title 17.

The term “mask work” in this context is given the same deﬁnition as provided in chapter 9 of title 17 of the United States Code, which deﬁnes mask work as “a series of related images, however ﬁxed or encoded— ”

(A) having or representing the predetermined, three-dimensional pattern of metallic, insulating or semiconductor material present or removed from the layers of a semiconductor chip product; and
(B) in which series the relation of the images to one another is that each image has the pattern of the surface of one form of the semiconductor chip product.

Reading these provisions together, the protections of Section 365(n) will typically extend to the nondebtor licensee under a mask work license as well as other licenses of intellectual property.

If the debtor licensor elects to reject a license of intellectual property (say, mask work), the licensee may elect to treat the license as terminated by such rejection and file a claim in the bankruptcy case for damages arising from such rejection and termination—in other words, to effectively acquiesce in the rejection and allow the license...
ChipX, a fabless semiconductor company founded in 1989, offers the broadest range of mixed-signal application-specific IC (ASIC) solutions targeting system and semiconductor companies. The company’s offering includes standard cell ASICs, the industry’s highest performance structured ASICs, unique hybrid ASICs (a blend of standard cell and structured elements) as well as full-custom analog design. This offers a true one-stop shop for all ASIC needs.

With limited cash, semiconductor companies can enter the market with ChipX’s low-cost ASICs, saving significant cash otherwise required to hire back-end engineers and license electronic design automation (EDA) tools and intellectual property (IP). ChipX’s expertise in analog design, high-speed interfaces and data converters will reduce the development risk associated with complex systems-on-chip (SOCs), further reducing customers’ project costs and speeding time-to-market.

While customers can validate their product and market with a field-programmable gate array (FPGA), ChipX can migrate them to a low-cost, low-power production ASIC solution with confidence. Applications can range from high-voltage 0.60-micron to low-power 65-nanometer for consumer devices.

In addition to servicing the commercial market, ChipX is International Trade in Arms Regulations (ITAR)-compliant, a requirement for military designs. The company’s process has also been audited for Design Assurance Guidance for Airborne Electronic Hardware (DO-254) compliance mandated by the Federal Aviation Administration (FAA), and is capable of undertaking aerospace designs that require adherence to DO-254. Finally, for legacy applications in telecom, industrial and military/aerospace, ChipX will replace end-of-life (EOL) FPGA and ASIC components with equivalent ASICs—risk free—and extend the life cycle of the customer’s system.

“ChipX’s partnership with GSA has been a great cross-functional resource to our team throughout the years. We use the market data to keep our pricing competitive, and the GSA conferences we attend allow us to remain up-to-date on technology trends and maintain a presence in the industry. The events that GSA hosts are the best opportunity for professional networking that we have.”

—Phil McCarthy, Director of Operations, ChipX

Amnon Fisher, President & CEO
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GEO Semiconductor develops and manufactures semiconductors that provide highly differentiated solutions for advanced geometry, graphics and video processing. Through its acquisition of key IC lines and associated intellectual property (IP), patents, software, brands, inventory and customers from Silicon Optix, GEO Semiconductor is able to offer its customers two highly capable platforms—Digital Video 2.0™ and Projection 2.0™. Through the GEO IC platform, Projection 2.0™ moves geometry processing into the software domain and allows customers to mix and match GEO Semiconductor’s IP and algorithms (offered via application programming interfaces (APIs)) with their own IP. Similarly, Digital Video 2.0™, through the Realta IC, enables customers to mix and match IP for video and graphics processing applications.

Both the Realta and GEO IC families, which are capable of real-time processing of full high-definition (HD) signals (1080p) and beyond, embody product concepts and algorithms resulting from two decades of breakthrough research valued in excess of $200 million. Realta’s key markets include high-end consumer video, broadcast, professional displays, 3D and education systems. The GEO IC serves the projection, telepresence and security markets by providing digital correction of optical systems, and the flat panel display market by providing brightness and color uniformity. This business is expected to ramp rapidly.

“Being a part of GSA provides opportunities to access information, network with industry leaders and get ongoing updates to the global evolution of the semiconductor industry. Presentations by Andy Rappaport, Alex Baklanski, Atiq Raza and Dan Niles were invaluable as their insights played a role in defining GEO Semiconductor’s strategy. And GSA makes it possible for young shoots to join at fire-sale prices!”

—Paul Russo, Chairman & CEO, GEO Semiconductor

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The dearth of capital during the past two quarters is clearly noticeable, with few new semiconductor companies forming, venture capitalists protecting their strongest investments and weak companies dropping like flies. In this helter-skelter environment, it’s hard to spot the obvious home runs. Yet, some trends are still evident.

For some time, there has been little room for traditional fabless start-ups in the 40-nanometer digital domain. Design costs are simply too high to make a reasonable return on investment. These days, most action appears at the fringe of the industry rather than in the mainstream.

After eliminating the $5 billion sub 65-nanometer foundries and their major league customers, what is left? Actually, quite a lot. There are still many emerging innovations in the compound semiconductor and microelectromechanical systems (MEMS) arenas. Materials such as Indium Phosphide and Gallium Nitride still have lots of runway, and there are many companies pursing optical, power, lighting and radio frequency (RF) products based on these materials.

From personnel area network (PAN) to local area network (LAN) and wide area network (WAN), there is always innovation in the RF arena (both baseband and mixed-signal); however, most recent efforts are focused on the front end as the cost of baseband development has become prohibitive.

There have always been companies pursuing alternative memory technologies to replace both dynamic random access memory (DRAM) and Flash. Today, more than a handful of companies are making advances and one was recently unveiled.

**Unity Semiconductor** was formed in 2002 to develop storage-class non-volatile memory (NVM) products utilizing multi-layer memory array architectures and a new memory cell technology called CMOx. The company has raised more than $70 million to date and anticipates seeking another $25 million in 2010.

Why do so many companies chase the memory market? Because it’s huge! Based on market research forecasts, Unity believes the total available market (TAM) for its storage-class NVM products will be approximately $15 billion in 2010 and grow to more than $25 billion in 2013.

Furthermore, Unity argues that the ability of NAND Flash technology to scale is reaching its limits, creating an opening for new technologies such as resistive random access memory (RRAM), ferroelectric RAM (FeRAM), phase-change memory (PCM) and magnetoresistive random access memory (MRAM).

In contrast to other emerging memory technologies, Unity argues that only its CMOx technology has the small cell size to beat NAND Flash in cost and density. Unity’s objective is to have the smallest die size and the lowest manufacturing cost-per-bit storage-class NVM products. The company has filed an intellectual property (IP) portfolio that presently includes 60 granted patents, with another 90 patent applications in various stages of being granted.

Unity’s technology is based on a passive cross-point, multi-layer memory array and its CMOx memory cell, a technology that is based on conductive metal oxide materials and the motion of ions. Unity’s CMOx-based design uses four physical layers of multi-level cell (MLC) memory and is the key to increasing the density of its storage-class memory products. CMOx will yield products with 4x the density and 5–10x the write speed of today’s NAND Flash.

Beyond technology innovation, Unity has also developed several groundbreaking business concepts. Key among these is the separation of front-end-of-line (FEOL) CMOS base wafer processing from back-end-of-line (BEOL) memory layer processing.

No new process technology is used in the CMOS base wafer, which can be fabricated on a trailing-edge 90-nanometer CMOS process. The CMOS FEOL strategy allows Unity to be a moderate follower in CMOS transistor technology. Its shrink path is unconventional in that a higher density memory core doesn’t require base CMOS technology migration. Instead, Unity can use the same 90-nanometer base CMOS process for multiple generations, as well as use proven design IP to reduce risk and time-to-market.

The finer pitch BEOL memory strategy calls for Unity to form a joint venture partnership for volume manufacturing with a top-tier integrated device manufacturer (IDM) already in the memory business.

Unity has been processing 64-kilobit devices for two years, a 64-megabit device for one year, and is in design of a 64-gigabit device that is now close to tape-out and slated for pilot production in 2H 2010, with volume production in 2Q 2011.

Unity’s planned second-generation products are high-capacity, high-performance 128-gigabit and 256-gigabit storage-class memories with an interface, command set and features tuned for state-of-the-art solid state devices (SSDs). The third generation will achieve the historic milestone of single-chip 1-terabit storage-class memory. Unity expects to build a 1-terabit storage-class memory product within five years using a 20-nanometer CMOx process technology.

Many alternative memory technologies have come and gone over the years. Why has it been so hard for any to achieve success? Certainly, the incumbent technologies are like steam rollers, flattening anything in their path. The inability of today’s memory technologies to scale into the future, if this is truly insurmountable, may create an opening for new emerging technologies, and Unity is well poised.

The other issue is that few emerging technologies ultimately deliver. At the end of the day, they all have problems, whether it’s cost, reliability, performance or manufacturability. Whereas many companies appear to have a singular focus on one technology, regardless of whether it’s flawed or not, Unity appears to have taken a pragmatic view of the market, focusing on business and market issues as strongly as technology issues as demonstrated by its separation of front-end and back-end wafer processing. Based on this, I believe Unity’s approach has much higher odds of success than many other competing alternatives.

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Robin Cheung, VP, Process Engineering
Christophe Chevallier, VP, Design Engineering
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a 3-to-1 selectivity make a successful polish even more difficult. If small, isolated features and large or dense structures exist in the same die, pattern density variation requires a different approach. To compensate, slurries specifically formulated with an extremely high selectivity to nitride offer the preferred approach.1

Further complicating an already complex scenario is the fact that each device—to a large degree—has its own integration scheme depending on the end product and inherent performance requirements. This means that copper CMP, for example, won’t always be run the same way—far from it in fact. It must be tailored for each implementation. In addition, these examples only address the truly “mainstream” CMP processes. The ongoing push to shrink geometries and to find and integrate new materials are two further areas that expand the complexity of the CMP process, and highlight some of the major considerations when deciding whether to develop and implement CMP in-house, or turn to partners with focused expertise.

**Applying Process Expertise to Emerging Technologies**

CMP has long been established in advanced CMOS manufacturing, and emerging technologies are now attempting to implement CMP to achieve the performance they need. These applications have their own challenges when looking to perform CMP, and in many cases, are being manufactured in facilities that have not previously implemented CMP.

MEMS is a rapidly growing market and the largest emerging market working to leverage CMP. Such devices are frequently constructed with alternating polysilicon and oxide layers and with much larger topographies than typically encountered in CMOS, with step heights up to tens of microns and feature sizes of several hundred microns. Long polish times are often required, increasing pattern density and process instability issues. New slurries created specifically for MEMS are being developed to address some of the unique CMP requirements of these devices.

Other areas in which CMP may have a role include: the development of engineered substrates and custom epitaxial layers such as SOI, SiGe strained layer structures and various III-V and II-VI compound semiconductors; analog, mixed-signal and power devices; advanced packaging and through-silicon vias (TSVs); and direct wafer bonding because CMP offers one of a very few means to get two surfaces smooth enough to achieve the necessary bond.

**Benefits of Outsourcing Specific Process Modules**

Underlying the technology discussion is one about costs. As if process complexity wasn’t enough, the costs to invest in and maintain a CMP line are substantial. Part of this is due to the process throughput, which often acts as a “roadblock” in the fab. To eliminate the roadblock internally, a manufacturer must order more tools (and find the fab floorspace for those tools), or look outside the facility (i.e., to an outsourced manufacturing partner) to enable the CMP module to keep pace with the other fab processes. Clearly, trying to perform advanced R&D on tools in a fab will further impact manufacturing capacity, which highlights another reason to outsource that work as well. As the number of integration schemes and new materials that require CMP (or other processes) climb, these factors will become even more pressing and push manufacturers to consider alternative strategies such as outsourcing.

Outsourcing allows manufacturers to reduce risks and accelerate time-to-market, largely due to shortened or reduced R&D cycles since a strong outsource partner will be able to provide a better “starting point” for a given process. Reducing R&D cycles directly impacts time-to-market since products are ready for manufacturing more quickly. Processes can be transferred back into the fab, or manufacturers can continue to outsource some or all manufacturing to the outsource partner to gain further time-to-market advantage.

Another benefit that comes from using an outsource partner is that in most cases they bring a broad exposure to all technologies, giving them a strong knowledge base to draw from as new materials, integration schemes and devices move into the manufacturing mainstream. Dedicated service foundries know what process(es) they run better than most process managers in the fab and across a much wider variety of process requirements. They fully understand and are able to characterize the risks posed by new requirements without having to engage in a trial-and-error approach, further accelerating R&D.

A strong outsource provider offers flexible production capacity and the ability to execute development projects on an as-needed basis. Such resources, external to manufacturing facilities, can provide the personnel, knowledge and tool time necessary to complete projects that would otherwise take up the available production resources in the fab.

**About the Author**

With over 20 years of semiconductor industry experience, Jim is responsible for revenue growth at Entrepix. In this role, Jim is focusing on globally expanding Entrepix offerings to all types of device manufacturers, materials and consumable providers, universities and laboratories. Jim joined the Entrepix team after holding various executive management positions for SEZ America—most recently as vice president of sales and marketing—where he was responsible for the growth of SEZ America and served on the strategic advisory board for the SEZ Group. Before serving SEZ, Jim was an engineering section manager for diffusion, implant, metals and back grind operations for a discrete components fab in Motorola’s semiconductor product sector. Jim received a Bachelor of Science degree in microelectronic engineering from Rochester Institute of Technology, Rochester, New York and a MBA from the University of Phoenix, Phoenix, Arizona. Jim Mello can be reached at jmello@entrepix.com.

**References**

Shrinking geometries and growing analog content exacerbate variations in parametric performance. Transistors become more sensitive to location context, wires become thinner and more resistive, and more routing layers introduce increased parasitic capacitance. Integrating the lithographic and CMP models described earlier with layout versus schematic (LVS) and extraction tools provides designers with detailed device and interconnect parameters based on accurate simulation of actual manufactured IC geometry and electrical interactions. Designers can plug the resulting device parameters, which reflect actual as-built device and interconnect shapes, into a fast SPICE simulator to get more accurate timing predictions.

Recommended rules are another part of the design process that have a direct impact on design optimization. Critical feature analysis (CFA) is a technique that can help designers achieve maximum benefit from recommended rules. Because CFA statistics are fab- and process-dependent, specific configuration data must be provided by the foundry. This information can then be used to evaluate and prioritize recommended rule violations, helping designers determine the most cost- and time-efficient optimizations. This information helps designers focus on maximizing manufacturing robustness while minimizing design area. To be effective, CFA usually requires evaluation of complex interdependencies, which is typically beyond the scope of traditional design rule checking (DRC) engines.

Addressing this challenge requires a new verification capability called equation-based DRC, which enables evaluation of continuous functions of 3D layout geometry. Equation-based DRC goes beyond simple pass/fail checking to solve for the relative contribution of each layout feature to a CFA score. Equation-based DRC is used to enable the definition of CFA evaluation criteria to provide the quantitative results needed to rank the violations by relative impact and to indicate how and how much a layout should be modified to accomplish the desired level of variability improvement.

Another area that is emerging at smaller process nodes is advanced electrical rules checking (ERC). With smaller geometries being more susceptible to electrostatic discharge and electromigration failures, new checks are needed to ensure both factory yield and in-system reliability. Often, these checks are complicated by the existence of multiple voltage domains that require additional interface circuits and connection constraints. These verification challenges cannot be addressed effectively by traditional checks based only on layout geometry. What is needed is an integrated platform that can apply user-programmed rules based on both netlist and geometric information in a cohesive and interrelated fashion. Such a programmable ERC engine opens up new areas of automation for design checks and improvements that can prevent factory failures, improve in-system reliability and ensure that designers are implementing circuits that are consistent with the company’s design style sheets.

**What about Process Feedback?**

If DFM due diligence is done at every stage, then most potential manufacturing variability problems will be controlled while achieving competitive performance. Of course, there will still be manufacturing defects, but if a process is under statistical process control, the defect rate should match the expected yield entitlement (random defect rate) based on the measured particle distribution for the process. But what if a yield excursion still takes place? It happens.

To address this eventuality, a new class of tools is emerging to help companies quickly recognize and diagnose remaining systematic yield limiters. Diagnosis-driven yield analysis tools use logical design and physical layout information, combined with statistical test failure data collected on all product test failures, to categorize the probable type and location of silicon defects. Essentially, these tools eliminate impossible or unlikely suspect failure causes based on all the available information about the chip, including its physical design details and actual test failure trends. This helps separate random from systematic yield issues and speeds up the failure analysis process tremendously. Once a systematic yield limiter is identified, it can be eliminated through process or design remediation. Over the life of a process node, diagnostic feedback from multiple designs can be used to close the DFM loop by indicating what DFM rules should be elevated in importance, or what new rules might be required for follow-on designs targeted for the same fab.

**Taking DFM to the Fab (and the Bank)**

DFM is both a discipline and a design automation environment. TSMC, the world’s largest independent IC foundry, describes DFM as the “cross-domain know-how” that addresses the gap between chip design and the wafer fab. Enhanced DFM technologies allowing design and optimization processes to be partially, if not completely, automated while providing knowledge of manufacturing variability sensitivities throughout the design flow are now available. But perhaps the biggest change has come in the interaction between the designers and the foundries. With specific process information from foundries, designers can accurately identify and predict impacts on design performance and robustness, and take steps to eliminate or reduce their effect long before the first wafer is produced. In turn, foundries can collect information from many designs to ensure that their processes are accurately reflected in the models and statistics they provide.

As design and manufacturing costs continue to rise at each node, electronic design automation (EDA) vendors and foundries are partnering to provide DFM solutions that enhance and optimize IC designs, making them more competitive, while reducing the unwanted effects of manufacturing variability.

**About the Author**

Michael Buehler-Garcia manages and directs the design-side marketing efforts for Mentor Graphics’ Calibre product offering. Prior to joining Mentor, Buehler-Garcia was vice president of marketing and business development at Ponte Solutions. Before joining Ponte, Buehler-Garcia held the title of vice president of worldwide marketing and business development for iBoC Technologies, a leader in soft error solutions, and held the same position at Chartered Semiconductor Manufacturing, one of the world’s top dedicated semiconductor foundries. He also served as vice president and general manager of PDF Solutions’ DFM business unit and was group director of strategic relationship marketing at Cadence Design Systems. Michael holds a bachelor’s in mechanical engineering and alternate energy systems from Arizona State University. Michael Buehler-Garcia can be reached at michael_buehler@mentor.com or 408-436-5804.
between customers and suppliers—especially in a downturn.

In a number of capital equipment industries, most notably aerospace and defense, there is a transition in the nature of service contracts. Traditional relationships between manufacturers and customers are being replaced by risk-sharing relationships commonly referred to as performance-based contracting (PBC). In PBC, the customer pays for the performance of the product—notthing more. This means that it is up to the OEM to manage the maintenance and repair of the product throughout its lifecycle and ensure that the equipment meets the agreed upon availability and performance targets.

Applied Materials pioneered the use of PBC in the semiconductor industry with the introduction of its Total Service Solutions program in the late 1990s, offering "price per wafer pass" contracts. Even still, this hasn't been a widely adopted practice, and there has been limited application across the industry over the past 10 years.

Table 1. Examples of Service Product Business Models

<table>
<thead>
<tr>
<th>Business Model</th>
<th>Product Ownership</th>
<th>Terms</th>
<th>Examples</th>
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</thead>
<tbody>
<tr>
<td>Disposal</td>
<td>Customer</td>
<td>Dispose upon failure or upgrade</td>
<td>Disposable cameras, cell phones</td>
</tr>
<tr>
<td>Ad Hoc Service</td>
<td>Customer</td>
<td>Pay as you go for service time and materials</td>
<td>Consumer electronics, traditional automobiles</td>
</tr>
<tr>
<td>Cost Plus</td>
<td>Customer</td>
<td>Payment for service based on actual support costs plus agreed upon margin</td>
<td>Construction, military weapon systems</td>
</tr>
<tr>
<td>Warranty/Contract</td>
<td>Customer</td>
<td>Fixed price, paid in advance, guaranteed service targets</td>
<td>Automobiles, computers, industrial capital equipment</td>
</tr>
<tr>
<td>Performance Based</td>
<td>OEM/Service Provider</td>
<td>Service payments based on actual uptime performance and unit of output</td>
<td>Aircraft, aircraft engines, avionics, tires, industrial chemicals, wafer fab equipment</td>
</tr>
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One of the most critical elements of PBC is the clear separation between the customer's expectation of service and how the supplier meets that expectation. Customer-driven efforts to prescribe how performance targets should be achieved often multiply overall supply chain costs without any tangible improvement in overall product performance. The OEM is always in the best position to determine how to achieve a performance improvement goal, but there aren't always sufficient incentives to drive a change in OEM behavior.

A case in point in the semiconductor industry is the traditional focus on spare parts "fill rate" as a surrogate for measuring the impact of parts availability on equipment uptime. One equipment manufacturer interviewed has successfully transitioned to "machine down awaiting parts" as a more appropriate measure. This has allowed them to increase performance while reducing overall inventory investment with lower fill rates.

Using PBC, OEMs and their customers can effectively align incentives by directly tying supplier compensation to product performance and customer value. The OEM has an incentive to achieve performance objectives at the lowest possible cost and to take actions that would cost effectively improve the performance of the system—which is also a significant benefit to the customer. This gives the OEM the incentive they need to meet contractual performance levels by separating the performance metric from the tactical methodology behind achieving it.

While the implications of PBC can be enormous for both OEMs and their customers, there are significant challenges to any organization trying to implement a PBC system. These challenges include:

- Pricing the contract correctly.
- Determining an accurate forecast of customer requirements.
- Analyzing the financial risk of a performance-based contract.
- Managing suppliers who are critical to achieving performance objectives.
- Tracking and managing performance against contractual metrics.
- Dealing with bad service data.

The common theme in all these issues is the need for advanced tools and technology to measure contract performance and model the infrastructure and costs associated with delivery target contract performance.

Furthermore, new markets such as solar will provide an excellent opportunity for equipment manufacturers to implement PBC. For semiconductor equipment manufacturers, the solar market is a unique but challenging opportunity as the market for solar fabs includes both new customers and new geographies. To be successful in this market, equipment manufacturers need to develop a new business model for fab support that is built on a performance-based relationship and addresses the changing needs of the customer over the product lifecycle.

Summary

While this downturn has been extremely painful for the semiconductor equipment industry, it’s time to start looking forward and planning for the future. The customer landscape and the equipment service supply chain have changed dramatically over the past 12 months and will continue to do so through 2010. Weaknesses in the supply chain will create challenges during the upturn, but this is an opportunity to re-think the service supply chain strategy and be better prepared for future business cycles.

About the Author

John Nunes is the vice president of strategic consulting for MCA Solutions Inc. He heads the company’s strategic consulting business to help clients develop and implement aftermarket and service supply chain strategies. John has senior management experience in service operations and marketing at KLA-Tencor and Applied Materials, and holds a bachelor’s in mechanical engineering and a master’s in operations research from Columbia University in New York, New York. John Nunes can be reached at john.nunes@mcasolutions.com.

References

GLOBALFOUNDRIES continued from page 24

of GLOBALFOUNDRIES provide the company and its customers? As a company that prides itself on being a “global” foundry, what long-term goals does the company hold in terms of expansion?

A: GLOBALFOUNDRIES’ manufacturing facilities in Germany and the U.S. present a number of strategic advantages for the company and its customers. First, our fab locations provide the optimal geographic footprint to attract the world’s top semiconductor technology talent. Second, with over 80 percent of our target customers in the U.S. and Europe, having fabs in these regions supports a higher level of engagement and intimacy with our customers.

While our current expansion plans are focused on the U.S. and Europe, we will look at developing long-term plans to further diversify our manufacturing footprint based on the needs of our customers.

Q: To maintain a competitive edge, many foundries are heavily investing in process technology development; however, this comes at a high price. With leading-edge technology being a cornerstone of the company’s value proposition, how does GLOBALFOUNDRIES plan to provide the latest process technology at a lower cost to customers, and yet continue to support the research and development (R&D) needed to develop new process technology?

A: GLOBALFOUNDRIES’ advanced process technology is possible because of the collaborative R&D model we have chosen to employ through our participation in the IBM Technology Alliance. As an early adopter of process technology, we’re in a privileged position to drive leading-edge technology within a collaborative environment that harnesses the shared talents of a number of the world’s largest semiconductor companies. We believe this is an incredibly scalable model and one that will provide significant competitive advantage, as it provided AMD when they competed against a much larger rival.

Q: GLOBALFOUNDRIES announced that it will bring 28-nanometer technology to the industry, displaying its advanced technology leadership. However, some foundries are already experiencing low yield levels at 40- and 65-nanometer. What measures are GLOBALFOUNDRIES taking to achieve high yield at these leading-edge nodes?

A: GLOBALFOUNDRIES possesses a number of unique capabilities that we’ve developed over the years to bring leading-edge technology into production at high volume and mature yield. One of the company’s most significant areas of differentiation is our Automated Precision Manufacturing (APM) technology. APM functions as a central nerve center for the fab and monitors wafer production at every step of the process to ensure optimal performance, yield and predictability of production. Today, there is great opportunity to apply these technologies and capabilities to set a new standard for foundries in time-to-mature yield for high-volume, leading-edge wafer manufacturing.

Q: There is much debate within the industry concerning the migration to 450mm fabs. Some companies are pushing for the shift in the coming years, while others argue that R&D costs will be too high. Do you believe 450mm fabs will be operating in the next three to four years, or will foundries pursue working on improving their current 300mm fabs?

A: We believe there is still tremendous efficiencies and scale to be had with 300mm manufacturing. So much so that our new state-of-the-art $4.2 billion manufacturing facility in upstate New York will be built on 300nm technology. At some point, the industry will likely migrate to a larger wafer size, but we perceive this as something that’s more likely to occur in the next decade or so when equipment manufacturers and the industry as a whole are ready.

Q: The microelectromechanical systems (MEMS) industry is undergoing a dramatic shift, as its market base expands into the consumer space. With an increasing number of consumer applications utilizing MEMS, more in-house production is being outsourced to independent foundries. With GLOBALFOUNDRIES’ services addressing the consumer segment, is it considering entering the MEMS market? What primary markets is the company currently focusing on?

A: While GLOBALFOUNDRIES does not currently plan to venture into the MEMS market, we will certainly explore other markets with our prospective customers in the future. Our initial focus will be in areas such as CPUs/graphics processing units (GPUs), consumer electronics and low-power technologies as they typically require leading-edge process technology and have the biggest market opportunity for GLOBALFOUNDRIES.
DFEB Overlay Library Preparation

To minimize shot count, the test chip was implemented with a DFEB-optimized cell library—the DFEB overlay library. A commercially available physical implementation system was used to create abstracts from the graphic design system II (GDSII) DFEB library. The conventional standard cells in the library were assigned a “hide” attribute so the place-and-route tool would not use them.

DFEB Floorplanning

EbDW stencil masks have limited capacity. But each cell’s orientation requires a different character except where symmetry can be exploited. To speed EbDW lithography throughput, the number of cells that can be shot using one character should be maximized. Therefore, the DFEB floorplanning methodology heavily favors standard cells of certain orientations and static random access memory (SRAM) macros of north-south orientations.

These preferences introduced additional criteria for floorplanning. Even so, the test chip’s 4.2 x 8.4mm² footprint was met while avoiding routing congestion. Routing over the 188 memory macros was allowed for five metal layers and above.

Another difference in DFEB floorplanning is power planning. The DFEB methodology recommends the metal width be an integer multiple of 1.0-micron because the widest power wire that can be written accurately on the EbDW machine in use for this process is 1.0-micron wide. So a 1.1-micron wire would have the same shot count as a 2.0-micron wire. The estimated power and ground width requirement for four to seven metal layers was calculated accordingly. The power ring design also followed the DFEB metal width guideline and met the design rule check (DRC) and metal density rules.

Synthesis/Post-Synthesis Timing Optimization

The use of clock tree synthesis (CTS) was restricted to only the DFEB buffer and inverter cells. The CTS results for clock skew and insertion delay met specifications, with the skew less than 300ps and the insertion delay less than 3000ps (less than half the clock cycle).

DFEB Test Chip Project Results

The goals of the test chip project were to establish a DFEB design methodology and to confirm the reduction in EbDW shot count using this methodology while maintaining quality of results, in terms of timing, area and power consumption.

The project successfully established a DFEB design methodology through tape-out using commercially available design and verification tools.

Shot count analysis tools are available in every stage of the DFEB methodology. The final estimated shot count for the test chip using the DFEB methodology and the DFEB stencil mask characters represented a 10.6X reduction over the conventional method using VSB for metal 1, contact, poly and diffusion layers. Tables 1 and 2 show the post-synthesis and post-layout estimated shot count for the chip, respectively. The shot count analysis in the pre-synthesis stage is more conservative than the post-layout shot count analysis.

The DFEB test chip met the design performance, power and area goals. Tables 3 and 4 show the worst timing input and output paths, respectively. Although the timing was a few percentages off, it nevertheless met the tolerances for tape-out.

Table 1. Post-Synthesis Shot Count Analysis

<table>
<thead>
<tr>
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<th>VSB Shot Count</th>
<th>DFEB Shot Count</th>
<th>Shot Count Reduction Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard + Memories +</td>
<td>315,709,961</td>
<td>36,320,156</td>
<td>8.69</td>
</tr>
<tr>
<td>IO + IP</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Post-Layout Shot Count Analysis

<table>
<thead>
<tr>
<th></th>
<th>VSB Shot Count</th>
<th>DFEB Shot Count</th>
<th>Shot Count Reduction Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard + Memories +</td>
<td>312,856,334</td>
<td>29,572,509</td>
<td>10.58</td>
</tr>
<tr>
<td>IO + IP</td>
<td></td>
<td></td>
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Generally, it is expected that a DFEB design may trade off some performance, power and/or area for EbDW shot count. The degradation is expected to be around 5 percent for most SOC designs and negligible for the majority of SOC designs, as was the case with the test chip. The most critical timing paths can be shot with VSB with only minimal impact on the overall shot count. Therefore, managing chip area has the most critical impact since area affects both performance and power. At 65-nanometer, the total area in most SOC designs is dominated by interconnect area. A 5 percent increase in the total area occupied by the standard cells for a given netlist can often be absorbed by increasing the cell utilization rate in the standard cell sections. For most SOC designs, the overall area, performance and power will be unaffected by the deployment of DFEB, as the test chip illustrated.

Virtually Maskless SOC Design Validated

DFEB is a new approach that merges design with manufacturing to enable the use of EbDW on all critical layers of a design. This new approach has been validated through a design chain collaboration, resulting in a proven DFEB design methodology. Results confirm a significant (10X) shot count reduction while maintaining design time, area and power performance. This shot count reduction provides increased EbDW throughput to make virtually maskless SOCs practical.

The DFEB approach is especially attractive for designs that are sensitive to reticle cost and manufacturing turnaround time: derivatives, prototypes and low-volume/high-value designs. These three types of designs represent a core of innovation and potential market growth for the semiconductor industry.
Moazzem Hossain is president and chief executive officer of Fastrack Design, a member of the eBeam Initiative. Moazzem founded Fastrack Design Inc. in 2001. Moazzem has been in the industry for over 12 years working in EDA tool development and design services. Prior to founding Fastrack Design, Moazzem worked for Magna Design Automation Inc. as director of design services. He has over 50 technical publications and numerous patents in EDA and chip design. For more information, go to www.fastrack-design.com.

References

1. In e-beam lithography, proximity effect correction (PEC) is required to correct for both back and forward scattering of electrons. The effects are small enough in the case of forward scattering and large enough in the case of back scattering that the complex interaction of adjacent features associated with OPC is avoided. Thus, character projection of a two-input NAND gate is stamped the same everywhere on the wafer using EbDW.

About the Author

Dr. Tuyls initiated work on PUFs within Philips Research in 2002. PUFs are now at the heart of Intrinsic-ID's technology development. As a principal scientist, he managed the cryptography cluster at Philips Research, in which the initial research work on PUFs was carried out. Later, he transferred this work to Intrinsic-ID and headed technology development. Since 2004, Dr. Tuyls has remained a visiting professor at the COSIC institute of the Katholieke Universiteit Leuven. His inventions have resulted in numerous patents. He is widely acclaimed for his work in the security field and, in particular, PUFs. Several of Dr. Tuyls’ papers relating to PUFs have been published at leading security conferences. He co-authored the book “Security with Noisy Data,” which was published by Springer in 2007. You can reach Pim Tuyls at pim.tuyls@intrinsic-id.com or +31 40 851 90 20.

References

1. Note that in systems where the external memory is encrypted, there still needs to be an on-chip key to decrypt the data from the memory as it is being read or written.

About the Authors

Aki Fujimura is chief executive officer of D2S Inc. Previously, Aki served as chief technology officer at Cadence Design Systems. Aki returned to Cadence for the second time through the acquisition of Simplex Solutions where he was president/chief operating officer and inside board member. Previously, he was an inside board member at Pure Software and was a founding member of Tangent Systems. He currently serves on the board of Coverity Inc. Aki received his bachelor’s and master’s in electrical engineering from MIT. For more information, go to www.direct2silicon.com.

Moazzem Hossain is president and chief executive officer of Fastrack Design, a member of the eBeam Initiative. Moazzem founded Fastrack Design Inc. in 2001. Moazzem has been in the industry for over 12 years working in EDA tool development and design services. Prior to founding Fastrack Design, Moazzem worked for Magna Design Automation Inc. as director of design services. He has over 50 technical publications and numerous patents in EDA and chip design. For more information, go to www.fastrack-design.com.

HIS System Function

Together, these three modules, the PUF measurement circuit, the key extractor and the activation code constructor, comprise a powerful HIS system.

Typically, the activation code constructor is used only once in the so-called enrollment phase. The activation code constructor takes as input the PUF data and, optionally, the key that needs to be reconstructed in the future. If no key is input, a random key is determined. Once the activation code is generated, it is stored in a memory that is accessible by the key extractor. This memory may be external to the device on which the key extractor is implemented and does not need to be secure.

Each time the device needs to use the secret key, a new PUF measurement is done and the key extractor reconstructs the key from the measured PUF data and the stored activation code. This is called the reconstruction phase. The reconstruction phase is typically carried out each time the key is needed throughout the lifetime of the device. Both the enrollment and reconstruction phases are illustrated in Figure 1.

Figure 1. Schematic Overview of the Enrollment and Reconstruction Phases

During enrollment (top), the activation code constructor is used to generate an activation code depending on the input PUF data and a (user) key. During the reconstruction phase (bottom) the key extractor is used to reconstruct the same key based on a PUF measurement and the activation code.

Chip Activation: Enhancing Trust in the Supply Chain

The per-device uniqueness inherent to PUFs enables an activation step that configures the IC to become functional in its system environment. During activation, a trusted party translates the chip’s electronic fingerprint to the activation code that correctly configures the IC. This interaction can take place securely over the Internet with a trusted party, or can be deployed in tamper-proof equipment at the production line. Chip activation also includes a reporting mechanism that prevents manufacturing overproduction.

Counterfeiting Also Addressed

A secure and unclonable key storage system implemented with PUFs not only protects secret keys, but when combined with good cryptology, also provides a strong anti-counterfeiting system. The unclonable key can be used as a unique identifier and transfer its unclonability to the product in which it is embedded. To detect whether a product has been counterfeited, an authenticity check is performed—usually a protocol between a “reader” and the component to be verified.

Conclusions

Hardware cloning, theft of service and tampering are serious issues which are exacting a growing toll on semiconductor company revenue. Secret key storage is a cornerstone of hardware security, but current approaches to this critical function fall short in terms of security and cost.

A radical new approach—HIS—is available today to prevent cloning of semiconductor products and to preserve revenue. HIS uses PUFs to generate the secret key. No key is actually stored in hardware, thereby significantly raising the level of security available beyond traditional methods.

Importantly, HIS provides this enhanced security while also providing critical benefits in terms of cost, time-to-market, flexibility, reliability and trust throughout the supply chain.
by offering deep discounts to customers in exchange for publicity as their “primary vendor.” Once you’ve given your software to your customers for free, it’s very hard to come back later and get them to pay you for it. Despite what these large EDA vendors believe, this is not an intelligent strategy for beating competitors. It does not drive industry growth, increase market share or help customers in the long term. Once these vendors realize this and stop this practice, the EDA industry will grow much faster.

The shift towards adopting a traditional software business model will also drive growth in the EDA industry. The industry has already transitioned from providing perpetual licenses (i.e., revenue is recognized upfront) to time-based licenses (i.e., revenue is booked quarterly), and I believe we will make one more transition to a project-based licensing model. With this new model, companies do not have to sell software off-the-shelf. We’re looking at transitioning a few of our product lines to a project-based licensing model, and we plan to lead the industry in making this transition.

Q: The convergence of more features in today’s electronic products has increased chip design complexity and cost. How is Magma assisting chip companies in tackling design complexity and decreasing software and verification costs?

A: Today, a greater number of engineers must be employed to develop complex products. However, this practice defeats the rationale of Moore’s Law (as more transistors are put on a chip, the cost to make each transistor decreases) because it actually increases costs. Magma has taken a unique approach to addressing design complexity by automating the chip design process. Within the next few months, the industry will see many companies taking advantage of this approach, displaying the value Magma offers in reducing chip complexities.

To help customers further reduce costs by shortening turnaround time, we’ve designed our products, including our circuit simulation and physical verification solutions, to leverage multiple central processing units (CPUs), which enables significantly faster runtimes. There will be many more of Magma’s tools using multi-CPUs to reduce costs and increase productivity in the future.

Q: Smart grid technology is attracting great interest from investors as the importance of alternative energy sources becomes a focal point of governments worldwide. How does Magma plan to contribute to the advancement of smart grid technology?

A: We are currently working with a number of solar companies to make our process manufacturing software, such as Camelot and YieldManager, relevant and help improve the performance and yield of chips used in smart grid technologies. Magma recently formed a partnership with Orion Metrology, a supplier of inline process monitoring and control tools to solar cell manufacturers. Through this partnership, Magma’s YieldManager Solar will integrate with Orion Metrology’s inline inspection technology to enable photovoltaic (PV) solar panel manufacturers to speed up defect identification and improve process control.

I believe the industry’s development in sensing and mixed-signal technology will be required to advance smart grid projects. To successfully integrate these technologies with the smart grid market, we need to thoroughly understand what types of chips are being produced in the sensing and mixed-signal markets and ensure the software we market can be used efficiently and quickly without much human effort.

Q: There are a great number of EDA start-ups saturating the marketplace. Though these companies are powerhouses of innovation, many are finding it difficult to obtain funding. In a recent EDA DesignLine article, author Nicolas Mokhoff stated that Mark Stevens, a principal at Sequoia Capital, has been studying a model used in the biotech industry where large companies help fund start-ups and then buy the companies once their products are complete. Since large, mature EDA companies tend to focus more on sales of existing products than developing new technology, could this business model be applied to large EDA companies to keep innovation alive? How does Magma prioritize its research & development (R&D) activities?

A: This business model has been evident in the EDA industry for the past few years. Magma has followed this strategy by investing in a number of companies that develop leading-edge technology and acquiring them during their early product stages. We recently funded a company whose products are just hitting the market and look forward to helping them succeed. Magma funds companies that we feel solve industry challenges and promote innovation. For example, we still have significant investments in one of the fastest logic simulation tools in the market, which addresses a significant problem area in verification.

We prioritize our R&D activities based on the level of differentiation the product offers. If the product developer cannot explain the competitive advantage of a proposed, new product in a 30- to 40-second elevator pitch, then we will not pursue it. During this recession, it is imperative to only support products that provide something unique to the market.

Q: Two leading EDA standard organizations, Accellera and The SPIRIT Consortium, recently announced their plans to merge. The merger intends to fuse the language-based design and IP-assembly worlds. How will the combined organization’s single view of the design process impact the development of future standards that will meet the needs of the EDA community and its customers (i.e., where will standards be going in the future)?

A: For the standards industry to successfully meet the needs of the EDA community, I would encourage the standards bodies to merge. For example, Accellera and The SPIRIT Consortium should merge with the standards body Silicon Integration Initiative (Si2). It took a tremendous amount of effort for Magma to support both Accellera and Si2 with relation to Common Power Format/Unified Power Format (CPF/UPF).

Today, the EDA community cannot afford to have multiple standards bodies. It was possible when the industry was in its early stage and files and formats were not being tracked. In reality, files and formats from the most widely used tools are what become de facto standards. Magma is fortunate in that our software’s architecture makes it much easier for our tools to read any files or formats regardless if they are standard or not—because of this, we can focus on supporting our customers rather than supporting standards.

Q: Magma has criticized the emerging trend of chip companies announcing specific EDA suppliers as their primary vendor, stating that the announcements prevent innovation and hurt product pricing. Are chip companies or EDA vendors more likely to feel the effects from these exclusive partnerships? How can Magma and other companies combat this practice?

A: I strongly believe that the primary vendor and flexible access models that the larger EDA companies are adopting are extremely detrimental to the industry. I know from firsthand accounts of these vendors offering a discount of 30 percent in exchange for publicity as a primary vendor. This can actually work to Magma’s advantage...
because the money that customers save on these deals with the large EDA companies often gets spent on Magma’s, or other, EDA software. So while the large EDA companies may get a press release, these deals don’t prevent Magma from making a software sale. The other problem with these deep-discount deals is that they don’t cover the EDA vendor’s support costs.

To combat these practices, Magma will simply continue to focus on producing differentiated, superior products and ensure that chip companies invest the money they save from the primary vendor deals in Magma, which is already occurring. We will continue to be profitable, while other companies shoot themselves in the foot by reducing their prices.

References

1 Harvard Business Review.
Don't miss the 2009 GSA Emerging Opportunities Expo & Conference, focused on energy harvesting, the innovation business model, medical applications, cloud computing, home networking, mobile gaming and smart grids. With up to 75 exhibitors showcasing their latest products and services, the Expo and conference will provide valuable networking opportunities to meet one-on-one with supply-chain partners.

2009 CONFERENCE PROGRAM

8:30 a.m. Show Floor Opens
9:00 a.m. Research Analyst – Jim Feldhan, President, Semico Research
9:15 a.m. “The Innovation Imperative” Business Model
Doug Grose, CEO, GlobalFoundries
9:45 a.m. Morning Snack - Sponsored by Tensoft
10:15 a.m. Research Analyst – Jeff Shepard, President, Darnell Group, Inc.
10:25 a.m. Energy Harvesting
Peter Henry, Vice President & General Manager, Power Management Group, Analog Devices Inc. (ADI)
11:15 a.m. Research Analyst - Matthew Towers, Founder & CEO, IMS Research/InMedica
11:25 a.m. Small Footprints SoC Enables Precision Portable Medical Instrumentation
Murugavel Raju, AEC Catalog Microcontrollers End Equipment Marketing Manager, Texas Instruments
12:00 p.m. Lunch on Show Floor - Sponsored by GlobalFoundries
1:15 p.m. Research Analyst - Mario Morales, Vice President, Global Semiconductor Research, IDC
1:25 p.m. Opportunities for High Performance Semiconductor Solutions in Cloud Computing
Dr. Francis Ho, Senior Director Business Development, Inphi Corporation
2:15 p.m. Research Analyst - Tony Massimini, CTO, Semico Research
2:25 p.m. Enabling 3G Wireless Digital Distribution in Emerging Markets
John Rizzo, CEO, Zeebo, Inc.
3:00 p.m. Afternoon Snack - Sponsored by Exar Corporation
3:15 p.m. Research Analyst - Joanne Itow, Managing Director, Semico Research
3:25 p.m. Home Networking: Opportunities and Challenges
Vinay Gokhale, Senior Vice President Marketing & Business Development, Entropic Communications
4:15 p.m. Research Analyst - Farah Saeed, Senior Consultant, Energy and Power Systems, Frost & Sullivan
4:25 p.m. Making a Smarter Grid
Robert Dolin, Vice President & CTO, Echelon
5:00 p.m. Networking Reception on Show Floor