LOW-POWER DESIGN INCLUDES LOW-POWER VERIFICATION

2012 END MARKETS: OPPORTUNITIES AND CHALLENGES

EMERGING PORTABLE CONSUMER DEVICES DRIVE THE NEED FOR HIGH PERFORMANCE POWER MANAGEMENT ICS (PMICS)

LITHOGRAPHY DRIVERS FOR MOBILE CONNECTED DEVICES

SOLVING VERIFICATION ISSUES FACING SEMICONDUCTOR COMPANIES PRESSURED TO GET PRODUCTS TO MARKET

Global Semiconductor Alliance

Semiconductors: The Engine of Consumer Electronics
GLOBALFOUNDRIES has shipped >250,000 32/28nm HKMG wafers to date. The milestone represents a significant lead over other foundries in HKMG manufacturing.

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The tradition of rapidly ramping leading-edge technologies to volume production continues.
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MISSION AND VISION STATEMENT

ACCELERATE THE GROWTH AND INCREASE THE RETURN ON INVESTED CAPITAL OF THE GLOBAL SEMICONDUCTOR INDUSTRY BY FOSTERING A MORE EFFECTIVE ECOSYSTEM THROUGH COLLABORATION, INTEGRATION AND INNOVATION.

- Address the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging
- Provide a platform for meaningful global collaboration
- Identify and articulate market opportunities
- Encourage and support entrepreneurship
- Provide members with comprehensive and unique market intelligence

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here is currently a general consensus among industry analysts, investors and company executives that leading-edge digital chip development projects cost between $30 million and $100 million to develop. This negative view of chip development costs has led to severely decimated levels of VC investments and has even led to some companies scrapping entire product lines. Today's chips have a bigger impact on the world economy than ever, and reduced investments in chip product development will eventually have a very negative impact on the economy. China, for one, has realized this and is pouring billions of dollars into their local semiconductor economy. This article will go through some of the reported data and show that present assumptions regarding chip development costs are very much exaggerated, and that it is possible to design state of the art chips at a fraction of the cost previously reported.

Why is Chip Development so Expensive?
Chip development has never been cheap and there is no question that it's only getting more expensive. The million dollar question is: “how much more expensive?” The consensus among industry pundits is that there is no way to do a leading-edge chip with less than $30 million to $100 million. Let's take a look at some of the most common arguments for the “exponential” increase in chip development costs.

“Mask Costs are Increasing Exponentially!”
It used to be that you could design a product with production mask costs in the range of $100 thousand. Today, production mask costs at leading nodes can cost $1 million to $2 million. This has the effect of increasing the minimum market size that is practical to address with a leading-edge chip design. Still, given a decent size market or high chip selling prices, mask costs are certainly not show stoppers, and don’t explain the $100 million price tag.

“EDA Tools are Getting Really Expensive!”
While electronic design automation (EDA) tools are certainly not cheap, aggressive volume purchasing agreements, increased feature integration and increased efficiency in the tools have made today's tools far more cost effective than those of 10 years ago. Today many leading chips can be taped out using vanilla flows derived from reference scripts provided by EDA vendors. Thus, per transistor and per project, the cost of EDA tools has actually gone down in the last 10 years.

“Deep Sub-Micron Design is Really Hard!”
Chip design is certainly getting more difficult as we move to finer process geometries. At 0.35um and above, life was simple. Gates were slow, wires were fast and there was virtually no leakage to speak of. The only problem was that chips were slow, power hungry and big! Since then, the design constraints and difficulties have been piling on with every process node. In order of introduction, designers have had to learn and deal with: wire delays, voltage drops, signal integrity, leakage, process engineering effects like stress, and most recently on-chip variability and an explosion in the number and complexity of device design rules. The introduction of each one of these effects was painful, but within one process generation, the EDA industry always seemed to find automated methods of dealing with them, thus keeping engineering team growth to a minimum. Deep sub-micron chip design is definitely not for hobbyists; but for a small expert team equipped with state of the art tools, it is today possible to accomplish in weeks what used to take a generously sized team six to nine months.

“Chips are Getting Incredibly Complex!”
Bingo! The simple reason for the explosive growth in chip design costs is that design complexities are growing exponentially thanks to Moore’s Law. At leading-edge nodes, it is now possible to integrate complete multi-billion transistor computer systems on a single chip. The more complicated the system, the more complicated the chip. Complicated systems-on-chip (SOCs) are indeed very expensive to develop and there are few if any examples of complete products that have cost less than $10 million from start to finish. An application-specific IC (ASIC) on the other hand tends to solve a very specific problem and be a key part of a larger system. The limited generality of ASICs can lead to much higher performance levels and generally results in reduced complexity and development. For a great discussion on the relationship between project complexity, team sizes and project costs, I highly recommend reading “The Mythical Man-Month”, by computer legend Fred Brooks. Unfortunately, there aren't a lot of short cuts for saving costs when projects are complex and need to be completed in a short time. Note that complexity drives up development costs of any project, regardless of the underlying implementation fabric. As many designers are discovering, large field programmable gate arrays (FPGAs) have all of the complexity problems of large SOC design, minus the long turnaround time and costs of manufacturing.
the-art SOC for a fabless semiconductor company. The data is based on personal experiences and numerous informal interviews with executives at chip startup companies who spent up to $50 million without reaching break-even.

Despite the large EDA tool component and mask building costs, the largest project cost by far is engineering. Figure 2 illustrates the biggest issue with the large burn rate business model shown above. It’s incredibly sensitive to delays in “time to money”, whether the delays are due to design slippage or the market materializing late. The figure shows three potential sales models with different degrees of eternal optimism built in. Anyone involved with semiconductor product sales knows that it’s incredibly hard to get to $10 million in profits for a chip product per year. The good news is that if you do, the potential upside is huge. The downside for startup companies without deep pockets is that if the company runs out of money before profitability is reached, it is again at the mercy of investors and/or macro-economic conditions. Many companies on the verge of greatness went out of business in 2008 because they ran out of money at the wrong time. Since time to sales carries the most amount of uncertainty, reducing the R&D expenses though the initial sales period can significantly increase the likelihood of success, given a fixed investment size.

Choose your Market

As discussed, the biggest contributor to semiconductor development cost is design complexity. The easiest way to reduce design complexity is by picking the right market. The market will drive feature sets and chip selling prices. By far, the most extreme example is the SOC application processor in a cellular phone. Half a billion transistors, every input/output (I/O) interface one can think of, and yet the average selling price is often less than a large latte at your local café. This is not a good space for a startup, as the total investment in software and hardware could actually reach $1 billion at the end of the day!

Markets that are not quite as cost and space sensitive have a huge advantage in terms of development costs savings, because they allow companies to leverage existing chips in the market to make chip set solutions that satisfy the system requirements. For example, it is possible to buy off the shelf FPGAs and/or microcontrollers for $1 to $10 that will give a system a complete host computer and every connectivity standard in the book. High-end I/O Internet protocol (IP) such as PCI express (PCIe), DDR, universal serial bus (USB) and Ethernet are very expensive to design into SOCs and choosing all of them on a single chip adds a lot of cost and risk to a project. It’s not just the purchasing costs, it’s also the integration, validation and testing costs; in addition to the sticker price. The trend towards inexpensive mid-end FPGAs is especially encouraging, as it allows the fabless startup company to go after a large number of markets with a single chip platform. Software development costs also have a huge impact on product development. Some markets demand that chip vendors develop the whole software stack and give it away for pennies. Unless you are designing a system solution, and get a good return on investment, always focus on “teaching your customer to fish, rather than giving him the fish for free”.

Further Cost Cutting Measures

Figure 3 shows the manpower breakdown for a typical modern fabless semiconductor startup company. On average, the SOC startup team seems to ramp up to approximately 75 engineers quickly, and stay at that team size until eventually ramping up towards an exit or going out of business.

If we turn the fabless semiconductor business model on its head and ask the question: “What could be done about spending if we are willing to give up time and some down the road profits, instead of trying to minimize time to product at all costs?” Let’s go through each one of the expense categories, and look at some things that could be done to reduce costs:

- Software: Many chips today are sold with a complete accompanying software stack. The big problem is that the chip vendors rarely get properly compensated for the software by original equipment manufacturers (OEMs). The question posed is often: “Why should we pay for the software? We can’t use your chip without it and we really aren’t interested in learning the inner workings of your chip to be able to program it ourselves”. Two potential solutions to reducing software R&D include: 1.) Design your architecture so that you can leverage existing open source software packages (e.g. make it
The demand for semiconductor devices used in radio frequency (RF) applications like smart phones and wireless local area networks (WLAN) has dramatically increased at an average growth rate of more than 20 percent over the last couple of years. As this demand increases, so too does the speed and capability required of these devices. RF automatic test equipment (ATE) is used for the high-volume production testing of these devices. The instruments of an RF ATE system are more complex than bench equipment, in that the set-up and control of the instruments take place within a highly integrated programming environment. Speed and accuracy are needed in RF ATE systems, because the volume of RF devices tested can be in the millions of units per month. Unit volume and complexity of the RF devices are also growing, as RF standards continue to proliferate. As a result, the RF ATE requirements are also increasing. Smart phones become more capable every year, but are also becoming cheaper and cheaper at the same time. This article will outline the current RF applications trends and discuss cost reduction concepts.

**Current RFIC and RF System-on-Chip (SOC) Market Developments**

**Growth in Unit Volume, Competitive Cost and Time-To-Market Pressure**

One main driver in the wireless semiconductor market is handset RFICs, which today generate more than 50 percent of the overall revenue for this market. Handset volumes continue healthy growth and reached 1.6 billion shipments in 2011. At the same time, the RFIC revenue has grown at an average rate of “only” 11 percent per year. The key reason for the disparate RFIC revenue (11 percent) versus handset shipments (20 percent) is the decline of the average selling price by roughly eight percent per year. Examining the iPhone bill of materials and comparing the 3G and 4G components, the RF transceiver device price erosion totaled a stunning 17 percent. This has a direct impact on the progression of device test costs. Typically, the annual cost-of-test (COT) reduction goal is in the range of eight percent.

Besides costs, time-to-market (TTM) becomes a key differentiator. To compete for business for key applications like the iPhone and iPad with steep production ramps and extremely high volumes, it is mandatory for semiconductor suppliers to deliver on time with the requested quality and volume. It is a winner-take-all type of business and timelines must be maintained.

**Continued Proliferation of Standards, Integration and Complexity Growth**

RF standards continue to proliferate, which implies a broader range of test requirements. In addition to the 2G/3G/4G telephone technologies, modern smart phones contain global positioning systems (GPS), frequency modulation (FM) radio, Bluetooth and WLAN. Signal bandwidth and carrier frequencies supporting higher data rates are steadily increasing, and new standards for wireless communications are expanding mobile handset capabilities at a relentless pace. Some good examples are the evolving WLAN standards 802.11a/b/g, 802.11n and the future 802.11ac with various throughput capabilities, carrier frequencies and bandwidths. In addition, new RF developments need to maintain compatibility with previous standards, enhancing value of both the wireless network and the new technology. As a result, previous generation hardware, which otherwise might have been eliminated by an emerging new standard, is often still required. This has a direct impact on the tester RF pin-count requirements. 3G cellular RF transceivers include both existing quad-band GSM/EDGE standards and dual-/tri-band WCDMA capability. While GSM/EDGE transceivers typically have five or more RF connections, WCDMA with its diversity, can receive channels and add as many as nine additional RF pins, depending on the actual implementation of the RF chip.

**RF Integration to SOC and System-In-Package (SIP)**

Another trend is the RF integration to SOC and SIP. Higher chip integration helps to reduce manufacturing costs and enables smaller products. The primary focus today is more functionality at an affordable cost and effort. Comparing again the bill of material of
iPhone 3G vs. 4G, it becomes apparent that integrating additional RF standards helps to protect the chip price. Today’s RF SOC/RF SIP devices incorporate the RF transceiver and digital/analog baseband with integrated power management. While these devices typically target the low-cost market, such as that in China, they add new test challenges. Due to the increased complexity, more tests increase test times. Higher parallelism can be used to counteract the increasing test time, but increasing parallelism for high pin-count RF SOCs forces the tester configuration to 60+ RF ports, together with 1,000+ digital pins and 70+ power supply pins.

Need for High Performance and High Quality Test at the Wafer Level

Compared to RF SOCs, RF SIPs are more flexible. SIPs offer faster time-to-market due to performance and cost-optimized front-end fabrication processes. However, SIPs add a cost layer from yield loss due to the multiple known good dies (KGDs) attached to the SIP substrate. Any of the dies can induce a failure and need to be tested at wafer level.

Another cost reduction trend is the usage of wafer-level chip-scale packaging (WL CSP). In this case, the die is mounted on an interposer, upon which pads or balls are formed; or the pads are etched directly onto the silicon wafer, resulting in a small chip package very close to the size of the silicon die.

RF test at probe becomes more and more common. This requires not only optimal signal integrity, but also much larger component space on the probe card to allow higher multi-site testing. Using a direct probe solution can enable a single-load board to be used for both wafer probe and final test. This reduces the time between IC development and production, minimizes the correlation effort between probe and final test and enables higher multi-site capability. Octal site RF probe is already a reality today.

Impact of Market Developments on ATE and RF Test

ATE Needs to Cover the Broadest RF Test Needs

The market developments can be summarized as follows: RF unit volume, as well as device complexity are increasing, while product life cycles and average selling prices are decreasing. The standard answer to this challenge so far has been to provide a more complex tester with a more bulky infrastructure to house all the extensive configurations. While this might be necessary for the leading edge and highly integrated RF transceivers and RF SOC devices, it is overkill and too expensive for RF connectivity or combo chips. The additional infrastructure simply adds too much unnecessary cost to the test solution. Depending on the actual configuration, an unsuitable tester infrastructure can add as much as 20 percent to the overall system price. Another 10 percent to 20 percent can be saved, if the tester configuration is matched to the actual application needs.

On the other hand, even low-cost RF devices share the same demodulation requirements, so compromises on tester performance cannot be accepted. Separating and targeting RF ATE platforms for different applications is also not a good choice, because the intersections are floating and quickly changing over time. Today’s optimized solution most will likely become obsolete over the lifetime of a device or with its next generation. Switching from one ATE platform to another incompatible platform places a large risk on TTM and will add significant switching costs, which can easily reach into the six-figure range.

A wireless test solution today needs to cover a broader range of devices with different levels of complexity than it did 10 years ago (Figure 1). On the low end, it needs to cover very cost sensitive connectivity devices and front-end modules (FEM), and on the high end it needs to be able to test devices with multiple RF ports, covering a variety of standards combined with mixed signal, digital, power management and embedded or stacked memory testing requirements.

Outlining the Architecture of a Scalable and Compatible RF ATE Platform

The need for covering a wide range of applications results in unprecedented asset utilization and manufacturing flexibility. Due to the boundary requirement to have similar RF, analog and digital performance over the full application range, a scalable platform approach provides the best test economics. A scalable platform has consistent operating software, allows exchanging the same hardware modules from one system to the other (digital, analog, RF, etc.) in a choice of compact, small or large test head classes and device-under-test (DUT) board reuse; and makes use of the same docking hardware and positioning, therefore enabling a consistent prober and handler set-up over the whole test floor.

The compatible, high-throughput tester classes (Figure 2) must have focus on different RF applications - each with an optimized infrastructure:

- Low-cost infrastructure with focus on dual or quad site testing of low-integration and cost-sensitive RF devices; ultra-small footprint, ideal for lab development and high-volume production; allows minimum capital cost or hourly rate at outsourced assembly and test (OSAT) companies.
- Low-cost and zero-footprint infrastructure with focus on quad or octal site testing of mid-integration RF devices; allows a high degree of configuration flexibility.
- High parallel test infrastructure for low COT of most complex RF SOC/RF SIP devices; it may need 2,000+ digital pins, 100+ power supply pins and 48+ RF pins.

See ATE Trends page 27
China’s Impact on the Semiconductor Industry

Raman Chitkara, Global Technology Industry Leader, PricewaterhouseCoopers LLP

PricewaterhouseCoopers began studying China’s impact on the semiconductor industry in 2004 in response to its clients’ interest in the rapid growth of the semiconductor industry in China, and their concern regarding whether China’s production volumes would contribute to worldwide overcapacity and a subsequent downturn. Since then, it has become clear that China’s consumption of semiconductors is far more significant to the worldwide semiconductor industry than either its industry production volumes or device sales.

China’s Consumption of Semiconductors

China has grown to be the dominating consumer of semiconductors. Figure 1 shows the growth and distribution of the worldwide semiconductor market by region for the eight years 2003 through 2010. The vertical bars represent the size of the total worldwide market and the circles represent the relative size of each region’s market, arranged by size, with the smallest on the bottom. China, which is the bottom smallest circle on the left (in 2003), moved up rapidly to become the largest upper circle (and largest regional market) by 2005.

Figure 1 Worldwide Semiconductor Market by Region, 2003 -2010

Sources: SIA, CCID

During the last decade, China’s consumption growth has outrun the rest of the world for nine of the 10 years. China’s share of worldwide semiconductor consumption had grown from six percent in 2000 to more than 40 percent in 2009 and 2010, and from being the smallest regional market in 2003 to the largest by 2005. China’s semiconductor consumption has exceeded the markets in Japan, Europe, Americas and the rest of world for six consecutive years, and its market growth and increase in market share has been at the expense of decreases in all other regional markets.

Figure 1 will only be updated when China’s final 2011 reports are released. Based upon preliminary data, we understand that China’s semiconductor consumption market grew 16 percent in 2011 to a record $156 billion, almost 48 percent of the worldwide market, while its semiconductor industry production remained slightly less than 11 percent of worldwide semiconductor value added, and Chinese semiconductor companies accounted for about three percent of worldwide semiconductor sales revenues.

China’s market has continued to grow more than six times as fast as the worldwide market, as a result of two driving factors: the continuing transfer of worldwide electronic equipment production to China, and the above-average semiconductor content of that equipment. China’s share of electronic equipment production, which had increased from 17 percent in 2004 to 32 percent in 2010, increased further to 33.2 percent in 2011;
while the semiconductor content of that production averaged 25 percent compared to the worldwide average of about 20 percent. Even during the global recession in 2008 and 2009, China's electronic equipment production value grew, while worldwide production decreased.

The major global semiconductor companies continue to dominate the Chinese market, and the largest suppliers to the Chinese market continue to be the same multinational semiconductor companies. In the last nine years, there have been only fourteen different companies among these top 10 suppliers, eight of which have been among the top 10 semiconductor suppliers to China every year from 2003 through 2011. These companies include Freescale, Hynix, Intel, NXP/Philips, Samsung, ST Microelectronics, Texas Instruments and Toshiba. There were no Chinese companies among the top 40 suppliers to the Chinese semiconductor market in 2011.

While the consumption of semiconductors used in components of finished products assembled in China and exported for sale in other countries has been the major contributor to the growth of China's semiconductor consumption market, China's domestic market is growing in significance to the global semiconductor industry. China's domestic market — the value of semiconductors consumed in China that are used in components of finished products assembled and sold in China — has risen from $10 billion in 2003 to more than $46 billion in 2010. By itself, China's domestic consumption market has made up more than 27 percent of total worldwide semiconductor market growth since 2003. Largely driven by China's economic stimulus package, with its focus on increased consumption of electronic consumer products, China's domestic market grew to represent more than 15 percent of the worldwide semiconductor market for the past three years. That growth is often credited with initiating or leading the industry's recovery from the depths of its decline in Q1 2009.

### China's Semiconductor Production

Figure 2 shows the relative size and market share for the four sectors of China's semiconductor industry from 2003 - 2010. It will also be updated when China's final 2011 reports are released. Based upon preliminary data, we understand that China's semiconductor industry grew 13 percent in 2011 to a record $43 billion. Individual sector growth varied from a low four percent for IC packaging and test, to a high of 40 percent for IC design. As a result, the distribution of China's 2011 semiconductor industry was optoelectronics-sensors-discretes (OSD) at 42 percent, IC packaging and testing at 23 percent, IC manufacturing (IDMs plus foundries) at 18 percent and IC design (fabless) at 17 percent. China's semiconductor production in 2011 will have accounted for at least nine percent and possibly 11.4 percent of the worldwide semiconductor industry, up from just two percent in 2000.

![Figure 2. China's Semiconductor Industry by Sector, 2003-2010](image)

Source: CCID, CSIA, PwC 2004-2010

Over the past 10 years, China's semiconductor industry production, although much smaller than its consumption, has grown at a 24 percent compounded average growth rate (CAGR), much faster than the worldwide industry at an eight percent CAGR, but slightly less than China's consumption at a 25 percent CAGR. Much of that growth was contributed by multinational IDMs, who until 2011, made up four of the five largest semiconductor manufacturing enterprises in China. The top two, Intel and Hynix, contributed more than half of China's semiconductor industry revenue growth in 2011, as they ramped into full production the fully vertically integrated IC manufacturing capabilities they had completed in China during 2010.

All Chinese fabless companies include IC design as a product offering, and so therefore do most Chinese semiconductor companies. It is the only segment of China's semiconductor industry that achieved positive year-over-year growth for every year of the past decade. It was also the fastest growing segment of China's semiconductor industry for this decade. Thanks to booming domestic demand, China's IC design industry even grew during the 2008/2009 downturn. Mobile devices became the major products for China's IC design industry during 2010, as companies in the communications sector, particularly mobile phones, achieved rapid growth in revenue and size, while those in the IC card sector experienced relative decline. The result is a significant change in the makeup of China's top 10 IC design companies. Based upon preliminary data, we understand that China's IC design sector grew by almost 40 percent in 2011 to a record $7.5 billion, which would represent 11.6 percent of total worldwide fabless sales and 2.5 percent of total worldwide semiconductor sales. The number of IC design enterprises in China increased to 503 with 32 of those companies having more than 500 employees. The largest, HiSilicon Technologies, a subsidiary of Huawei, reported a 51 percent increase in sales revenue in 2011 to just over $1 billion (including internal sales to Huawei) becoming the first Chinese semiconductor company to reach this level.

### Conclusion

Figure 3 shows the difference between IC consumption and production in China. This is described as China's IC Consumption/Production Gap. This gap is the annual difference between China's IC consumption and IC production revenues. It continues to grow despite all of the Chinese government's plans and efforts to contain it. This annual gap had grown from $6 billion in 1999 to a record $87 billion in 2010—and based upon preliminary data we understand it grew by another $16 billion in 2011 to $103 billion. Chinese authorities now expect this trend to continue through at least 2014, providing continuing motivation for the Chinese government’s initiatives to increase indigenous production.
The idea of low-power design for portable consumer electronics is nothing new. Battery life has been an issue for as long as there have been portable devices, and efforts to reduce power consumption have played a critical role in shaping the landscape of IC and semiconductor development for decades.

One of the key factors contributing to the widespread adoption of CMOS technology in modern application-specific IC (ASIC) and system-on-chip (SOC) design was its inherent low-power characteristics. As design complexity increased over the years, the need for low-power implementation techniques has driven the development of new tools, standards and methodologies from the electronic design automation (EDA) industry.

**Power-Aware Functional Verification**

Today, power management is having a significant impact on the evolution of functional verification. Modern devices such as smartphones and tablets are placing aggressively competing integration and power requirements on chip developers, and with time-to-market pressures driving up the cost of failure, the need to verify functionality in various power scenarios prior to tapeout has become critical. Design teams would be well advised to consider power-aware functional verification as a part of their global power strategy.

In the early days, as with other aspects of IC design, developers would manage power through mostly manual efforts. Power consumption would be balanced against performance, area and other factors through transistor sizing, voltage (VDD) selection and clock gating. At the time, dynamic or switching power consumption was the dominant power factor in CMOS technology processes. Verification too was a manual affair; with engineers performing logic simulation using directed testbenches on their Verilog or VHDL designs. Since transistor sizing and voltage are concepts that get abstracted out in digital logic simulation, the only power-saving technique that required functional verification was clock gating, typically implemented as register-enabled logic. This type of functionality was easily compatible with logic simulation and could be tested at the block level.

Jumping forward to the present, after years of shrinking process geometries, increasing complexity and the actualization of Moore’s Law, many ASIC processes have been automated and much of the designer’s work has been raised to a higher level of abstraction—including power management.

Power management is now tightly integrated throughout the ASIC and SOC design implementation process via automated or semi-automated EDA tools. These tools fulfill power-intent through a myriad of power-optimization techniques applied at the circuit, block and system-level. Many of these techniques still follow the same core philosophies—adjusting transistor properties, voltage levels and gating—of those used in the past; but now applied to a modern ASIC design flow, and considering the characteristics of current device geometries.

Individual transistors are no longer resized and laid out manually; rather, ASIC libraries now include low-power and low-threshold (Vt) standard cells to be applied in synthesis and place & route. Multi-VDD designs are now commonplace, with dynamic voltage scaling applied at the circuit level, and voltage islands with level-shifting applied at the block and system level. And with leakage power becoming an increasing factor in smaller geometries, clocks are no longer the only signals being gated. Power gating or switching, implemented via high-Vt sleep transistors, shuts off VDD when the power domain is inactive.

**Challenges in Functional Verification**

How do these new power-optimization techniques, now applied in an ASIC flow, affect functional verification? In fact, aside from the register-enable logic of clock gating, most ASIC power-optimization techniques are not functionally coded into the initial register-transfer level (RTL) design at all. Rather, the required standard cell or circuitry is inserted by the implementation tool based on a separate description of the designer’s intent, typically defined using the Unified Power Format (UPF) or Common Power Format (CPF). This methodology is aligned with the basic precepts of EDA implementation technology, where developers are meant to focus on the core functionality of the design, and let the tools manage the low-level insertion of logic and circuitry for more general features.

As a result, much of the functional verification of power optimization is performed as it would be with any other implementation processes—through logic equivalency checking.
Equivalency checking statically verifies that the power-optimized netlist is functionally equivalent to the original one; and indeed, this method is ideal for many low-power optimizations. No functionality should be changed when swapping standard threshold cells with low-Vt ones. Further, since digital simulators and emulators don’t care about voltage levels and thresholds, dynamic functional verification would be ineffective for testing the level-shifting required for multiple VDD islands.

On the other hand, some power-optimization techniques applied during implementation are not appropriate for static verification and logic equivalency checking, because they change the functionality and the state of the design from the original RTL code. Looking at Figure 1, when the power-gating control logic circuit switches off the Virtual VDD of a power domain, the register contents of that domain are erased. Further, when that block is powered up again, the state of the register contents are indeterminate. These power scenarios cannot be functionally verified statically, and require dynamic verification through simulation and/or emulation. However, adding a power-aware component to dynamic functional verification presents a number of challenges.

**Figure 1: Clock and Power Gating Circuit**

One of the biggest challenges to power-aware, dynamic functional verification is one that chip developers are already well familiar with—verification bandwidth. With consumer electronics devices routinely exceeding 15-million gates and requiring pre-tapeout software development for system-level realization, logic simulators—the traditional choice for dynamic functional verification—are already at the limits of their capacity and performance. The introduction of power-aware verification only exacerbates the problem.

Each power-switching domain introduces at least two new verification scenarios: (1) the cross-domain scenario, which verifies the behavior of other domains when a power domain is turned OFF; and (2) the intra-domain scenario, which verifies the behavior of a power domain after it is turned ON again. The more power domains, the worse the problem gets, as the number of new verification scenarios increases exponentially. Furthermore, these power scenarios must be verified at the system-level, where all of the power domains have been integrated.

Even the venerable clock-gating has an impact on verification performance and capacity. At a minimum, an AND-gate (shown in Figure 1) is required to implement clock gating. But in practical application, a larger circuit, usually involving a latch to prevent glitches, is used. The number of clock domains has also gone up over the years, further increasing the size and complexity of ASIC designs. Ten years ago, a typical design might have contained a handful of clock domains—now, that number has easily increased to more than 20, and in applications such as mobile, can regularly reach up to 100.

Other challenges for functional verification are more specific to power switching, especially given the general incompatibility of voltage with digital netlists. RTL functionality is not affected by VDD, and even gate-level netlists may not connect VDD signals or consider power in their logic tables. Power switching behavior is only really described in the power-intent UPF/CPF files. This contrasts with clock-gating, where the suppression of the clock is recognized in the behavior of the netlist.

The indeterminate nature of power switching also presents challenges for functional verification in terms of debugging. The UPF defines power domains as containing “X” states when turned OFF, which results in greater complexity. In synthesis, an “X” is interpreted as a “don’t care,” while in simulation it is unknown or indeterminate. Chip developers are well aware that these two usages are not the same, and can result in missed corner cases and unexpected behavior.

**New Requirements in Verification**

Overcoming the challenges of dynamic, power-aware verification places new requirements on verification tool suppliers, and requires careful consideration from project managers and verification engineers when developing their verification strategies. No tool is perfect, and each comes with its own strengths and trade-offs that will affect power-aware verification.

For example, both simulation and emulation provide the means to meet the increased verification bandwidth requirements of power-aware verification, but through vastly differing approaches. Using simulation, overall throughout can be increased with more licenses and larger compute farms. But, running more jobs in parallel won’t improve the time to complete a single system-level test. Running a realistic power scenario may require first booting Linux on the SOC processor, which could take hours or even days in simulation. Meanwhile, emulators can supply multi-MHz execution of system-level tests, but their relatively higher cost usually prohibits teams from access to more than a few emulation resources at a time, and tests must be run serially.

A similar situation can be seen with verification tools in their support for power-intent. By now, all of the major simulators and most commercial emulators have introduced support for UPF, and/or CPF-based power intent, but again, each tool has its advantages and disadvantages.

Emulators aren’t able to support the UPF specification to supply an “X” for power-gated circuits, because in real hardware there’s no such thing. As a result, emulators must supply other alternatives, such as pseudo-random state values that can be executed repeatedly using different seeds. This diverges from the UPF definition; however, in some cases this behavior is advantageous over that of simulation, which can provide the specified “X” value. In simulation, a memory write to an “X” address may not change any memory contents, but in the real hardware, an actual memory location will be written to. On the other hand, “X” propagation in simulation comes in handy for debugging once a failure has occurred.

A single platform approach to power-aware functional verification creates the potential for verification bottlenecks, missed corner cases and debugging challenges. Rather than focusing on the individual strengths and weaknesses of a particular tool, perhaps a combined, complementary approach would yield better results. Using both emulation and simulation for power-aware verification would balance the verification bandwidth against cost, and provide coverage of both simulated and “real” behavior. And if emulation and simulation providers partner to ensure matching cross-platform behavior in
At the digital revolution continues to change the way we communicate, play, work and travel, semiconductor companies are faced with many challenges in satisfying consumer demand. In my interview with Samuel Fuller, chief technology officer and vice president, research and development at Analog Devices, we discussed the technology ADI has available to address these challenges; its recent product expansion and offerings; satisfying end-user demand with shorter time-to-market goals; and much more.

— Jodi Shelton, President, GSA

SAMUEL H. FULLER
CTO and VP, Research and Development, Analog Devices Inc.

Q: As the digital revolution continues, moving to higher speeds and multimedia, and thus changing the way we communicate, play, work and travel, the technology created by Analog Devices is increasingly sought after. Tell us about ADI’s recent product expansion and some of your most exciting offerings.

A: Respecting the user of consumer products is very important: whether it’s capturing the best picture quality, or the sound of your voice or maintaining personal safety. Our microelectromechanical systems (MEMS) microphones have proven themselves in the most demanding use cases with industry leading SNR of 65dBA and extended frequency response from 100Hz to 20KHz. Another area of emerging importance, for which we introduced converter-based products to the market, is the ability to sense the near presence of the human body, process that information to lower power to the radio transmitters, and make sure everything operates below safe limits. The power of the digital processing is ultimately limited by how much signal we can get into and out of the digital domain, which comes back to the performance of the analog signal processing and data converters. ADI continues to put a lot of engineering into advancing state of the art options for dynamic range, bandwidth and power efficiency.

Q: Mobile consumer electronics continue to converge, in terms of functionality and feature sets, bringing many challenges to the circuits required to power these applications. Describe some of the technology ADI has available to address these challenges.

A: Convergence is really happening in mobile devices offered to end users, and that forces critical design choices. Handset makers, for example, constantly struggle with the size and capacity of the batteries to power their devices, and digital camera makers face a battle between image quality and cost. Some things, however, cannot be compromised. These include the end users’ experience of the image quality of the camera, or how frequently the device needs to be charged. ADI’s power management units (PMUs) have proven themselves in terms of efficiency and contribution to final picture quality and are in some of the finest cameras on the market today. We expect to see that become relevant in other mobile products as well. As mobile products become more sophisticated, they may operate in many different modalities, with a variety of sensors and each with very different supply needs. The need for optimizing battery life demands extreme power efficiency in every mode—so adaptivity is becoming increasingly important.

Q: With MEMS now seen as a critical enabling technology, semiconductor players have increasingly entered into the MEMS field as a potential high-value/high-growth market opportunity. As a result, the MEMS supply chain is expanding rapidly. Describe the current state of affairs in the MEMS market and some of ADI’s continued efforts to further develop its MEMS capabilities.

A: ADI provides MEMs-based products into a range of markets, each with different needs. We’ve optimized our supply chain by utilizing the best wafer fab and assembly services available. For most markets, we’ve worked cooperatively with key suppliers to assure both product performance and quality levels are maintained to ADI’s standards. In some cases, we have added specialized suppliers. And in some markets, we have determined that developing specialized internal capabilities is the most appropriate strategy. Those internal capabilities range from wafer fabrication to packaging and test. This blended supply chain allows us to service the needs of all of our customers, regardless of market or requirement.

Q: How has ADI effectively established an efficient and integrated MEMS

See Analog Devices Inc. page 29
Q: Silicon Laboratories offers high-performance, analog-intensive, mixed-signal products for a variety of end markets. Tell us about some of your most recent product offerings and which product offering you’re the most excited about.

A: At Silicon Labs, we’re attracted to large established markets that have resisted innovation. We like to solve difficult mixed-signal problems for customers and bring something disruptive to market.

We recently launched our Precision32 family of mixed-signal MCUs. We’re one of many competitors in the crowded 32-bit MCU space, but we’re convinced we’ll be able to gain market share given our innovative approach. We are using a standard ARM Cortex-M3 core and wrapping high-performance mixed-signal peripherals around it, and then layering on very easy-to-use prototyping and development tools that take some of the complexity out of embedded design.

Another good example is our latest generation of sub-GHz wireless radios. Radio frequency (RF) in CMOS has always been a core capability for Silicon Labs, and these radios leverage our ability to integrate highly sensitive RF circuits in a standard process technology to deliver cost-effective, high-performance radios. In this case, the radios are optimized for short-range applications like smart meters, remote controls and remote keyless entry (RKE). When combined with our very low-power MCUs, they form a complete system solution.

I’m also excited about recent innovations in our timing portfolio of clocks and oscillators, our digital isolators that replace optocouplers and our latest generation of silicon tuners displacing discrete, module-based tuners in iDTVs.

Q: Silicon Labs serves a broad set of markets and applications including consumer, communications, computing, industrial and automotive. Which end market do you believe provides the greatest opportunity for Silicon Laboratories and how are you addressing that opportunity?

A: That’s a good question. Silicon Labs is a very diversified company for its size, and that is by design. We have leveraged our core mixed-signal intellectual property (IP) to address problems across a broad set of applications and our revenue today is split relatively evenly between communications, consumer and industrial/automotive.

We’re focused on creating sustainable businesses with long life cycles. That focus naturally attracts us to the industrial, automotive and communications markets. However, we have found that in cases where differentiation creates very high barriers to entry and the long-term integration path favors mixed-signal IC companies, the consumer market presents some interesting opportunities as well.

We’re currently focusing considerable R&D investment on building out our portfolio to offer complete system solutions for the end points in connected devices in the home and factory. We’ve also built out a complete timing portfolio allowing us to be a one-stop shop for our telecommunications customers.

Q: This year’s International Consumer Electronics Show (CES) in Las Vegas, Nevada was the largest in history, with over 3,100 exhibitors and over 153,000 attendees—further showcasing the insatiable demand consumers have for the latest and greatest in electronics. What devices will drive growth in consumer electronics and semiconductors in 2012?

A: All the buzz at CES this year seemed to be around the Nest Labs thermostat, a very innovative smart thermostat with a clean user interface that can learn the home owner’s preferences and respond automatically without complicated programming. We are a supplier into the thermostat and are also big believers in the underlying trend that this type of device supports, the Internet of Things. Just as PCs were the first 100 million unit per year market and handsets were the first billion unit market, we believe the Internet of Things will be the first 10 billion unit per year market. The connectivity of devices in the home and factory through lower power, low-cost, smart electronics is finally being realized. The industry has more work to do in terms of standardizing the networking protocols to interface all of these devices together, but it is no longer a question of if this will happen, but when it will happen.

We expect the explosion of connected devices in the home will represent a terrific growth opportunity for mixed-signal IC companies, and we’re positioning ourselves to be at the center of those systems, offering the low-power processing, sensors and connectivity required.

Q: As consumer demand for universal connectivity, social networking and portable electronics for every facet of our lives continues to increase, the challenges facing semiconductor companies are also increasing. In my interview with Tyson Tuttle, president and chief executive office of Silicon Laboratories, we discussed the demand for mixed-signal devices; some of Silicon Labs recent and exciting product offerings; the future of consumer electronics; and much more.

— Jodi Shelton, President, GSA
The global semiconductor industry finished out 2011 on a weak note, as excess semiconductor inventories, which hit an 11-year high in the fourth quarter of 2011, dragged down average selling prices (ASPs) for components. This excess inventory, which was primarily the result of poor conditions in the macroeconomic environment and weak consumer demand, has represented a considerable challenge for the semiconductor industry, and correcting these levels has been a top priority for the world’s IC suppliers. This is due to the fact that inventory levels are a good gauge of near-term industry health. Increasing inventory demonstrates a confidence in the supply chain’s upcoming prospects, while a reduction demonstrates caution for possible difficulties in the short term, as suppliers expect demand to fall further.

Starting with the first quarter of 2012, stockpiles of semiconductor components began their decline, coinciding with the return of consumer demand across most regional markets. Specifically, in January 2012, U.S. consumer confidence reached its highest levels since July 2011, expanded yet again in February and held steady in March, which resulted in general growth for electronics during the first quarter. Meanwhile, China is expected to put a greater priority in shifting its economy to one that is less export dependent and generates more internal consumer demand. In order to generate this demand, China’s leaders have enacted new plans aimed at freeing up disposable income among more middle and low-income Chinese workers. On the other hand, consumer confidence in regions such as Europe and Japan remains diminished and will likely remain poor for the next few quarters in the wake of rising prices, particularly for necessities such as food and fuel.

As a whole, the second and third quarters will mark the stabilization of the global economic outlook, as the inventory correction concludes and foundry utilization rates return to normal levels. Semiconductor fab equipment spending is expected to stay level or even slightly increase later this year. This is important, as just a few months ago total spending for this year was expected to decline, and then top spenders like Samsung and Intel boosted their cap spending for the entire year. In fact, eight major companies, including Samsung and Intel, will keep their fab equipment spending level above $2 billion in 2012. This is a good indication that the suppliers are expecting some modest growth for the industry as a whole later on this year.

Leading the Recovery

Consumer

In terms of specific consumer devices, smartphones and PCs, including both notebooks and tablets, will be the products that have the greatest impact on total global IC demand and the correction of the inventory situation in 2012. Notably, demand for traditional PC categories, including both desktop and laptops, has been uneven over the first several months of 2012, with demand coming from some markets, including China, and weakness coming from other regions, such as the U.S. The general lack of demand was exacerbated by shortages of components used in hard disk drives, which first began in the third quarter of 2011 after flooding in Thailand. However, the hard drive shortage situation bottomed out in the first quarter of 2012, as storage manufacturers were busy boosting their production in areas outside of Thailand during the last quarter of 2011 and the first quarter of 2012. This increase in production is set to help improve storage pricing and make these components more affordable in the near term; however the additional production may also result in a hard drive oversupply situation in the second half of this year.

Automotive

Automotive semiconductors are also still in recovery from the supply chain and earthquake effects from the March 2011 disaster in Japan, although many suppliers have permanently adjusted to new conditions in the wake of the disaster. Specifically, the disruptions from both the earthquake and the floods have prompted many auto manufacturers to reconsider their supplier selection process for parts in their vehicles. Typically, auto parts are supplied from a single source in order to help mitigate costs. However, it is expected that such inventory risks could be lowered if manufacturers were spread out over several regions, so in the event of a disaster, other facilities could make up for lost production capability. Automotive semiconductors are projected to grow with an eight percent compound annual growth rate (CAGR) over the next five years. In terms of worldwide automotive semiconductor sales, analog products represent the single largest category, with 29 percent of the total market. Microcontrollers are the second largest segment, with 23 percent market share, followed by memory and logic.
Personal Computer (PC)
The weakness in the traditional PC market will be offset by the booming popularity of new smartphones, multimedia tablets and the latest category of "Ultrabooks", thin and light laptops with powerful capabilities and a premium price tag. More than 75 new Ultrabooks are expected to be launched over the course of 2012, most of which will enter into the market during the third quarter in order to take advantage of Microsoft's upcoming Windows 8 operating system, which is set to be released in October 2012. Although sales in this new segment have failed to live up to industry expectations so far, it is expected that consumer interest will improve significantly as the year continues, thanks to lower prices, a more developed product ecosystem, a greater advertising presence -- which will lead to greater product awareness and the return of demand spurred on by the PC refresh cycle and the release of Windows 8.

If successful in capturing market share, Ultrabooks will provide a major boost to top semiconductor suppliers. This is due to the fact that these high-end devices require premium components such as powerful microprocessors, highly dense NAND Flash memory and a considerable amount of DRAM, as well as radio frequency (RF) and power management. Intel, the world's leading semiconductor manufacturer by sales, has perhaps the most at stake in this market, as the majority of these "second generation" Ultrabooks will feature Intel's new "Ivy Bridge" mobile processor, first unveiled at the International Consumer Electronics Show in January 2012. Meanwhile, NAND Flash memory will remain one of the fastest-growing device types in 2012, thanks to a strong increase in the number of solid-state drives used in both tablets and Ultrabooks.

However, it is the DRAM market that is poised to see the greatest turn around in the second half of 2012. The DRAM market had a disastrous 2011, but is seeing the beginnings of pricing increases, which will lead to greater investments. This was aided in part by the recent bankruptcy filing of Japan's Elpida in the second quarter of 2012. South Korea's Samsung and SK Hynix, two of the leaders of the DRAM market, with 2012 market shares of 44 percent and 24 percent, respectively, are poised to benefit the most from the downfall of Elpida. Samsung, in particular, managed a record company wide profit of $5.1 billion in Q1 2012. Shortly after, the company announced that it would further increase its total investments by 25 percent this year, including $17 billion in semiconductor spending, which includes additional DRAM capacity. The company is also set to put a greater emphasis on its mobile application processors, as top clients appear to prefer their superior pricing, quality and output commitment. SK Hynix will also increase its investments this year. The company announced in Q2 2012 that it would boost its corporate spending by 20 percent more than it previously expected, reaching an investment target of almost $4.4 billion for 2012.

Industrial
In the industrial segment, the process controls end market will continue its slow implementation of advanced electronics technologies into manufacturing and commercial segments. Examples of these product opportunities include security systems, RF identification systems (RFID), real-time monitoring and operator interface applications. This market is the largest in the industrial electronics segment, accounting for an estimated 36 percent of the market. The largest opportunities for growth within process control are in smart heating, ventilation, and air conditioning (HVAC) control systems and RFID tags. Obviously, the ASP levels are higher in HVAC and it is forecasted to grow with an eight percent CAGR specifically. Many products at the Consumer Electronics Show (CES) for 2012 were directed at this application area, such as the smart platform by Allure Energy or the Nest home management system. These systems integrate smartphone controls and rely on precise energy management to support green initiatives. RFID is also a key growth market within industrial because of the third generation of RFID tags, which allow wireless network sensors to function as readers and more accurately track real-time location and more. The combined market of RFID tags and readers is expected to reach $1.13 billion worldwide by the end of 2012.

Medical
In regards to semiconductors in the medical space, there is a shift in concentration to portable electronics. Many of these items, such as the brand new WiThings Blood Pressure Monitor, are meant to improve monitoring while patients are separated from physicians. The WiThings monitor is on the leading edge of a growing group of medical devices that will be aimed at keeping a large amount of real-time statistics for physicians to analyze. A majority of these innovations are being integrated into cell phone applications to improve accessibility. Still, there are many challenges in the medical market, and despite its high growth rates, this industry has been affected by macro factors that have also influenced the consumer and computing markets. Namely, generally weak demand and slowing shipments have led to excesses in IC inventory supply and caused manufacturers to slash their capacity in order to salvage their margins. This factor is mainly why year-over-year growth in the medical segment is weaker than usual, at zero percent
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The features integrated in mobile consumer devices continue to increase at a rate that far outpaces the development in battery technology and power delivery. Therefore, the power conversion methodology and architecture must evolve in such a way to keep the battery life of mobile devices at a reasonable level.

Application processors are increasingly becoming more complex, and system engineers are striving to optimize architectures to ensure the user experience is not damaged by power running out during user interaction. It is unacceptable for the device to power-down due to low battery levels during game play; for it to get too hot during charging; for it to freeze during multi-tasking; or simply for it to be unable to perform basic tasks due to internal power dissipation issues. This article explores some of the potential methods of improving battery lifetime with PMICs in order to improve the user experience.

PMIC Overview
The system power circuits of a portable consumer device have to manage several key actions:

- Provide the correct voltage rails and sequence to the application processor in order to wake it up
- Provide enough power rails/channels to ensure an optimal solution in terms of cost and size
- Provide power to keep the real-time clock (RTC) or areas of the application processor awake to enable user continuity, even after the device has been switched off
- Auxiliary components to facilitate ease of device design, such as general-purpose input outputs (GPIOs) and analog to digital converters (ADCs)
- Safe charging and discharging of the battery, whether there are just one, several in series or several in parallel

Due to all of the above it is necessary for the PMIC to be the last component that consumes power, and thus directly responsible for the standby time of the device. As such, it must be highly efficient at low loads, or under low usage case scenarios. However, it is also responsible for converting battery energy to power the application processor during extreme or high-use case scenarios, thereby needing to be highly efficient at high loads, or output powers. Both conditions are investigated below.

The Effect of Efficiency on Battery Life under Heavy Use Cases
Consider an arbitrary high-use case scenario, which could involve listening to music while playing an on-line game. In this case, the direct current to direct current (DC-DC) requirements could resemble the following:

- DC-DC1 $V_{out}=1.2V$, $I_{out}=2.0A$
- DC-DC2 $V_{out}=1.5V$, $I_{out}=0.5A$
- DC-DC3 $V_{out}=1.8V$, $I_{out}=0.75A$
- DC-DC4 $V_{out}=2.5V$, $I_{out}=0.5A$

Previous generations of PMIC devices have not necessarily provided good efficiency DC-DCs, primarily because it is more
difficult to achieve a comparable performance in an integrated solution compared to a discrete solution. In the past, this would have been acceptable, but this is no longer the case as consumer user experiences become more demanding. Taking the conditions above and comparing different efficiencies, it becomes immediately apparent that integrated PMICs now have to offer high efficiency converters. For instance, if the power system just consisted of the four DC-DCs above, then every increase of one percent of efficiency results in a 1.3 percent increase in battery life. If all four DC-DCs operated at 95 percent, rather than say 75 percent, that would equate to almost an extra hour of heavy use time for a typical tablet with a 7.5Ahr battery (note: in some high-end tablet computers, the battery size can be up to 11.5Ahr and a 20 percent increase in efficiency in these systems would equate to an extra hour and a half of use time).

However, the DC-DCs are just one part of the power solution. Due to the complexity of the systems, multiple power rails are required, some of which, are supported with low-dropouts (LDOs). Again, considering an arbitrary high-use case scenario, the requirements on the LDOs could resemble the following:

- LDO1 Vout=1.2V, Iout=0.2A
- LDO2 Vout=1.2V, Iout=0.2A
- LDO3 Vout=1.5V, Iout=0.2A
- LDO4 Vout=1.5V, Iout=0.2A
- LDO5 Vout=1.8V, Iout=0.2A
- LDO6 Vout=1.8V, Iout=0.2A
- LDO7 Vout=2.5V, Iout=0.2A
- LDO8 Vout=2.5V, Iout=0.2A
- LDO9 Vout=3.0V, Iout=0.2A
- LDO10 Vout=3.0V, Iout=0.2A

As detailed in Power Management Trends in Portable Consumer Applications\(^1\) the efficiency of the LDO is inversely proportional to the difference between the input and output voltage of the LDO. The smaller the difference, the more efficient the LDO. In an ideal situation, each of the LDOs with a larger input output voltage difference would have a DC-DC pre-regulator to improve the efficiency. However, this adds cost and complexity to the system and typically one DC-DC may be available to pre-regulate the LDOs. In this case, care should be taken to determine which of the LDOs should be pre-regulated, and at what level. Figure 1 shows the battery lifetime improvement (just considering the LDOs) for different levels of pre-regulation, assuming a DC-DC pre-regulation efficiency of 85 percent.

Figure 1. Potential Battery Life Savings with DC-DC Pre-Regulation.

<table>
<thead>
<tr>
<th></th>
<th>DC-DC Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery Size</td>
<td>75%</td>
</tr>
<tr>
<td>No Pre-Regulation</td>
<td>-</td>
</tr>
<tr>
<td>7500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>11500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>All LDOs Pre-Regulated</td>
<td>-</td>
</tr>
<tr>
<td>7500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>11500mAhr</td>
<td>-11.2</td>
</tr>
<tr>
<td>LDOs with Outputs 2.5V or Less Pre-Regulated</td>
<td>-</td>
</tr>
<tr>
<td>7500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>11500mAhr</td>
<td>2.4</td>
</tr>
<tr>
<td>LDOs with Outputs 1.8V or Less Pre-Regulated</td>
<td>-</td>
</tr>
<tr>
<td>7500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>11500mAhr</td>
<td>15.7</td>
</tr>
<tr>
<td>LDOs with Outputs 1.5V or Less Pre-Regulated</td>
<td>-</td>
</tr>
<tr>
<td>7500mAhr</td>
<td>-</td>
</tr>
<tr>
<td>11500mAhr</td>
<td>14.3</td>
</tr>
</tbody>
</table>

As can be seen in Figure 1, care must be taken in determining the best and most efficient pre-regulation scheme. In the worst case, it could even result in a less efficient solution.

In the two examples above, the LDOs and DC-DCs have been considered in isolation. So, for a complete system, both the power dissipation of the DC-DCs and LDOs must be considered to give a valid comparison for the lifetime of the battery in a high-use case situation. Figure 2 shows the overall lifetime increase in battery lifetime for various configurations, where in the ideal case of having all the DC-DCs operating at an efficiency level of 95 percent and pre-regulating all the LDOs at 1.8V and below, gives a battery lifetime improvement of 31.2 percent, or an increase in battery lifetime of up to 52 minutes.

Figure 2. Increase in Battery Lifetime (in Percent and Minutes) for Various DC-DC and LDO Pre-Regulation Configurations.

The Effect of Quiescent Current on Battery Life under Light Load Conditions

Under light loads, a major contribution to battery life is the quiescent current. A low quiescent current is key to maintaining the battery level while the device is switched off or in standby mode. If the quiescent current is too high, then the battery charge will reduce while the power is turned off, and therefore the device will not turn back on, causing a poor experience for the user.

The next generation of PMICs need to have multiple modes of operation in order to minimize the quiescent currents and ultimately maximize battery life. A breakdown of a typical PMIC’s quiescent current is shown in Figure 3. This particular PMIC has multiple modes of operation for each power channel to optimize the battery life during different scenarios. In Figure 3, it can be seen that the DC-DCs have four modes of operation: auto mode (Mode 1), hysteretic mode (Mode 2), LDO mode (Mode 3) and off mode (Mode 4). The standard LDOs also have four modes of operation which are: normal mode (Mode 1), two low power modes (Mode 2 and 3) and off mode (Mode 4), while the low noise LDOs have three modes of operation: normal mode (Mode 1), low power mode (Mode 2) and off mode (Mode 3).
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Environmental issues have become a global focus where alternative energy solutions are converging as fast growing drivers for many user generations to come. One of the key challenges of alternative energy is how to optimize the storage system in order to convert the alternative energy to efficient and secure uses for the long term. The solution is to enhance the battery storage/management systems, which are primarily driven by the ICs controlling and managing these battery systems for various applications.

Energy Pass Inc. (EPI) is dedicated to fabless product design of Li-battery power management ICs for various application markets including the mobile, motion, solar and medical markets. The product features optimize the discharging efficiency, as well as the charging efficiency, out of the battery and energy storage system, throughout precise measurement, smart control and calculation of battery stored charge (state-of-charge (SOC)) and optimal management of battery state-of-health (SOH). SOC and SOH are accomplished by EPI’s smart battery power management system composed of microchips to carry out the cell-to-cell charging, balancing and smart integration of discharging and charging functions. Additionally, the products are supported by the high specification of battery protection for over-charge, over-discharge and over-temperature to maintain long battery life.

“I have been very pleased with GSA’s communication forums and efforts to provide updated semiconductor supply chain knowledge to its member companies. In keeping member companies informed of industry trends and activities, GSA is consistently focused on adding value for its member companies.”

– Dr. Robert Tsu, President and CEO, EPI

Robert Tsu, President and CEO
Kevin Lin, Vice President and CTO
Jason Kao, Senior Director, Sales and Marketing
Eric Luo, Senior Director, R&D

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Nigel R. Farrar, Vice President, Lithography Applications Development, Cymer Inc.
Tommy Oga, Director, Strategic Marketing, Cymer Inc.

Advances in semiconductor technology have driven the explosive growth of new mobile applications. And, mobile computing and wireless communications have become the leading drivers for semiconductor chip demand. Scaling and technology innovation have combined to deliver the small size and form factor, wireless connectivity and low power consumption that have resulted in low-cost products that have expanded the consumer market for these devices. Many consumers are now buying multiple computing platforms, such as smartphones, tablets and laptops, driving the need for them to communicate with each other and provide seamless access to personal or Web content on any of them. Future demand for increasing levels of connectivity, with increasing support of file sharing and video content, drives not only the market for new portable devices, but also the computing and storage infrastructure needed to support these technologies.

In particular, demand for smartphone chips has grown from a new application only seven years ago, to what will be the largest segment of semiconductor chip demand by 2014. The ability of designers to add more and more features to new devices leads to continued upgrading of these devices in developed countries, and rapid adoption in developing countries. One key factor in achieving this growth has been the rapid reduction in chip cost per function, driven by the scaling of chip size and transistor dimensions. Over the last 50 years, the cost per megabyte of DRAM has decreased by about 10 orders of magnitude. Similar performance scaling has been seen in the number of transistors per logic chip, and is leading to an explosive growth in the total number of transistors produced by the semiconductor industry each year. The additional functionality provided by all of these devices is in strong demand and can be used by designers as fast as it can be provided. Although smaller transistors enable more functionality per chip, performance improvements have also required innovations in new materials and device architectures. The challenge of minimizing transistor current leakage has been particularly important, as low-power consumption is crucial for mobile applications. Consumers now want devices that are always on and always connected, making long battery life essential, and a key factor in new chip designs. These new transistor architectures also provide a significant reduction in power consumption for the increasingly large server farms needed to support the expansion of mobile computing.

Challenges in Lithography

The key technology driver of Moore’s Law, which forecasts that the number of transistors on a chip doubles every 18 months, has been advanced lithography. The value provided by advanced lithography equipment in improving resolution and productivity has more than offset the rapidly increasing equipment cost. Resolution has been extended by a combination of reduced exposure wavelength and increased lens numerical aperture (NA), as described by Rayleigh’s resolution equation, R = k /NA, where R is the minimum half-pitch that can be resolved, l is exposure wavelength and k, is a proportionality factor that is determined by process conditions such as photoresist characteristics, illumination scheme and photomask design, and is desired to be as large as possible. To improve resolution, lens NA was typically increased to close to its theoretical maximum value of 1 before a smaller wavelength was required. However, wavelength changes are a major disruption since they require new light sources, new optical materials and new process materials.

A significant shift occurred in 1996 when excimer laser light sources started to be used in chip production, replacing the previous mercury arc lamp sources. Excimer laser technology for lithography applications had been under development for 10 years when the industry was able to successfully ramp KrF (248nm) lithography into production. Today, these sources can cost less to operate than the older mercury arc lamps and have exceptionally high reliability, with about 99.8 percent uptime. This success led to the move to ArF (193nm) lithography starting in 1999 and reaching widespread use by 2003.

But the materials challenges at the next proposed wavelength shift (to 157nm) proved more challenging than an alternative approach which broke the NA=1 barrier. This was the use of immersion lithography, where a film of water between the lens and the wafer allowed NA to be increased above 1. Today, NA has reached 1.35, though limited again by the lack of suitable new optical materials and immersion fluids to enable even higher NA. However, despite these continuous improvements in the scaling of NA and wavelength, lithography resolution capability would have fallen well behind the demands of Moore’s Law without the introduction of various resolution enhancement techniques to reduce k, . This has recently culminated in the use of double patterning, where some process layers require two interleaved exposures to achieve the desired resolution. In some cases, additional exposures or further pitch division are required, and these processes significantly increase the design complexity, process control challenges and the process cost. Design restrictions are particularly undesirable as they can lead to limitations to density scaling, hindering the goal of improving lithography resolution.
Extreme Ultra-Violet Lithography (EUVL) as a Likely Solution

The most likely solution to maintain Moore's Law scaling, and reduce the escalating cost of these complex lithography solutions is EUVL. EUVL operates with an order of magnitude reduction in wavelength, at 13.5nm. Such a short wavelength poses challenges, such as the need for tools to operate in vacuum and the use of all-reflective mirrors, instead of lenses, made of precision multi-layers of silicon and molybdenum. The use of these mirrors and their relatively low-reflectivity (about 70 percent), drives increased demand for source power. However, since the EUV wavelength offers the advantage of much higher resolution, without complex processing techniques, the industry has been eagerly awaiting delivery of pre-production tools for process development. Over the last few years, there have been significant developments in EUV technology, not only in the exposure tools and sources, but also in photoresist materials and the additional infrastructure needed for high-volume manufacturing. Today, the industry has started to introduce this next major wavelength shift into process development fabs. And, although the exposure system and light source are increasingly complex, the benefits of increased capability and further extendibility are expected to justify the investment in this technology.

Keys to Acceptance: Competitive Productivity

The key for EUVL to gain widespread acceptance in the industry is competitive productivity. After excimer laser light sources were introduced into production over 15 years ago to reduce wavelength and improve resolution and continued scaling of source power; this combined with enhanced exposure tool stage performance delivered increased productivity, the other key enabler for node-to-node chip cost reduction. Over the last 15 years, lithography productivity has improved by a factor of five. And an important factor in ensuring the successful introduction of EUV lithography is developing a powerful light source to enable the level of throughput that meets the industry's productivity requirements for cost-effective production.

Lithography performance across multiple technologies can be compared by using a metric that combines its key benefits of resolution and productivity, relative to the cost to achieve the increased performance. Here, this metric is defined as TP/(CD×C), where TP is throughput, CD is resolution and C is tool cost, and is shown in Figure 1, as a function of time, for various lithography technologies from KrF to EUV.

Increasing Value

It is clear that the value of this metric must increase over time in order for the technology to provide a benefit relative to its cost. Historically, it can be seen that such a metric indicates that lithography increases its value at a rate of about 28 percent per year; whether this increase has been provided by improvements to an existing technology, through increased NA, reduced k, and higher throughput or through a shift to a new technology with shorter wavelength. It is also evident, for all technologies, that the value of early tools initially falls below requirements, but increases over time after their introduction to reach a maturity level that follows a consistent trend. It can be seen that both KrF and dry ArF tools improved slightly beyond the historical trend, and maintained that performance for several generations. However, ArF immersion tools barely reached the trend line and would not have kept pace with the value trend, despite continued improvements over time. This shortfall was compensated by the use of resolution enhancement techniques and double patterning, but at added process cost.

The attraction of EUV is that it offers the possibility of returning to, and exceeding, the value trend line as the technology matures. As expected, the first generations of tools will fall short of this value trend, but are expected to eventually exceed requirements. By comparison, an alternative next-generation lithography (NGL) technique, multiple e-beam direct write lithography (MEBDW), by the same metric, starts much further below the trend line and would fail to improve to meet the industry value requirement. Despite the intrinsic resolution capability of MEBDW, and an aggressive roadmap, these tools never achieve the throughput necessary to become competitive for high volume applications.

Achievement of Throughput Targets

However, EUVL also needs to achieve its throughput targets to deliver the expected value. The key to meeting these requirements is the light source. For the first time in 20 years, a radically new light source is required. The EUV light for these systems will be provided by a laser-produced plasma (LPP) source. This approach uses a high-power pulsed CO₂ drive laser, which is focused to ionize and heat small droplets of molten tin to a very high temperature so that they emit 13.5nm wavelength light. The laser pulses must be perfectly synchronized at a high repetition rate with the position of the stream of moving tin droplets so that every droplet is hit, and the source operates at high efficiency. Significant new mirror technology has also been developed to collect the light and direct it precisely to the entrance to the exposure tool illuminator system. Additional techniques for maintaining high reflectivity of the mirror in the presence of contaminants, such as residue from the tin target itself, are required to ensure that source uptime is high and does not detract from the required productivity. Such sources have been under development for some time and all technologies are now fully integrated and installed at multiple fabs for pilot development. Figure 2 shows a photo of a state-of-the art LPP EUV source.
Roughly one year ago, the GSA formed “The Capital Lite Working Group” to “develop, promote and execute expanded investment models that can be used by semiconductor start-ups to innovate and prosper.” The GSA also published the paper, “The Capital-Lite Semiconductor Model: Revitalizing Startup Investment”, which provides a model for enabling startup semiconductor companies to source intellectual property (IP) and capital from more sizable semiconductor companies.

It’s no secret that the semiconductor investment model is stressed. “Capital-Lite” is simply an imperative because investors have little appetite for the massive investment and extended time required to reach cash flow breakeven. The GSA model appears to be directed at start-ups that are developing large systems-on-chip (SOCs) that require large development efforts and costly “commodity” IP that adds little differentiation.

There is another “Capital-Lite” that appears to be successfully emerging in the industry. In this model, companies develop ICs that are tiny, thus eliminating the need for large development teams, and leverage trailing edge processes. In this model, the IC is the core IP, with little, if any, “commodity” IP overhead. By definition, the IC is usually a small mixed-signal device with low average selling prices (ASPs) targeted at high-volume markets.

One example of this model is eoSemi, a fabless semiconductor company focused on developing patent-pending, all-silicon replacements for quartz crystal timing references. The company was founded in 2005 with initial funding by the founders using profits from IC design consultancy services. In June 2010, the company closed a $4.9 million Series A round from NESTA Investments, Capital-E, Enterprise Ventures (“EV”) via its RisingStars Growth Fund II and South Yorkshire Investment Fund. eoSemi does plan to seek additional capital towards the end of the 2012; however, the existing investors are already committed and the investment-lite, lean organization business model is unlikely to change. The company has just 12 employees.

Quartz crystals are expensive, consume too much space and power, require too many external components and have limitations in mechanical shock resistance. eoSemi’s ATOC™ (Accurate Timing Oscillator Circuit) technology uses standard CMOS processes and brings together a number of innovations in oscillator design to replace crystals. The company plans to become a provider of miniature, silicon-only references and derivative products for a wide variety of applications. Because its devices can be made using standard CMOS, eoSemi’s products are cheaper, smaller, easier to integrate, more robust and consume less power than competing offerings.

eoSemi’s immediate focus is on handheld battery powered devices, such as mobile phones, smartphones and tablets, worth $800 million in 2011. eoSemi argues that other silicon- and microelectromechanical systems (MEMS)-based competitors don’t offer viable solutions, which is why cellphones still contain crystals. Compared to other silicon and MEMS-based timing devices, eoSemi argues that its technology uniquely combines the benefits of standard CMOS, better accuracy, lower power, smaller size, higher integration and lower cost.

The first product to be based on ATOC technology is a 32kHz timing reference circuit aimed at the mobile market and designed to directly replace crystals. Manufactured using standard CMOS, the new device draws just 8µA of supply current in active mode and delivers accuracy down to ±30ppm. eoSemi’s products are inherently temperature and stress compensated, so accuracy over temperature is much improved. This combination of specifications, along with an operating temperature range of -40°C to +85°C, means that the timing reference will comply with the system design requirements of major 3G handset manufacturers.

The 32kHz product occupies around 2mm² of board space, far less than the equivalent crystal, which will occupy roughly 70mm² once it’s laid out on a board in its exclusion zone. The products are manufactured using TSMC’s 180nm 4-layer metal CMOS process with no extra steps, allowing future integration. The same technology will also scale to other frequencies.

eoSemi has already delivered engineering samples for the first 32kHz product to key customers. Commercial production, in a 1.5mm² chip-scale package, will commence in Q3 2012. In classic “Capital-Lite” fashion, eoSemi is partnering with leading silicon companies and granting “right to manufacture” licenses, to penetrate the mobile handset segment, thus giving major customers access to eoSemi’s products through established and trusted supply channels.

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The consumer electronics market offers the largest market opportunity today for semiconductor companies, which, under a broad definition includes mobile phones, tablets and traditional consumer electronics. However, the market creates many challenges for semiconductor suppliers, including:

- Low margins, fierce price competition and new entrants (China)
- The risk of aligning with a standard, which does not achieve market acceptance
- Volatile consumer market cycles

Low Margins, Fierce Price Competition and New Entrants (China)

Consumer electronics are generally aimed at large end user markets. Although there are some niche products with relatively small market sizes, most major consumer electronics are targeted toward adoption by the majority of households in advanced economies, and many upper income households in developing economies. Key examples are mobile phones, liquid crystal display (LCD) televisions, DVD players/recorders, digital video recorders (DVR), notebook personal computers (PC), tablet PCs, digital audio players, digital cameras and digital camcorders.

Large markets draw many competitors. The more competitors, the more fierce the competition. Competition takes many forms – innovation, features, design, marketing – but price is always a key competitive factor in these markets.

Figure 1 shows the largest consumer electronics companies. The list excludes companies that primarily sell PCs (such as Hewlett-Packard, Dell and Lenovo), since much of their sales are to businesses. Total revenue, consumer electronics revenue and operating margin and rank in some key categories are shown.

Apple is the number one consumer electronics company, including its PCs, mobile phones and tablets, and enjoys high operating margins due to its proprietary operating systems, and success in products such as the iPad and iPhone. Samsung is second, with strong market share in several categories including LCD TVs and mobile phones. Samsung's economy of scale allows it somewhat higher operating margins (five percent to eight percent) than most other consumer electronics companies. The companies below Samsung generally have low margins of less than five percent. An exception is Microsoft, whose consumer electronics business is primarily its Xbox game systems.

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**Figure 1: Top Worldwide Consumer Electronics Companies**

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<thead>
<tr>
<th>Total Company</th>
<th>Consumer Electronics</th>
<th>Worldwide Rank</th>
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<tr>
<td><strong>Company</strong></td>
<td><strong>Base Revenue</strong></td>
<td><strong>2010</strong></td>
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<td><strong>Billions of US$, Calendar Year</strong></td>
<td><strong>Revenue</strong></td>
<td><strong>Revenue</strong></td>
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<tr>
<td>Apple</td>
<td>US 76</td>
<td>128</td>
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<tr>
<td>Samsung</td>
<td>Korea 134</td>
<td>149</td>
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<tr>
<td>Panasonic</td>
<td>Japan 101</td>
<td>100</td>
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<tr>
<td>Nokia</td>
<td>Finland 56</td>
<td>54</td>
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<tr>
<td>LG Electronics</td>
<td>Korea 48</td>
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<tr>
<td>Sony</td>
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<td>Toshiba</td>
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<td>Sharp</td>
<td>Japan 35</td>
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<tr>
<td>Mitsubishi Elec.</td>
<td>Japan 42</td>
<td>45</td>
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<tr>
<td>Microsoft</td>
<td>US 67</td>
<td>72</td>
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Source: Company reports, Semiconductor Intelligence estimates
The low profit margins of most consumer electronics companies force them to be cost efficient in manufacturing. These companies tend to squeeze their suppliers (including semiconductor companies) on pricing with the potential reward of high volume.

The cost competitiveness of consumer electronics can be seen in LCD TVs. The Consumer Electronics Association (CEA) estimated the average price in the U.S. for an LCD TV has declined an average of 14 percent a year from 2005 to 2010. One factor in the price drop is learning-curve-based cost declines for LCD panels. However, competition is also a significant factor. Over the last five years, the typical LCD TV has increased in screen size, gone from 720p to 1080p resolution, added light-emitting diode (LED) backlights and added Wi-Fi connectivity.

Competitiveness in the consumer electronics industry is increasing with the emergence of China-based companies. The CEA listed seven Chinese companies among the 2011 top 50 consumer electronics brands. The exact number of Chinese companies which exhibited at the January 2012 International Consumer Electronics Show is difficult to come by. However counting the exhibitors with major Chinese cities in their name results in almost 400 companies, about 15 percent of total exhibitors. There were 244 companies with Shenzhen in their name. Haier, a Chinese company with a broad range of consumer electronics products, had an exhibit rivaling the size of those by top consumer electronics companies.

**Risk of Aligning with a Standard, that does not Achieve Market Acceptance**

Standards are important to the growth of the electronics industry. New product categories usually have many companies competing with different technologies. Most consumers are reluctant to adopt a new product until standards are set to ensure a product does not become obsolete. Standards can be set by the marketplace, by government agencies or by industry standards bodies. A key example is the PC in the late 1970s and early 1980s. Several companies were making a variety of PCs, all with different operating systems, and software generally had to be custom developed for each type of PC. As a result, most businesses and consumers were reluctant to buy PCs. IBM introduced its PC in 1981 with a Microsoft operating system and Intel microprocessor, and created an open standard, through which other companies could build IBM compatible PCs. The strength of IBM’s position as a dominant overall computer company coupled with early market acceptance, led to the creation of a standard that is still used in the vast majority of PCs 30 years later (with numerous hardware and software upgrades through the years).

A major risk to consumer electronics companies is aligning with a standard that does not become mainstream in the marketplace. Early video cassette recorders (VCR) came in two standards: Video Home System (VHS) and Betamax. Each required different types of tapes. Prerecorded tapes were often released in both standards. Sony made Betamax VCRs while VHS VCRs were made by several companies licensed by JVC. By the mid 1980s, VHS came to dominate VCRs, largely due to its multiple suppliers. A similar situation occurred in the 2000s with the introduction of high-definition DVD players. Sony was producing Blu-ray DVD, while Toshiba was producing HD DVD. Sony learned its lesson from the Betamax debacle and took on several partners in Blu-ray. Sony had also acquired Columbia Pictures in 1989, which gave it a major movie studio in the Blu-ray camp. Blu-ray won out in 2008 when Toshiba announced it was withdrawing from HD DVDs.

A new standards battle is currently emerging in operating systems (OS) for smartphones. Smartphones are growing at a rapid rate and are the growth drivers of the overall mobile phone market, and several operating systems have, and continue to emerge. The charts below show Gartner’s estimate of OS market share in 2011 and the top mobile phone suppliers and operating systems they support.

Gartner estimated Android (developed by Google) had the largest share in 2011 at over 40 percent, with most of the major mobile phone suppliers providing Android phones. LG Electronics and Motorola only supply Android phones; and with the merger of Google and Motorola Mobility, Motorola should solidly remain in the Android camp.

iOS (Apple’s iPhone OS) and Symbian (by Nokia) had the next largest shares, at just under 20 percent. Apple has been successful with the iOS and has a vast number of application (or app) developers. Nokia has been deemphasizing its Symbian operating system to focus on the Microsoft OS.

Research in Motion (RIM) was fourth with its OS for BlackBerry devices. BlackBerry has been popular with corporations, as it functions well with corporate email systems, but has had limited success with consumers.

Microsoft had a relatively small OS share of around two percent; however, with Microsoft’s resources and a huge base of Windows PC users, it is expected to gain share, though it remains to be seen if it will be a serious competitor with Android and iOS. As mentioned earlier, Nokia, the largest mobile phone maker, agreed to support Microsoft’s Windows Phone for its main smartphone OS. Several other major mobile phone companies are hedging their bets by supporting both Android and Microsoft.

Bada also had about two percent share. Bada is an OS from Samsung designed for low-cost smartphones. Thus, Samsung is supporting three operating systems: Android, Microsoft and Bada.

The battle over smartphone operating systems is important, because much of the popularity of smartphones is due to apps that can be downloaded for free, or for a small charge. Some major app developers...
In the fast-paced world of consumer electronics, getting a competitive product to market quickly is the goal. Margins matter. Quality matters. A product that bombs in the market due to poor performance or quality can kill a small company and wound even the largest.

Enhanced features, functionality and performance are driving the next generation of system-on-chip (SOC) designs that now contain not just one, but multiple processors enabling almost every possible form of communication and computation. Verifying that these devices work as intended is hellish, leaving semiconductor companies strategizing about how to ensure sufficient product quality without incurring cost overruns or slowing down time to market. After all, it's all about making a profit and having a hit.

Often, this challenging burden falls on verification engineers who must resort to manually developing tests for these big, complex chips, an insufficient approach for designs with multiple embedded processors. Fortunately, new, cost-effective approaches in SOC verification are emerging to automate this process and provide more thorough verification without impacting time to market.

Until lately, that hasn’t been the case. The verification segment within electronic design automation (EDA) has evolved without a real strategic focus on SOCs. As an industry, EDA has focused on block-level verification to reasonable success. Languages and methodologies have been developed for the block level that enable tests to be automatically created from a unified testbench description, but these don’t scale or adequately address the system level. When it comes to verifying multiple processors with different kinds of intellectual property (IP), methodologies used for block-level verification quickly break down.

The SOC verification problem is so daunting that it will only be solved through automation. This problem is not going away, or at least not until consumers tire of their electronic devices. A new system-level verification approach that turns the EDA industry’s tried-and-true, block-level approach upside down is the key. Instead of focusing on the stimulus, this approach favors devising a plan by the verification team with clearly defined goals, along with a valid way of achieving those goals.

An automated tool is the keystone of this strategic planning. It must be able to handle one or more processors within the SOC, as well as coordinate multiple concurrent activities. It should be capable of managing all integrated verification tasks as well. In sum, the tool should be constructed to find ways to meet verification goals and be able to provide examples of ways those goals could be achieved using different parts or paths through the system.

Embedded Processors in SOCs

The extensive use of multiple embedded processors in SOCs has created a complex challenge that includes thorough verification of the system and IP interconnect, shared system resources, use cases and system performance. For example, verification engineers must consider every possible way in which a cell phone can be used and figure the proper way to test these scenarios.

At the block level, constrained-random test generation is a leap ahead of traditional functional verification via directed testing. Industry standards SystemVerilog and the Universal Verification Methodology (UVM) and their accompanying tools have been integrated into the development flow and enable transactional tests to be created from a unified testbench description for IP block-level verification.

While many tout the benefits of these standards and consider the verification problem fixed, they are limited in their capabilities, especially when it comes to verifying SOCs. Functional verification has become the bottleneck for many of these designs, because engineers today verify independent IP and stitch them together in hopes that the SOC will work as intended. Testing an SOC containing embedded processors requires much more than that, starting with additional software tests typically written in C.

With a dearth of tools, SOC verification engineers are forced to design and manually write C tests individually. For the most part, these tests address the tip of the SOC verification iceberg, leaving behind system bugs that are not discovered until much later. Bugs discovered late in the development process, or when first silicon is sampled, delay time to market and affect revenue.

Removing functional verification as the bottleneck for technological innovation and SOC project schedules should be the EDA industry’s next initiative.
SOC verification is a complex task with a variety of objectives and challenges, but offers verification engineers the ability to establish that system-level capabilities, such as functionality, performance and power management, perform according to specification. Using a cell phone’s various uses as an example again, a verification engineer could uncover an overwhelming number of possible scenarios. At the heart of each cell phone is a complex SOC with use cases across multiple concurrent applications, along with shared resources and on-board power and clocking management systems.

Automation software can assess what to verify and develop test cases needed to adequately cover the wide spectrum of verification objectives. This is accomplished through automated self-verifying C test cases running on embedded processors. They exercise a wide range of functional scenarios to ensure that the SOC can support the necessary concurrency, system-level and software functionality while meeting performance requirements.

Today’s SOC often contains numerous IP blocks from a variety of different sources, including internal design teams, EDA vendors and third parties. While each individual IP block will have been verified on its own, it’s not certain that blocks will operate correctly when fully integrated within the SOC. They need to be tested for shared resources, interrupts and system management, along with application use cases and performance.

The new SOC verification approach includes software that automates the generation of self-verifying test cases for multi-threaded, multi-processor SOC devices. It determines what to test and then creates test cases to cover the wide spectrum of verification objectives. A verification engineer can use it to generate C test cases to target system interactions that are self-checking and optimized to run efficiently in simulation.

Scenario models are an integral part of the new approach, an intuitive way to describe SOC functionality, much as an engineer would draw a diagram of the chip operation. The automation software uses the scenario models to generate input stimulus, check results and measure coverage closure, creating transactional tests at the IP level and C tests at the system level. This approach integrates with all current solutions, including the UVM, the Open Verification Methodology (OVM), the Verification Methodology Manual (VMM), SystemVerilog, Verilog and commercial simulators.

This approach has the flexibility to work at all stages of the development flow and be applied to models at any level of abstraction. As a result, the verification task will be no longer relegated to the later stages of development activity as it has been in the past. Design teams with a virtual prototype created for software development can start verifying at the same time. Earlier in the flow means having the time necessary to accomplish thorough verification and the tools to ensure that system-level coverage goals can be met.

Bringing verification earlier in the development process allows tasks such as performance measurement to have a greater impact. Rather than finding problems late in the development cycle, the system can be optimized for the desired performance early in the project. Integration verification then becomes a design task and performing verification on abstract models enables a more efficient process with execution speeds often orders of magnitude faster than for register transfer level (RTL) verification.

**Conclusion**

Consumer demand for electronic devices with more features and capabilities increases with each new offering, which means that each system-level design is more complex than the last. Verification engineers play an integral role in an electronic product’s success since they are responsible for integration verification, performing system verification and validation. They need the right tools and methodology to be successful.

Semiconductor companies can arm their verification team with a new weapon to fight the SOC verification battle that will help them succeed in the consumer market and successfully battle low margins, fierce competition and aggressive pricing. All the while, making themselves the darlings of the consumer market. Indeed, many will view SOC verification as a key engine, driving the success of chips targeted for consumer electronic devices.

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**About the Author**

Adnan Hamid is co-founder and CEO of Breker Verification Systems. Prior to starting Breker in 2003, he worked at AMD as department manager of the System Logic Division. Previously, he served as a member of the consulting staff at AMD and Cadence Design Systems. Hamid graduated from Princeton University with Bachelor of Science degrees in electrical engineering and computer science and holds an MBA from the McCombs School of Business at The University of Texas.
ANSI-C programmable in the case of processors) 2.) Make the chip attractive and easy enough to use that the customer can effectively do the programming himself.

- **Hardware:** Quoting the slogan of the green movement, “Reduce, Reuse and Recycle”. The way to reduce hardware development costs is by reducing the feature set that needs to be implemented, maximizing the reuse of validated blocks and recycling all the great chip ideas of the last 70 years (no not-invented-here nonsense allowed). Reuse is one of the key competitive advantages in the chip industry. An SOC company that does not embrace reuse as a basic design imperative will not be profitable in the long run, because they will miss market windows and have R&D costs that are far too high.

- **Design Verification:** Reduced design complexity again comes to the rescue and the key here is to not be "too clever". The prevailing method of chip development usually involves an experienced system architect writing a set of specifications that are then given to a team to design and verify. Without close interaction from day one between the architects and the complete design team, this almost certainly causes expensive problems downstream. In the words of Richie Kernigan. “Debugging is twice as hard as writing the code in the first place. Therefore, if you write the code as cleverly as possible, you are, by definition, not smart enough to debug it.” Designing architectures that can easily be verified with a small team is an art form that requires very tight integration between the architecture, design and verification teams.

- **Back-End:** There is a rich ecosystem of support companies that can take over as much, or as little, of the chip business the client requests. Opportunities for outsourcing include: manufacturing (a must!), RTL design, synthesis, verification, package design, board design, testing and logistics. If your core competency is chip design and computer architecture, then outsourcing software, board design, sales, marketing and logistics makes sense. If your core competency is system architecture, outsourcing a large part of the chip design makes sense, but make sure you find the right implementation team.

- **Sales/Marketing:** Selling chips with power point presentations has never worked and really just wastes money and burns out the sales and marketing team. The bigger the claim of the chip, the smaller the chance that the customer will do anything before he gets his hands on a board level development system. If you have a low R&D burn rate, you can be less aggressive with the pre-product sales and marketing effort and subsequently waste less money.

## Conclusion

It is possible to spend $100 million (or even $1 billion) on chip development, but it’s also possible to spend as little as $2 million to reach profitability as a fabless semiconductor company.

## About the Author

Andreas is a world expert in computer design. His experience is unparalleled, having worked on digital signal processors, network processors, multimedia processors, and high-speed networking devices. His work has been featured in numerous publications, including The Journal of Electronic Design, Innovation and Entrepreneurship, where he has contributed articles on the future of computer design.

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Establishing compatible tester classes will have a significant impact on COT and cost-of-ownership (COO), while eliminating many technology and loading risks. This concept enables semiconductor devices to quickly and easily move from one tester class to another to optimize for lowest cost.

Benefits of a Scalable RF ATE Platform for Low-Cost Applications

A scalable platform has several advantages, especially for the low-end classes. First of all, the same high-performance RF, analog, (high-speed) digital and power supply hardware cards can be used, but the amount of resources needs to be tailored to the needs. Non-critical low-cost applications, like legacy 2G transceivers representing roughly 50 percent of the overall transceiver volume, have typically much shorter and simpler test lists. In some cases, the index time of the handlers is limiting the throughput. In this case, it is more cost effective to scale down hardware resources and infrastructure to a minimum to achieve the best COT. However, test quality must be maintained. Inaccurate error vector magnitude (EVM) results will lead to yield loss, as well as obsolete voltage and current measurement units. A scalable platform ensures that unexpected test requirements in the low-end have already been solved in the high-end and therefore can be easily leveraged.

The same is true for advanced test techniques. Conventional low-cost ATE for example does not provide mandatory throughput and efficiency features like hidden capture data upload, hidden/multithreaded calculation and protocol-aware or concurrent test. These benefits can be simply inherited if part of a scalable ATE platform approach. The software is also more powerful. Low-end configurations can leverage the same demodulation library, the same test method library and debug tools. This dramatically improves TTM by reducing training efforts and test program development time. Overall, low-end configurations as part of a scalable RF ATE platform provide best-in-class throughput and usability.

Cost Reduction through Scalability, Compatibility and Innovation

Innovation is the third force that drives cost reduction in addition to scalability and compatibility. Innovation enables new test techniques and higher integration. And without real innovation, only short-dated point solutions are possible. On the other hand, innovative ATE test processors can be as integrated as today's smartphones. They can be implemented in inexpensive CMOS technology and make expensive and large components like field programmable gate arrays (FPGAs) redundant, while performing in the several GHz range. Like other technologies, the same is true for ATE – the higher the integration, the lower the cost. The test processor technology has reached an integration and functionality level that scalable platforms with just a few tester cards can cover the full spectrum from low-cost to high-performance. This is the key economic driver.

The Personal Tester: Benefits of Using Low-Cost Configuration for Engineering and Test Program Development

The legacy approach of test program development is that multiple test engineers share the same test system with a full multi-site production configuration. In a scalable ATE platform environment, using the smallest tester class, with its optimized infrastructure costs, allows the concept of a personal tester. A personal tester would be used by a small team in an engineering or office environment to bring up the single site (or dual site) test program, which typically takes 80 percent of the test program development time, but also quickly handles production escalations (qualification lots, customer samples, pre-production lots). The high-volume manufacturing tester configuration needs to be used only for the last 20 percent, which is the final multi-site tweaking and correlation. Since a real scalable platform is by definition compatible, it is possible to move seamlessly from one tester class to another, dependent on the task. Assuming the engineering configuration has just half the price of the production test system, the engineering fleet could be increased by 66 percent with the same level of ATE investment. This potentially improves TTM by as much as 66 percent, providing more debug time and at the same time higher product quality, faster customer escalation handling and more time for test time reduction.

Summary

Today, a wireless test solution needs to cover an even broader range of devices, with different levels of complexity than a decade ago. This article has shown that overall cost reduction can be only successful, if the platform is scalable, compatible and innovative. A scalable and innovative ATE platform can cover the broad range of requirements to test a variety of wireless devices, thus enabling higher asset utilization and manufacturing flexibility. One aspect of scalability is to provide different compatible tester classes with optimized infrastructure. The low-cost classes especially benefit from scalability. They can inherit all the innovative throughput and usability features, which today's legacy low-cost test solutions cannot provide. This enables low-cost ATE, with best in class usability, throughput and economics.

About the Author

Martin Dresler works at Advantest Europe and has more than 16 years of ATE experience in the areas of mixed-signal, high-speed memory and RF in different positions. As RF market development manager, he is researching new types of businesses, products and services, with an emphasis on identifying current and future opportunities in the mitigation of customer needs. He is a frequent presenter at international conferences and has a university teaching assignment in Stuttgart. He holds a Master (Dipl.-Ing.) of electrical engineering from the Technical University of Munich and a Master (Dipl. Wirt.-Ing.) of business administration from the Fern-University Hagen.
Figure 3. Quiescent Currents for a Typical PMIC (WM8326)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Quiescent Current (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-DC1</td>
<td>580 90 25 0</td>
</tr>
<tr>
<td>DC-DC2</td>
<td>580 90 25 0</td>
</tr>
<tr>
<td>DC-DC3</td>
<td>320 110 25 0</td>
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<td>DC-DC4</td>
<td>320 110 25 0</td>
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</tr>
<tr>
<td>LDO2</td>
<td>30 10 5 0</td>
</tr>
<tr>
<td>LDO3</td>
<td>30 10 5 0</td>
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<tr>
<td>LDO4</td>
<td>30 10 5 0</td>
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<tr>
<td>LDO5</td>
<td>30 10 5 0</td>
</tr>
<tr>
<td>LDO6</td>
<td>30 10 5 0</td>
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<tr>
<td>LDO7</td>
<td>110 70 0</td>
</tr>
<tr>
<td>LDO8</td>
<td>110 70 0</td>
</tr>
<tr>
<td>LDO9</td>
<td>110 70 0</td>
</tr>
<tr>
<td>LDO10</td>
<td>110 70 0</td>
</tr>
<tr>
<td>LDO11</td>
<td>2.5 0 0</td>
</tr>
<tr>
<td>System</td>
<td>220 10 2 0</td>
</tr>
</tbody>
</table>

If the PMIC did not have multiple modes of operation, then the quiescent current of the DC-DCs and LDOs would all be Mode 1, and the total quiescent current would be 2643µA. With a PMIC that is able to change modes during normal operation, the quiescent current can be significantly reduced. The values highlighted in gold in Figure 3 are taken from a typical use case, where DC-DC 1, 3 and 4 are required to be in hysteretic mode in order to react to a sudden increase in load current if needed. In this instance, the quiescent current is reduced to 475µA. This would equate to approximately 21 months of standby time with a 7500mAh common in tablets, compared to 3.9 months with a PMIC that was not able to change modes. The same comparison with a typical smartphone battery of 1800mAh would be less than a month for the PMIC, which was restricted to not being able to change modes, however the flexible PMIC would be able to provide over five months of standby time.

Conclusion

In the past it was possible to use a sub-standard PMIC to power the application processors in portable consumer devices. However, in order to provide the consumer with the best user experience and to provide differentiation in an overcrowded market, the PMIC must be optimized to provide the best power delivery. Performance is becoming essential to providing differentiation to the consumer and in facilitating a successful product in the market place. The consumer will no longer accept products that do not last long enough (typical target for a tablet computer is a 10 hour use time) and as the application processor demands more and more power, the selection of PMIC devices will be based on performance.

About the Author

Dr. Jess Brown joined Wolfson Microelectronics in August 2008 and is the principal product line manager for power management, with responsibility for all areas of the product line including product definition, marketing, sales support and product life cycle analysis. He previously worked at Volterra Semiconductor as the European business development manager and prior to that at Vishay Siliconix where he was the mains powered, power IC market development manager. Dr. Brown holds a degree in electrical and electronic engineering from the University of Bath, and a PhD from the University of Sheffield.

References


Lithography Drivers continued from page 20

Figure 2. Pre-Production EUV LPP Source

Conclusion

Although performance metrics still need continued improvement, many thousands of wafers have already been exposed and have demonstrated the outstanding resolution that the industry needs to develop advanced process nodes. The advantage of LPP source technology is that the basic design is scalable to higher power by increasing drive laser power, so that there is confidence EUVL will deliver both the productivity and resolution requirements for continued scaling according to Moore’s Law.

It is an exciting time for the semiconductor industry as demand for advanced chips continues to grow to support the increasing demand for new applications, particularly for consumer applications and mobile computing products. The key to meeting this demand is continued device shrink enabled by advanced lithography. As excimer laser lithography is reaching its limit for the most critical patterning layers, EUVL is becoming ready for introduction into pre-production. The resolution benefits are clear. The real key for success is the high productivity provided by high power LPP sources.

About the Authors

Nigel Farrar is vice president of lithography applications development at Cymer, Inc., and a member of its Scientific Advisory Board. Farrar joined Cymer in 1999 and has led activities to identify the critical performance factors for the light source in advanced lithography processing. He has authored over 40 technical papers in the field of advanced lithography. He holds Bachelor and Doctorate degrees in physics from the University of Bristol in England.

Tommy Oga is the director of strategic marketing at Cymer Inc., and has been with the company for seven years. Dr. Oga has a Bachelor degree in electrical engineering from Kyusyu University, Japan and a Doctorate in engineering from SCU.
Analog Devices Inc. continued from page 10

supply chain?

A: In our non-MEMS businesses, ADI has used a combination of internal and externally sourced supply for many years. In our MEMS businesses, we began with a primarily internal supply chain. Over time, we worked with our existing suppliers as they expanded into MEMs. In some cases, it was a traditional technology transfer model. In other instances, we co-developed new technologies. Today, we interface and cooperate with our MEMs suppliers the same way we do with our traditional electronics suppliers.

Q: Analog Devices recently transferred its stock exchange listing from The New York Stock Exchange to The NASDAQ Global Select Market. Other tech companies have also recently transferred from the NYSE to NASDAQ. What prompted the transfer for ADI?

A: Stock trading is a technology intensive operation and all the world’s major exchanges offer exemplary service. ADI was attracted to NASDAQ’s reputation as the exchange for high technology companies. Moving to the NASDAQ was a seamless process for our shareholders and was cost-effective for ADI. We were partly prompted by the fact that nearly every semiconductor company in the United States is listed on the NASDAQ, but primarily by the opportunity to save money without sacrificing service and performance.

Q: Analog and mixed-signal content is increasing with the wireless market, specifically smartphones, growing at an exponential rate. While this creates great opportunity for analog/mixed-signal IC suppliers, opportunity comes with challenge. IC design is becoming increasingly complex as we move to the leading edge. Describe some of the current design complexities, tools, scalability and advancements in analog/mixed signal.

A: Any market with more than one billion units shipping per year creates some very strong forces in the industry, and the handset market has become a primary driver for integration, cost and power efficiency for the digital as well as analog/mixed signal IC space. The high-level integration required puts pressure on mixed-signal designs to be implemented in advanced “digital” CMOS processes—this means being designed to operate on low supply voltages (1.2V or less), and forgo the expense of special “mixed signal” process steps. New architectures and approaches have been developed to help enable that—and in some cases, performance compromises are made to accommodate the desired integration level.

For system-on-chip (SOC) or system-in-package (SIP) integration, many of the system tradeoffs that were formerly made by the system implementer now fall to the IC provider. This includes the problem of performance verification across multiple domains (analog, digital, radio frequency (RF), power, etc.). The tools are becoming exponentially more sophisticated with techniques like built-in-self-test (BIST) and error detection/error correction architectures becoming more common. In general, it’s not enough to simply “port” old designs or architectures onto the new process nodes. The constraints of very deep submicron technology really call for entirely new architectural approaches.

Q: Analog Devices has been a long-time member of GSA since 1997. What has been one of the greatest benefits of being a GSA member?

A: The benefits of GSA membership for ADI have changed over the years as the semiconductor industry has evolved. In the early days, when GSA was known as FSA, a lot of the benefits came from establishing a more connected ecosystem around the foundry providers and promoting communication and collaboration. Today, GSA provides broader support across the entire supply chain. As a result, ADI directly benefits from GSA’s work to improve foundry process design kits (PDKs) and the pricing surveys used to benchmark technologies and provide useful trends.

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for global revenue and slightly down in terms of shipments. What’s more, despite innovation, the medical market continues to face unique governmental regulation and approval process factors that force product engineers to attempt to plan for potential trends years in advance.

Figure 3: Worldwide Medical Semiconductor Market Forecast

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<td>$0.73</td>
<td>$0.73</td>
<td>-1%</td>
<td>2%</td>
</tr>
</tbody>
</table>

databeans Estimates

Conclusion

There are a handful of macro factors that should have at least a minor impact on general consumer spending this year. This includes the summer Olympics event, which should provide a slight boost in sales of HDTVs as consumers, especially in less penetrated markets, upgrade older sets to view the event. Also, major elections in the U.S., China, France, Russia, Taiwan and South Korea this year should provide another modest consumer market boost, as the incumbent administration attempts to pass short-term legislations in order to prop up the economy and improve consumer sentiment during this crucial re-election phase. Ultimately, after a somewhat weak first half of the year, growing momentum in consumer and business spending during the remainder of 2012 should provide a solid base for total market growth heading into the year 2013. ■

About the Author

Matthew Scherer, a semiconductor market research analyst at research firm Databeans Inc, received his bachelor’s degree in English with an emphasis on technical writing from the University of Nevada, Reno. He has worked in the semiconductor analysis industry for four years, tracking the latest trends in all major IC categories and end markets. However, he is primarily focused in consumer electronics, audio, industrial and embedded markets. Matthew also publishes a monthly newsletter for Databeans, Inc and has submitted materials that have since been quoted in the national press by publications including EDN.com, EETimes, CNBC, Fox News, Nikkei Electronics, Digitimes, the Wall Street Journal, San Jose Mercury News and US News and World Report. Matthew currently resides in Seattle, Washington, where he enjoys creative writing, cooking, tech gadgets and console gaming.
A: It’s true that the demand for mixed-signal devices is on the rise. The interaction between the analog and digital worlds has never been greater. We see a number of critical needs that Silicon Labs is uniquely positioned to address. First is the availability of very low-power devices that can reduce power consumption and/or enable energy to be harvested to eliminate batteries completely. Power efficiency is inherently a mixed-signal problem, and we have low-power design at the heart of all of our IC developments. Second is the increasing need for sensors of all types. We view the integration of high-performance sensors with smart MCUs as central to the next generation of electronic devices.

Q: Short lead times and the ability to get products to market quickly have long been a focus for semiconductor companies. How does Silicon Labs help its customers get products to market quickly?

A: The value proposition of our timing products is directly related to reducing supply chain headaches for customers. For example, crystals have long been a source of time-to-market delay in electronics systems of all kinds. The process for manufacturing them is very mechanical and the sources of supply are geographically concentrated and easily disrupted. We looked at the problem and thought there had to be a better way.

We leveraged our core intellectual property (IP) in digital phase-locked loops (PLLs) and developed a technology to allow customers to buy custom oscillators able to support a very wide range of frequencies in a single device that they can get in two weeks or less, versus the 14-week lead times they were used to getting from other suppliers.

Instead of a solution relying on an unsophisticated IC and a complex crystal resonator subject to reliability and other issues, we developed IC technology to do all of the frequency control and use a relatively simple and low-cost crystal. We can stock these crystals and the blank ICs, program the ICs to our customers’ specifications and ship them in a matter of days. There is no need to have the crystal shaved to a specific frequency, and there is no wait. And if in the course of designing their system, the customer finds that their frequency needs have changed, the same device can be reprogrammed to support the new frequency. This innovative approach has been behind our large market share gains among telecom customers.

Q: You have been with Silicon Labs for nearly as long as the company has been in existence; but you recently took over the helm as President and CEO. How is the transition going, and what are your goals for the future of Silicon Labs?

A: The transition has been very smooth. I worked closely with our former CEO, and I became CEO at a time when we are really primed to accelerate our growth. I love the company. I believe that we have a really special team and a unique culture that has allowed us to take on very challenging designs and achieve a great deal of commercial success.

My focus is on growing the company to a billion dollars. We have the technology and available market to achieve that scale; we need to execute well and make the right product development decisions to ensure we continue to win in the market place.

I am very focused and passionate about products. I spend a lot of time working with the product teams to assess our markets, identify customer needs and be sure that as our customers’ systems evolve, we’ll be ready with the solutions to enable the differentiation they need to succeed.

Q: Silicon Labs recently reported better than expected earnings for Q1 2012, with a five percent increase over the same period in 2011. To what do you attribute such growth, and how are you working to sustain and increase this growth?

A: One of the benefits of mixed-signal products is they tend to have longer life cycles than many IC components. We have however, seen two of our products go through the tail end of their life cycles after five and 10 years respectively of delivering strong profits to the company. With those headwinds largely behind us, we have a number of growth areas we’ve been investing in that are hitting their respective strides. Our video business tripled last year and had a better than expected quarter in Q1. We expect another strong growth year in that product line. Our MCU and timing products also had a strong start to the year, and are both anticipated to grow sequentially each quarter this year. Our emerging business in automotive will be ramping in the second half of 2012, and our small but high-growth businesses in wireless and isolation are also becoming meaningful this year.

We’re in a very good position given the strong R&D investments we’ve been making and feel that with continued focus on product selection and innovation, we’ll be able to gain a disproportionate amount of market share in our target markets.

Global Insights continued from page 7

Figure 3. Comparison of China’s IC Consumption and Production: 1999–2013

This gap represents both an opportunity and challenge for the established multinational semiconductor industry. Over the near term, it continues to represent an unparalleled market opportunity; but over the longer term, it represents a domestic industry void that will inevitably get filled. The question is how will it be filled: will it be a combination transfer and expansion of multinational companies, or the emergence and growth of significant Chinese companies?

About the Author

Raman Chikara is recognized as one of the foremost authorities in the semiconductor industry and has held a variety of prominent leadership roles. He was appointed as PwC’s US semiconductor leader in 1997 before earning the position of global semiconductor leader in 2000 and global technology leader in 2008. As global leader of PwC’s technology practice, he is well versed in the key trends in the tech industry and how such trends translate into challenges and opportunities. In addition to publishing China’s Impact on the Semiconductor Industry study for the past six years, Raman has authored several white papers and thought leadership documents relating to financial reporting matters impacting semiconductor companies.
Volatile Consumer Market Cycles
Consumer electronics are subject to occasionally volatile market cycles. The cycles can be caused by economic cycles, technology changes and consumer taste changes. For the most part, consumer electronics are not necessities. Although some people cannot conceive life without their smartphone, television or tablet PC – these are not basic necessities such as food, shelter, clothing, transportation and medical care. Thus when times get tough, expenditures on consumer electronics are frequently cut.

Businesses are not usually subject to such extremes in electronics purchases. Many electronics systems are necessary for running a business (such as manufacturing equipment or computer systems). Other electronic system purchases can be justified by increases in productivity (such as notebook PCs or tablets for employees in the field).

The chart below shows the annual change in U.S. consumer expenditures on electronics for a 30-year period from the U.S. Department of Commerce. Changes vary from a high of 23 percent in 1983 to a low of -6 percent in 2009. The compound average annual growth rate (CAGR) from 1980 to 2010 was 7.8 percent.

**Figure 3: US Consumer Expenditures on Electronics**

![Figure 3: US Consumer Expenditures on Electronics](image)

After the two recessions in the early 1980s, U.S. consumer spending on electronics grew strongly, driven by relatively new devices such as PCs, VCRs, video game consoles and compact disk (CD) players. Spending slowed around the 1990 recession, growing only 0.5 percent in 1990. Spending was strong again by 1993 as new products, such as lower cost PCs, notebook PCs, DVD players and digital mobile phones emerged. The 2001 recession resulted in another slowdown to two percent growth. Growth returned to double digits in 2004 and remained strong through 2007 as high-definition LCD televisions, digital video recorders, digital cameras, digital audio players and smartphones became popular. The great recession of 2008-2009 resulted in a six percent decline in spending, though growth resumed in 2010.

As illustrated above, volatility in the growth rate of consumer electronics is largely influenced by economic cycles. High growth is due to constant innovation in consumer electronics products. Although early adopters will almost always buy the latest electronic gadgets, most consumers must see a significant advantage to either replace their electronics with improved versions, or buy new types of devices. Just in the last 20-30 years we have seen major shifts in electronics in the typical household.

### Shifts in Consumer Electronic Devices by Function

- Cathode ray tube (CRT) standard definition analog TV => LCD flat screen HD digital TV
- Broadcast TV => cable TV => satellite TV => Internet TV
- VCR => DVD player/recorder => digital video recorder
- Record player => tape player => CD player => digital audio player
- Film still/video camera => digital still/video camera
- Wired telephone => wireless telephone => voice over Internet phone (VoIP)
- Analog mobile phone => digital mobile phone => smartphone
- Desktop PC => notebook PC => tablet PC
- Dialup modem => cable modem => DSL modem => fiber optic modem => WiMax modem

New innovation is a requirement to drive growth in the consumer electronics markets. Many new consumer electronics devices have no previous electronic ancestor. Examples include e-book readers and global positioning system (GPS) navigation devices. If the pace of innovation slows, growth rates will collapse. This is both a risk and an opportunity for semiconductor suppliers. The risk is slower growth if innovation slows; the opportunity for advances in semiconductors are essential to innovation in consumer electronics.

### Conclusion

Despite the risks of the consumer electronics market, it remains a huge growth opportunity for semiconductor suppliers. Semiconductor suppliers must be aware of the risks and be prepared to act quickly to respond to price drops, changing standards and market volatility.

### About the Author

Bill Jewell is principal of Semiconductor Intelligence LLC, a consulting firm specializing in market and company analysis for the semiconductor and electronics industries. Prior to forming Semiconductor Intelligence in 2007, he spent over 20 years in market analysis at Texas Instruments. Bill is a former Americas vice chairman and worldwide chairman of World Semiconductor Trade Statistics (WSTS). He was on the founding executive committee of Semiconductor Industry Capacity Statistics (SICAS). Bill can be reached at billjewell@sc-iq.com.

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